VERTICAL INTEGRATION OF CMOS ELECTRONICS WITH PHOTONIC DEVICES

CROSS-REFERENCES TO RELATED APPLICATIONS

[0001] This application claims priority to U.S. Provisional Patent Application No. 61/588,080, filed on January 18, 2012, entitled "Vertical Integration of CMOS Electronics with Photonic Devices," the disclosure of which is hereby incorporated by reference in its entirety for all purposes.

BACKGROUND OF THE INVENTION

[0002] Advanced electronic functions such as photonic device bias control, modulation, amplification, data serialization and de-serialization, framing, routing, and other functions are typically deployed on silicon integrated circuits. A key reason for this is the presence of a global infrastructure for the design and fabrication of silicon integrate circuits that enables the production of devices having very advanced functions and performance at market-enabling costs. Silicon has not been useful for light emission or optical amplification due to its indirect energy bandgap. This deficiency has prevented the fabrication of monolithically integrated opto-electronic integrated circuits on silicon.

[0003] Compound semiconductors such as indium phosphide, gallium arsenide, and related ternary and quaternary materials have been extremely important for optical communications, and in particular light emitting devices and photodiodes because of their direct energy bandgap. At the same time, integration of advanced electrical functions on these materials has been limited to niche, high-performance applications due to the much higher cost of fabricating devices and circuits in these materials.

[0004] Thus, there is a need in the art for improved methods and systems related to composite integration of silicon and compound semiconductor devices.

SUMMARY OF THE INVENTION

[0005] Embodiments of the present invention relate to methods and systems for template assisted bonding of semiconductor wafers, also referred to as substrates. More particularly, embodiments of the present invention relate to methods and apparatus for wafer-scale

bonding of photonic devices to SOI wafers including CMOS devices. Embodiments of the present invention have wider applicability than this example and also include applications for heterogeneous growth of semiconductor materials or integration of III-V materials for high-speed devices on silicon.

[0006] According to an embodiment of the present invention, methods that enable wafer-scale processing in silicon photonics are provided. As an example, according to an embodiment of the present invention, a method of fabricating a composite semiconductor structure is provided. The method includes providing an SOI substrate including a plurality of silicon-based devices, providing a compound semiconductor substrate including a plurality of photonic or other devices such as high-speed transistors, and dicing or otherwise forming the compound semiconductor substrate to provide a plurality of photonic dies. Each die includes one or more of the plurality of photonic or electronic devices. The method also includes providing an assembly substrate that may already include a plurality of silicon-based devices, such as CMOS devices, mounting the plurality of compound semiconductor dies on predetermined portions of the assembly substrate, aligning the SOI substrate and the assembly substrate, joining the SOI substrate and the assembly substrate to form a composite substrate structure, and removing at least a portion of the assembly substrate from the composite substrate structure.

[0007] Allowing silicon-based devices to be contained within the assembly wafer provides several advantages. For example, the processing required to fabricate silicon-based devices on the SOI substrate that are compatible with the compound semiconductors integrated using the assembly wafer may not be compatible with other silicon-based devices required for the integration process, such as CMOS devices. The inclusion of silicon-based devices in the assembly wafer allows for integration of a broad range of silicon device technologies that require incompatible processing techniques. As an example, in a particular embodiment, the SOI wafer may contain silicon devices that require a 130 nanometer CMOS process while the assembly wafer contains silicon devices that require a 65 nanometer CMOS process. Since these two processes cannot typically be executed on the same wafer, template assisted bonding allows the smaller, faster devices produced in the 65 nanometer process to be integrated with the larger 130 nanometer devices in addition to the compound semiconductor devices.

[0008] According to another embodiment of the present invention, a method of growing a compound semiconductor structure on a silicon-based substrate is provided. The method includes providing an SOI base wafer having a bonding surface, providing a seed wafer, and

dicing the seed wafer to provide a plurality of seed dies. The method also includes providing a template wafer, mounting the plurality of seed dies on the template wafer, and bonding the template wafer to the SOI base wafer. The plurality of seed dies are joined to the bonding surface of the SOI base wafer. The method further includes removing at least a portion of the template wafer, exposing at least a portion of a surface of the plurality of seed dies, and growing the compound semiconductor structure on the exposed seed dies.

[0009] According to an embodiment of the present invention, a method of fabricating a composite semiconductor structure is provided. The method includes providing an SOI substrate including a plurality of silicon-based devices, providing a compound semiconductor substrate including a plurality of photonic devices, and dicing the compound semiconductor substrate to provide a plurality of photonic dies. Each die includes one or more of the plurality of photonics devices. The method also includes providing an assembly substrate having a base layer and a device layer including a plurality of CMOS devices, mounting the plurality of photonic dies on predetermined portions of the assembly substrate, and aligning the SOI substrate and the assembly substrate. The method further includes joining the SOI substrate and the assembly substrate to form a composite substrate structure and removing at least the base layer of the assembly substrate from the composite substrate structure.

[0010] According to another embodiment of the present invention, a method of growing a compound semiconductor structure on a silicon-based substrate is provided. The method includes providing an SOI base wafer having a bonding surface, providing a seed wafer, and dicing the seed wafer to provide a plurality of seed dies. The method also includes providing a template wafer including a plurality of CMOS devices, mounting the plurality of seed dies on the template wafer, and bonding the template wafer to the SOI base wafer. The plurality of seed dies are joined to the bonding surface of the SOI base wafer. The method further includes removing at least a portion of the template wafer, exposing at least a portion of a surface of the plurality of seed dies, and growing the compound semiconductor structure on the exposed seed dies.

[0011] Numerous benefits are achieved using the present invention over conventional techniques. For example, in an embodiment according to the present invention, the use of a template wafer allows more expensive III-V materials to be used sparingly, for example, only where required to implement a specific device function. Thus, the cost structure of the finished product is improved by embodiments described herein by minimizing the quantity of

III-V or other materials needed. Additionally, multiple levels of optical interconnects can be formed in a photonic integrated circuit according to some embodiments by routing optical signals in patterned regions of the template wafer that remain after an anneal process is employed to create a split plane. The attach and split process described herein may be employed a single time or multiple times.

[0012] In a particular embodiment, multiple bonding processes are employed and three dimensional structures of alternating crystalline silicon with interspersed planes of III-V, II-VI, or other materials, are formed. Yet another benefit provided by embodiments of the present invention are that alignment to a silicon base wafer is performed on a wafer-scale basis. Additionally, definition of active stripes or regions may be performed on the III-V or other material after the wafer bonding process, significantly relaxing alignment tolerances.

[0013] Depending upon the embodiment, one or more of these benefits may exist. These and other benefits have been described throughout the present specification and more particularly below. Various additional objects, features and advantages of the present invention can be more fully appreciated with reference to the detailed description and accompanying drawings that follow.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] FIG. 1 is simplified schematic diagram of an integrated optoelectronic device according to an embodiment of the present invention;

[0015] FIG. 2 is a simplified flowchart illustrating a method of fabricating integrated optoelectronic devices according to an embodiment of the present invention;

[0016] FIG. 3A is a simplified plan view of a processed SOI substrate according to an embodiment of the present invention;

[0017] FIG. 3B is a simplified perspective view of a processed III-V substrate and dicing of the processed III-V substrate according to an embodiment of the present invention;

[0018] FIG. 3C is a simplified plan view of an assembly substrate including a plurality of III-V die according to an embodiment of the present invention;

[0019] FIG. 3D is a simplified exploded perspective diagram illustrating joining of the processed SOI substrate and assembly substrate including a plurality of III-V die according to an embodiment of the present invention;

[0020] FIG. 3E is a simplified perspective view of removal of a portion of the assembly substrate from the bonded substrate structure illustrated in FIG. 3D;

[0021] FIG. 4 is a simplified schematic diagram illustrating a portion of a composite substrate structure after wafer bonding, assembly substrate splitting, and polishing according to an embodiment of the present invention;

[0022] FIG. 5 is a simplified plan view of a substrate with integrated optoelectronic devices according to an embodiment of the present invention.

[0023] FIG. 6 is a simplified flowchart illustrating a method of fabricating integrated optoelectronic devices according to another embodiment of the present invention;

[0024] FIG. 7A is a simplified schematic diagram illustrating a portion of a composite substrate structure during device definition according to an embodiment of the present invention;

[0025] FIG. 7B is a simplified schematic diagram illustrating a portion of a composite substrate structure after processing according to an embodiment of the present invention;

[0026] FIG. 7C is a simplified schematic diagram of a multilayer structure according to an embodiment of the present invention;

[0027] FIG. 8 is a simplified flowchart illustrating a method of performing heterogeneous epitaxial growth according to an embodiment of the present invention;

[0028] FIGS. 9A - 9E are simplified schematic diagrams of a portion of a composite substrate structure at various fabrication stages according to an embodiment of the present invention;

[0029] FIG. 10 is a simplified schematic diagram of a multilayer structure fabricated according to an embodiment of the present invention;

[0030] FIGS. 11A - 11C are simplified schematic diagrams illustrating a process for vertically integrating CMOS devices using a template assisted bonding process according to an embodiment of the present invention;

[0031] FIG. 12 is a simplified flowchart illustrating a method of vertically integrating CMOS devices using a template assisted bonding process according to an embodiment of the present invention;

[0032] FIG. 13 is a simplified flowchart illustrating a method of fabricating a composite semiconductor structure according to an embodiment of the present invention; and

[0033] FIG. 14 is a simplified flowchart illustrating a method of growing a compound semiconductor structure on a silicon-based substrate according to an embodiment of the present invention.

DETAILED DESCRIPTION OF SPECIFIC EMBODIMENTS

[0034] According to the present invention, methods and systems related to template assisted bonding of semiconductor wafers are provided. Merely by way of example, the invention has been applied to a method of bonding III-V dies (or device regions for more complex circuits) to a substrate at a wafer level using an assembly substrate (also referred to as a template wafer/substrate). The method and apparatus is applicable to a variety of semiconductor processing applications including wafer-scale processing of photonics integrating silicon-devices and silicon circuits integrating high-speed electronic functions with compound semiconductor devices.

[0035] The inventors have determined that the commercial significance of silicon photonics will be enhanced if cost and power can be reduced relative to discrete implementations while not sacrificing performance. According to embodiments of the present invention, performance parity is achieved by integrating III-V materials onto the silicon photonic wafer as a wafer-scale process. As described more fully throughout the present specification, template-assisted bonding provides a wafer-scale processing paradigm for the composite integration of III-V materials with silicon or silicon-on-insulator that is amenable to batch processing (cassette to cassette).

[0036] Without limiting embodiments of the present invention, the following definitions are used to define processes and structures described herein:

[0037] Composite Bonding: A wafer bonding process using a combination of metal to metal, metal interface layer assisted, and/or direct semiconductor bonding to achieve a combination of the desirable characteristics of each of these techniques. Benefits provided by these techniques include, without limitation, strength for a metal to metal bond, ability to accommodate thermal expansion coefficient mismatches and surface roughness for metal interface layer assisted, and optical transparency for direct semiconductor bonding.

[0038] Composite Semiconductor-on-Insulator (C-SOI): A silicon photonic wafer that combines wafer-bonded III-V materials on a silicon-on-insulator substrate to create a composite of III-Vs, silicon, and potentially other materials. The resultant stack is referred to as a composite semiconductor-on-insulator wafer, or a C-SOI wafer or substrate.

[0039] Template-Assisted Bonding: Wafer bonding of pieces at a wafer-scale level through the intermediate step of producing a template. As described throughout the present specification, in an embodiment, an intermediate carrier (also referred to as an assembly substrate), for example, a carrier that has been prepared to include an implant region to enable a cleaner separation of the material on the template from the carrier substrate, is utilized.

[0040] FIG. 1 is simplified schematic diagram of an integrated optoelectronic device 100 according to an embodiment of the present invention. Referring to FIG. 1, an SOI substrate 110 (also referred to as a base wafer) including a silicon handle wafer 112, an oxide layer 114 and a single crystal silicon layer 116 is processed to form one or more electronic circuits, photonic elements such as waveguides, multimode interference couplers, gratings, index tuning elements, Mach-Zehnder modulators (MZMs), or the like. As an example, CMOS circuits can be fabricated in silicon layer 116 providing for a wide variety of electrical device functionality. In the schematic diagram illustrated in FIG. 1, these circuits and elements are formed in layer 116 although the actual device components can extend outside layer 116. Although an SOI substrate 110 is illustrated in FIG. 1, some embodiments utilize a silicon wafer in place of the SOI substrate.

[0041] A waveguide 130 formed in the device layer of the assembly substrate (described more fully throughout the present specification) is illustrated in FIG. 1. As shown in FIG. 1, this device layer provides for multiple functionalities, including an electrical interconnect layer connected to CMOS circuitry formed in the single crystal silicon layer 116 of the SOI substrate through via 132. The waveguide 130 can be an optical waveguide defined in the device layer to interconnect optical devices or to bring the optical signal from one section of the structure to another section. Thus, the device layer of the assembly substrate the template wafer itself can be processed into several different types of functional applications. One of ordinary skill in the art would recognize many variations, modifications, and alternatives.

[0042] Another function of the device layer in the assembly wafer may include formation of CMOS circuitry that cannot typically be formed in the base wafer as depicted in FIG. 11. The formation of CMOS circuitry in a separate wafer enables the use of a CMOS process that

may otherwise be unavailable if only forming CMOS circuits in the base wafer. After formation of CMOS circuitry in the assembly wafer, the subsequent processing steps described herein for template assisted bonding still apply.

[0043] In one embodiment, the substrate can be removed from the standard silicon process flow (e.g., a CMOS process flow) prior to metal patterning. The lack of metal patterning enables higher temperature processing to be performed during the template assisted bonding process described herein. In this embodiment, the substrate can be returned to the fabrication facility or other suitable processing facility for completion of the standard silicon process after the template assisted bonding process. FIG. 3A is a simplified plan view of a processed SOI substrate corresponding to SOI substrate 110 illustrated in FIG. 1. The processed SOI substrate includes a plurality of device regions illustrated by the grid shown in FIG. 3A.

[0044] FIG. 3B is a simplified perspective view of a processed III-V substrate and dicing of the processed III-V substrate according to an embodiment of the present invention. In the embodiment illustrated in FIG. 3B, dicing is performed using a saw blade but embodiments of the present invention are not limited to this particular dicing method and other techniques are included within the scope of the present invention. Typically, III-V substrates are smaller than the processed SOI substrate illustrated in FIG. 3A. After the dicing operation illustrated in FIG. 3B, a plurality of III-V dies are available for mounting to an assembly substrate as described more fully throughout the present specification. III-V dies can include elements suitable as gain chips, photodetectors, MZMs, circulators, a variety of electronics such as high speed transistors, or the like, thereby providing both photonics as well as electronics. Although dicing is discussed in relation to some embodiments, the present invention is not limited to this particular technique for separating materials into smaller sections for bonding. As will be evident to one of skill in the art, dicing is one method suitable for use with embodiments of the present invention and other separation methods such as cleaving, etching, or the like are included within the scope of the present invention and may be utilized as well.

[0045] FIG. 3C is a simplified plan view of an assembly substrate including a plurality of III-V die according to an embodiment of the present invention. Although not illustrated in FIG. 3C, the assembly substrate, also referred to as a template substrate or wafer is processed to provide a mechanism for wafer separation. In an embodiment, the assembly substrate (e.g., a silicon substrate that is the same size as the processed SOI substrate) is oxidized and ion implanted (e.g., using H_2^+ or He_2^+ ions) to form a wafer separation region (i.e., a fracture plane) at a predetermined depth into the assembly substrate. Such a process is illustrated in the assembly substrate - base layer (also referred to as a base region) and assembly substrate -

device layer (also referred to as a device region) as shown in FIG. 3D. According to the illustrated embodiment, implant separation is used to accomplish substrate removal, but it is also possible to physically remove the bulk of the template wafer by mechanical thinning or other lapping techniques.

[0046] In FIG. 3C, the plan view includes the surface of the base layer adjacent the dies and the various III-V dies. The device layer of the assembly substrate can then be patterned with alignment features and/or bonding locations for attachment of the III-V dies as illustrated in FIG. 3C. In addition to III-V die, other devices, structures, and materials can be joined to or mounted on the assembly substrate as appropriate to the particular application. In some embodiments, the strength of the bond between the III-V dies and the assembly substrate is varied as appropriate to the particular application. Thus, both strong and weak bonding between these elements is included within the scope of the present invention. Examples of the other materials that can be attached to the defined bonding locations on the assembly substrate are one or multiple III-V materials, II-VI materials, magnetic materials, silicon-based materials (e.g., silicon material with different characteristics than the silicon from the assembly substrate), nonlinear optical materials, or other materials that provide a functional enhancement to the functions provided by the devices on the processed SOI substrate. Attachment of the III-V dies or other materials can be performed using a pick and place tool or other suitable die attach systems.

[0047] FIG. 3D is a simplified exploded perspective diagram illustrating joining of the processed SOI substrate and the assembly substrate including the plurality of III-V die according to an embodiment of the present invention. The III-V dies mounted on the assembly substrate are represented as a III-V device matrix in FIG. 3D and one of skill in the art will appreciate that reference to a matrix indicates, not a continuous layer, but a dimension in which the III-V dies are distributed. As illustrated in FIG. 3D, the devices on the processed SOI substrate are aligned with the III-V die mounted on the assembly substrate and the two substrates are joined to form a bonded substrate structure. As will be evident to one of skill in the art, alignment of the elements provides for placement of the III-V dies mounted on the assembly substrate relative to the electronic and/or photonic circuits present on the SOI substrate. Several methods of performing wafer bonding are included within the scope of the present invention, including methods discussed in U.S. Patent Application No. 12/902,621, filed on October 12, 2010, the disclosure of which is hereby incorporated by reference in its entirety for all purposes.

[0048] In a particular embodiment, an interface assisted bond is formed between the semiconductor elements (e.g., between the layers of the SOI substrate and the III-V dies) in which an intermediate layer (e.g., In_xPd_y, for example, $In_{0.7}Pd_{0.3}$), provides an ohmic contact and optical quality including transparency, stress accommodation, and other benefits.

[0049] FIG. 3E is a simplified perspective view of removal of the base region of the assembly substrate from the device region of the assembly substrate portion of the bonded substrate structure illustrated in FIG. 3D. In an embodiment, an ion implantation process performed on the assembly substrate as discussed above allows for wafer separation of a portion of the assembly substrate (the base region) to occur as illustrated in FIG. 3E. As shown in FIG. 3E, the base region of the assembly substrate is removed, and may be used again in a manner analogous to substrate reuse associated with SOI substrate fabrication and reuse techniques. Although the wafer separation process is illustrated as following the substrate bonding process, this is not required by the present invention and wafer separation may be performed before, during, or after the wafer bonding process.

[0050] In some embodiments, the processes illustrated in FIGS. 3D and 3E are combined as heat from the bonding process causes the assembly substrate to split along the plane defined by the peak of the implanted species. In other embodiments, the assembly substrate is split during an anneal process that is performed either prior to or following the bonding process. One of ordinary skill in the art would recognize many variations, modifications, and alternatives. In yet other embodiments, lapping and/or polishing steps are utilized to move the base layer portion.

[0051] The processed SOI substrate, the attached III-V die matrix, and the device region of the assembly substrate, which can include a thin silicon layer or an oxide/silicon layer associated with the device region of the assembly substrate, as illustrated in FIG. 3E can be polished using a CMP process or other polishing process to remove any residual roughness produced by the splitting process. Thus, embodiments provide a substrate 350 that includes a silicon - III-V - silicon stack suitable for use in fabricating integrated optoelectronic devices. The substrate 350 resulting in FIG. 3E, can be further processed to define additional optical or electronic devices in the thin silicon layer. Electrical interconnects are made to the other materials as needed. Referring to FIG. 1, a portion of the device layer of the assembly substrate remains on the left portion of the device and another portion is processed to form a waveguide. A via is illustrated as passing through the device layer of the assembly substrate to make electrical contact to silicon layer 116 on the processed SOI substrate. Planarizing material is deposited to planarize and passivate the surfaces of the various device elements.

Examples of planarizing material include silicon dioxide, silicon nitride, silicon oxynitride, polyimide or other polymeric materials, spin-on glasses, cyclotene, pyraline, or the like. Planarizing materials may be first applied to the base wafer structure 110 and then patterned to open access areas through which the device elements may be attached to the base wafer.

[0052] As an example, if the device region of assembly substrate includes a silicon layer (e.g., single crystal silicon), this silicon layer can be removed or patterned to form optical interconnects on the chip. This enables optical routing to be provided in a process that can be repeated for multiple optical levels. In embodiments in which the processed SOI substrate was removed from the fabrication facility prior to metallization processes, it is returned for those process steps to be performed.

[0053] As an alternative to the wafer splitting based on an ion implantation process as illustrated in FIG. 3E, other embodiments utilize bulk removal of a portion of the assembly substrate, for example, using a chemical mechanical polishing (CMP) process. This technique can be useful when thicker silicon top layers are desired in the finished structures. One of ordinary skill in the art would recognize many variations, modifications, and alternatives.

[0054] In an embodiment, the substrate 350 including a number of integrated optoelectronic devices as illustrated in FIG. 3E can be used as a new assembly substrate in order to create a multi-layer stack of silicon and other materials by repeating the processes illustrated in FIGS. 3C-3E. Patterning and planarization may be performed as the processes are repeated to define multiple layers of optical interconnects. After processing, the substrate 350 can be diced to provide singulated dies (such as the device illustrated in FIG. 1) for testing and use.

[0055] Utilizing the template assisted bonding process illustrated in FIGS. 3A-3E, a variety of devices including III-V dies, other materials suitable for use as gain chips, photodetectors, MZMs, circulators, high-speed electronic devices, or the like, are mounted on the assembly substrate, which can be a hydrogen implanted silicon wafer that is patterned with alignment targets and/or material attach sites. In some implementations, hydrogen, helium, or other implantation processes are performed prior to patterning to define the split plane illustrated in FIG. 3E along which the SOI wafer splits, for example, during an anneal step. Referring to FIG. 3E, the illustrated embodiment includes a thin silicon device layer, creating a silicon – III-V – silicon stack. The device layer can be removed or patterned to form optical interconnects on chip and to enable optical routing, which can be repeated for multiple

optical levels. As an example, traces could be patterned in the silicon to form, effectively, an upper plane of optical waveguides. As another example, connections could be formed between multi-core processors in the SOI substrate and optical waveguides in the device layer. In some embodiments, the assembly substrate can be repolished and reused. As illustrated in FIG. 10, the processes described herein can be repeated to create multi-layer stacks of III-V dies and silicon, allowing for multi-layer optical interconnects to be formed.

[0056] Referring to FIG. 3C, device layer 312 is processed to fabricate a plurality of CMOS devices and provides a layer of silicon on top of the III-V device matrix that is suitable for further processing after bonding of the composite substrate structure. As described more fully herein, in some embodiments, processing of device layer 312 is performed prior to mounting of the III-V die on the assembly substrate. As an example, this layer can be polished and used to fabricate additional devices, providing a stack of vertically integrated devices. Thus, embodiments of the present invention provide methods and techniques in which CMOS devices can be fabricated in device layer 312. Subsequently, the III-V device matrix can be mounted and bonded to device layer 312. Then, when the bonded substrate structure is formed as illustrated in FIG. 3D and the base layer is removed as illustrated in FIG. 3E, the III-V device matrix is present with the illustrated device layer 312, which can include CMOS devices, elements, electronics, and structures. Moreover, additional processing could then be performed on device layer 312, for example, subsequent processing after bonding to complete the fabrication processes for one or more the CMOS electronics in that device layer, such as the formation of metal interconnects. Thus, embodiments of the present invention include CMOS fabrication techniques in which a portion of the CMOS elements would be formed prior to bonding of the composite substrate structure and other portions of the CMOS elements would be formed after bonding of the composite substrate structure.

[0057] FIG. 2 is a simplified flowchart illustrating a method 200 of fabricating integrated optoelectronic devices according to an embodiment of the present invention. The method includes processing a III-V substrate to form III-V devices (210), such as lasers, optical gain media, detectors, modulators, optical elements, or the like. In addition to the formation of III-V devices other materials can be processed to form magnetic device elements for devices such as optical circulators or isolators, other optoelectronic elements, and the like. After device processing, the III-V substrate can be lapped to form a uniform thickness and diced to provide III-V dies (212). Lapping is not required.

[0058] The method also includes preparing an assembly substrate (220). In an embodiment, a silicon substrate is oxidized, implanted, and patterned to provide mounting locations for the III-V dies discussed above (222). The assembly substrate in this embodiment includes a base region and a device region separated by a split plane defined by the peak of the implant dose (e.g., formed during a hydrogen implantation process). The patterning process can include definition of metal patterns on the template wafer that define locations where the semiconductor pieces (e.g., III-V semiconductor devices) are bonded. In some embodiments, in addition to or in place of metal patterns, targets are formed during the patterning process to provide an indication of locations at which the semiconductor pieces (e.g., III-V semiconductor devices) are directly bonded. As described more fully throughout the present specification, the device region is bonded to the processed SOI substrate and used for device fabrication and the base region is removed and potentially reused. An SOI substrate is processed (230) to provide CMOS devices, electronics, photonic elements, and the like. The SOI substrate is prepared for wafer bonding operations including surface preparation (232). The assembly substrate and the SOI substrate are aligned (240) and a wafer bonding process is performed to join the two substrates and form a composite substrate structure (242).

[0059] Thus, embodiments of the present invention provide III-V devices that can provide photonic and/or electronic functionality as well as CMOS devices (e.g., electronics) fabricated on the assembly substrate that can complement the functionality provided through the III-V devices. Accordingly, depending on the particular application, some of the electronics functionality can be implemented in cost-effective CMOS elements while some of the other electronics functionality can be implemented in III-V devices as appropriate to the particular application.

[0060] An anneal process is then used to split the assembly substrate at the depth at which the peak of the implant dose lies (244). In some embodiments, this step is omitted since the assembly substrate splits as a result of the wafer bonding process (242). In some embodiments, the substrate after splitting is polished (246) to remove surface roughness resulting from the splitting process. FIG. 4 is a simplified schematic diagram illustrating a portion of a composite substrate structure after wafer bonding, assembly substrate splitting, and polishing according to an embodiment of the present invention. Subsequent processing can also be performed to pattern optical waveguides in the device layer of the assembly substrate (248) and to form electrical interconnects (250). The bonds between the bond pads, the SOI substrate, and the III-V dies, as well as the bonds between the III-V dies and the SOI

substrate can be metal-assisted bonds, semiconductor-semiconductor bonds, or the like, as described in U.S. Patent Application No. 12/902,621, referenced above.

[0061] Although the assembly substrate can be split at or near the depth of the implant dose peak, embodiments of the present invention are not limited to this particular split depth and other depths other than the peak of the implant dose can be achieved. Also, it should be noted that while splitting using an anneal process is described herein as a method of removing the assembly substrate, other methods are included within the scope of the present invention, for example, without limitation, lapping to remove the bulk of the assembly substrate, or other suitable techniques.

[0062] It should be appreciated that the specific steps illustrated in FIG. 2 provide a particular method of fabricating integrated optoelectronic devices according to an embodiment of the present invention. Other sequences of steps may also be performed according to alternative embodiments. For example, alternative embodiments of the present invention may perform the steps outlined above in a different order. Moreover, the individual steps illustrated in FIG. 2 may include multiple sub-steps that may be performed in various sequences as appropriate to the individual step. Furthermore, additional steps may be added or removed depending on the particular applications. One of ordinary skill in the art would recognize many variations, modifications, and alternatives.

[0063] FIG. 5 is a simplified plan view of a substrate with integrated optoelectronic devices according to an embodiment of the present invention. Referring to FIG. 5, the SOI substrate is illustrated with electrical bond pads formed at peripheral portions of the SOI substrate. CMOS circuits are typically formed in the SOI substrate. Silicon waveguides formed in the device layer of the assembly substrate provide for optical communication between III-V devices located at the III-V device regions and CMOS elements formed in the SOI substrate and/or other III-V devices. As an example, four multi-core processors fabricated in the four illustrated portions of the CMOS circuitry region can be interconnected using optical waveguides optically coupled to the illustrated III-V devices.

[0064] FIG. 6 is a simplified flowchart illustrating a method of fabricating integrated optoelectronic devices according to another embodiment of the present invention. In the embodiment illustrated in FIG. 6, unprocessed epitaxial material is thinned and attached to an assembly substrate for further processing. The method 600 includes growing epitaxial structures and preparing other materials (610) useful for lasers, detectors, modulator, optical elements, high-speed electronics, magnetic devices, or the like. These unprocessed wafers

can be diced (612) to form device elements for further processing. The unprocessed wafers can be thinned after or as part of the epitaxial growth process.

[0065] An assembly wafer is prepared (620), for example by oxidizing, implanting, and patterning a silicon wafer to form a device layer and a base layer. In some embodiments, one or more of these steps are not performed as appropriate to the particular application. As illustrated in process 620, in addition to the processing of the assembly substrate described above, CMOS devices can be fabricated on the assembly substrate to provide a variety of CMOS element functionality.

[0066] The device elements from the unprocessed wafer are mounted onto the assembly wafer (622). Because of the provision of CMOS elements or devices on the assembly substrate, the device elements mounted in process 622, can be mounted in conjunction with the CMOS devices provided in process 620.

[0067] An SOI base wafer is processed (630), which can include the formation of CMOS circuits, electronics, and photonic elements and prepared for wafer bonding (632). In an embodiment, additional metals are deposited onto the SOI base wafer to form contact regions to the unprocessed epitaxial material during the wafer bonding process described below.

[0068] The assembly wafer and SOI base wafer are aligned (640) and wafer bonded (642). In an embodiment, the assembly wafer is aligned to the SOI base wafer, but this is not required by embodiments of the present invention. The assembly wafer is split using an anneal process, for example, at approximately the peak of the implant dose (644). A polishing process (e.g., CMP) is used to remove surface roughness resulting from the separation of the device layer of the assembly wafer from the base layer of the assembly substrate (646).

[0069] After the wafer bonding process and removal of the base layer of the assembly wafer, additional process steps such as patterning of the device layer to form optical waveguides (648) and proton implantation or III-V oxidation (650) may be performed to define active stripe regions on the epitaxial material. For example, during a proton implantation process, the energy of the implant is selected such that an implant through the "back" of the device structure (formed in the III-V material) defines the stripe region in the material adjacent to the bond to the SOI base wafer. Planarization of layers (652) and repeating of one or more of the steps illustrated in FIG. 6 can be used to build up a multilayer structure. Patterning of electrical interconnects to the III-V materials is performed in some embodiments (654).

[0070] In the embodiment illustrated in FIG. 6, epitaxial material is bonded and then post-processed to define stripe regions and interconnects to the regions on the processed SOI substrate that can include optics and have other traces defined on them. An advantage of the embodiment illustrated in FIG. 6 is the reduction or elimination of tight alignment tolerances associated with pre-defined features on the III-V devices. Thus, although the embodiment illustrated in FIG. 6 shares common elements with the embodiment illustrated in FIG. 3, the method illustrated in FIG. 6 may provide benefits not available using the method illustrated in FIG. 1. As an example, because the active stripe region is formed after bonding in the embodiment illustrated in FIG. 6, the alignment tolerance of both the process of attachment to the assembly wafer and the alignment of the assembly wafer to the SOI base wafer are substantially reduced (on the order of approximately ±1 μm to approximately ±10 μm).

[0071] It should be appreciated that the specific steps illustrated in FIG. 6 provide a particular method of fabricating integrated optoelectronic devices according to an embodiment of the present invention. Other sequences of steps may also be performed according to alternative embodiments. For example, alternative embodiments of the present invention may perform the steps outlined above in a different order. Moreover, the individual steps illustrated in FIG. 6 may include multiple sub-steps that may be performed in various sequences as appropriate to the individual step. Furthermore, additional steps may be added or removed depending on the particular applications. One of ordinary skill in the art would recognize many variations, modifications, and alternatives.

[0072] FIG. 11 illustrates a method of vertically integrating CMOS circuitry according to another embodiment of the present invention. In the embodiment illustrated in FIG. 11, the CMOS circuitry is formed in the device layer of the assembly wafer during preparation of the assembly wafer. The CMOS devices formed in the device layer of the assembly wafer may include but are not limited to CMOS devices, logic circuits, or emitter coupled logic circuits, BiCMOS circuits, SiGe BiCMOS circuits, NMOS circuits, PMOS circuits, or other silicon-based devices or circuits. In a particular embodiment, the CMOS devices formed in the device layer are devices that utilize a CMOS fabrication process not compatible with the processes utilized in fabricating the base or SOI wafer. After formation of the CMOS circuitry, the assembly wafer is used in a way that is similar to that described by FIG. 6 in that unprocessed III-V device elements are mounted to the assembly wafer. An SOI wafer with photonic device elements is prepared for wafer bonding. The SOI wafer and assembly wafer are aligned and bonded. After the bonding process, in this embodiment, the bulk of the assembly wafer is removed using a chemical mechanical polish, etching process, or other

suitable technique. After removal of the bulk of the assembly wafer substrate, additional processing steps may be performed to define device regions in the III-V material. Metallization processes are used to form interconnects between the CMOS circuitry and the photonic devices.

[0073] FIG. 7A is a simplified schematic diagram illustrating a portion of a composite substrate structure during device definition according to an embodiment of the present invention. As illustrated in FIG. 7A, the III-V device elements (or other materials) are bonded to the SOI base wafer such that the planarizing material may be under the device layer or above the device layer. In one process flow provided by embodiments of the present invention, openings are defined in the planarizing material that allow the III-V device to be bonded. Formation of the planarizing material under the device may occur if access regions in the template wafer allow the formation of this planarizing material subsequent to the patterning of the template wafer, but prior to definition of the implant mask. Regions are opened to access the III-V device and an implant mask is formed on the "back" side of the III-V device elements and as described above, the implant defines the active regions. After implantation, post-processing is performed to define interconnects, provide for planarization, and the like.

[0074] FIG. 7B is a simplified schematic diagram illustrating a portion of a composite substrate structure after processing according to an embodiment of the present invention. As illustrated in FIG. 7B, the implant mask has been removed and an additional planarizing material has been deposited and planarized to provide passivation among other benefits.

[0075] FIG. 7C is a simplified schematic diagram of a multilayer structure according to an embodiment of the present invention. As illustrated in the cross section in FIG. 7C, multiple levels of silicon and III-V materials are formed by using the embodiments described herein. Silicon layers can be used to create optical waveguides or can be patterned with vias to carry electrical connections to the III-V semiconductors or other materials in the layer stack. Utilizing embodiments of the present invention, it is possible to create circuits in the illustrated silicon device layers (originally from the assembly wafer), thus creating a "3-D" integrated optoelectronic circuit. One of ordinary skill in the art would recognize many variations, modifications, and alternatives.

[0076] FIG. 8 is a simplified flowchart illustrating a method of performing heterogeneous epitaxial growth according to an embodiment of the present invention. The method 800 utilizes crystal "seeds" that are attached to the assembly wafer and then bonded to a processed

wafer, for example, a silicon or SOI wafer using, for example, either direct wafer bonding or metal-assisted bonding. Metal assisted bonding is utilized in some embodiments since the metal layer helps to accommodate stress between materials with dissimilar thermal coefficients of expansion. The seed material may be any non-silicon crystalline material that is desired on the silicon, for example, InP or GaAs seed material or other suitable materials. Although an assembly wafer is utilized in the embodiment illustrated in FIG. 8, this is not required by the present invention and some embodiments dispense with the use of the assembly wafer and grow epitaxial material on a generic wafer having a dissimilar lattice constant. In other embodiments, III-V material mounted on an assembly wafer form a layer of seeds for epitaxial growth of III-V materials on an SOI wafer following high-temperature CMOS processing steps. One of ordinary skill in the art would recognize many variations, modifications, and alternatives.

[0077] Referring to FIG. 8, the method 800 includes lapping a seed material wafer to a uniform thickness (810). In some embodiments, the seed material wafer is received at a uniform thickness and step 810 is omitted. Seed material may also be lapped and polished to a uniform thickness subsequent to the mounting to the assembly wafer (822). The seed material wafer is diced (812) to provide a plurality of seed material dies. In various embodiments, the seed material is a III-V material, a II-VI material, a magnetic material, a non-linear optical material, or the like. An assembly wafer is prepared and one or more CMOS devices are fabricated in a device layer of the assembly wafer (820).

[0078] The seed material dies are mounted to the assembly wafer (822). During preparation of the assembly wafer (820), the oxidation, implant, and patterning steps may all be used or a subset may be used as part of or in addition to the CMOS device element fabrication steps. For example, any or all steps may be eliminated depending upon the particular structure of the overall 3-D layer stack. The fabrication of CMOS devices on the assembly wafer enables the integration of the seed material mounted in process 822 with a variety of CMOS devices.

[0079] An SOI base wafer is processed up to, but not through, metal deposition processes (830) and the SOI base wafer is prepared for wafer bonding (832). In the illustrated embodiment, the SOI base wafer is processed up to the metal deposition processes, but this is not required by the embodiments of the present invention. In other embodiments, the SOI processing is stopped prior to steps preceding the metal deposition processes and these steps prior to the metal deposition processes are then performed after epitaxial growth (e.g., at step

850). One of ordinary skill in the art would recognize many variations, modifications, and alternatives.

[0080] The assembly wafer is aligned with the SOI base wafer (840) and wafer bonding is performed to join the wafers together (842). FIG. 9A illustrates the implanted assembly wafer with the attached III-V seed dies aligned with the SOI wafer prior to wafer bonding. As described more fully below, the embodiment illustrated in FIGS. 9A - 9E utilizes III-V seed crystals in a selective epitaxial growth process. As an example, rather than bonding an InP structure containing various epitaxial layers, a set of InP seed crystals are bonded to the assembly substrate, which is then bonded to an SOI substrate. Openings are made to expose the InP seed crystals, and selective epitaxy is performed define device regions (e.g., gain materials in a first region, detectors in another region, MZM devices in a third region, etc.), thus providing a generalized approach for selectively growing III-V materials on selected regions overlying silicon devices. Mixed seed materials may be used, for example InP and GaAs, III-V and II-VI material, or the like.

[0081] FIG. 9B illustrates the implanted assembly wafer after a CMP process is performed to planarize the surface of the seed dies and the device layer of the assembly wafer. Wafer bonding of the two wafers is illustrated in FIG. 9C. The assembly wafer is split at approximately the implant dose peak to form a device layer and a base layer in embodiments utilizing an implantation process. In other embodiments, the assembly wafer is polished to remove a portion of the assembly wafer. In the embodiment illustrated in FIG. 9D, a CMP process is used to remove surface roughness at the split plane. The base layer has been removed and is not illustrated in FIG. 9D. In some embodiments in which the processed devices are attached to the assembly wafer, the thickness tolerances of the III-V seed dies is controlled (e.g., by a polishing process) to provide for uniform bonding between bond sites on the SOI substrate and the III-V seed dies. In addition to CMP processing, a dry or wet chemical etch process could be used to open a hole above the III-V seeds to provide an area for epitaxial growth through the hole.

[0082] Access areas are opened for growth on the seed material dies (848) and epitaxial structures are grown using selective epitaxy as illustrated in FIG. 9E. The seed material may be accessed through wet or dry etching, CMP, or the like. Thus, although the seed material dies are mounted on an SOI wafer at this stage of the process, epitaxial growth of materials with a lattice constant dissimilar from silicon can be performed to form epitaxial materials lattice matched to the seed material dies. Thus, heterogeneous growth (III-V materials on a

silicon substrate (e.g., an SOI substrate)) are provided by embodiments of the present invention.

[0083] After growth of epitaxial structures lattice matched to the seed material, the remainder of the CMOS processing, as well as processing of the seed materials (e.g., III-V materials) can be performed, including the metal deposition steps not performed in step 830. Different seed materials may be accessed at different points in the process for embodiments in which growth on multiple different seed materials is performed (for example, both GaAs and InP). Masking of predetermined portions of the substrate can be performed to access these varied seed materials.

[0084] In light of the applicability of the methods and systems described herein to different seed materials, it should be noted that embodiments of the present invention are therefore useful for applications where high-speed III-V devices or circuits are incorporated onto the silicon wafer and embodiments of the present invention are not limited to optical elements joined to the silicon substrate. As another example, embodiments of the present invention are useful for the fabrication of short-distance optical interconnects (e.g., core-to-core, chip-to-chip, or the like) that can be combined with longer-haul optical devices. Further examples might include integration of high-speed transistors for circuits (such as power amplifiers) with other circuits formed in CMOS for wireless communications applications.

[0085] The various steps illustrated in FIG. 8 can be repeated to form a multilevel structure as discussed in relation to FIG. 6. It should be appreciated that the specific steps illustrated in FIG. 8 provide a particular method of performing heterogeneous epitaxial growth according to an embodiment of the present invention. Other sequences of steps may also be performed according to alternative embodiments. For example, alternative embodiments of the present invention may perform the steps outlined above in a different order. Moreover, the individual steps illustrated in FIG. 8 may include multiple sub-steps that may be performed in various sequences as appropriate to the individual step. Furthermore, additional steps may be added or removed depending on the particular applications. One of ordinary skill in the art would recognize many variations, modifications, and alternatives.

[0086] Utilizing the methods illustrated in reference to FIGS. 8 and 9A-9E, seed crystals are attached to the assembly substrate and then bonded to a silicon or SOI substrate using direct wafer bonding, metal-assisted bonding, or the like. Some embodiments utilize metal-assisted bonding since the metal layer will help to accommodate stress between materials with dissimilar TCEs. The seed material can be non-silicon crystalline materials that are

integrated with silicon, for example, InP, GaAs, other III-Vs, II-VIs, or other suitable seed material. In an alternative embodiment, the assembly substrate is not used and epitaxial structures are formed on a substrate having a dissimilar lattice constant. As illustrated, the seed material may be accessed through wet or dry etching, CMP, or the like.

[0087] Different seed crystals may be provided and/or accessed at different points in the process if growth on multiple different seed materials is desired (for example, both GaAs and InP or a II-VI). The use of multiple seed materials will be useful for applications in which high-speed III-V devices or circuits are incorporated onto the silicon structure. Thus, embodiments of the present invention are not limited to optical interconnection applications. As another example, this process would be applicable to the combination of short-distance optical interconnects (e.g., core-to-core, chip-to-chip) with longer-haul optical devices.

[0088] FIG. 10 is a simplified schematic diagram of a multilayer structure fabricated according to an embodiment of the present invention. In the embodiment illustrated in FIG. 10, an SOI substrate including CMOS devices is provided including SOI base wafer 1024, buried oxide (BOX) layer 1022, silicon layer 1020 and CMOS circuitry. A silicon device layer 1018 is joined to the SOI substrate and epitaxial layer 1016 is grown on seed crystals integrated with the silicon device layer 1018. Planarizing material in the plane of the device layer 1018 is illustrated.

[0089] Subsequent device layers and epitaxial layers are illustrated making up the multilayer structure. These layers are formed through repeating the template assisted bonding process with additional templates having seed material, epitaxial material, or the like. For example, template wafers with seed material 1014 and 1012 can be bonded sequentially. Etched openings in the template wafer provide access for selective area growth of epitaxial structures. Vias and interconnects may also be formed between and within the layers. Additional electronic devices or circuits may also be formed on the template wafers in the stack.

[0090] Thus, multilayer structures are fabricated using the seed crystal approach described herein. As illustrated in FIG. 10, multiple levels of electronics (e.g., CMOS circuits) are fabricated in the silicon device layers that are separated from the various assembly wafers as the structure is built up layer by layer. Although growth of III-Vs on silicon is illustrated, other embodiments utilize other material systems such as GaN on Sapphire and other lattice mismatched structures. In an embodiment, the growth of the final III-V epitaxial material is

performed on seed crystals regions on SOI wafer. One of ordinary skill in the art would recognize many variations, modifications, and alternatives.

[0091] FIGS. 11A - 11C are simplified schematic diagrams illustrating a process for vertically integrating CMOS devices using a template assisted bonding process according to an embodiment of the present invention. As illustrated in FIGS. 11A - 11C, the method of vertically integrating CMOS devices utilizes the template assisted bonding approach described herein, with the CMOS devices formed in the device layer of the assembly wafer. Thus, embodiments of the present invention extend the Template Assisted Bonding process to include the integration of III-V devices via bonding using an assembly substrate or wafer, but an assembly wafer into which CMOS devices have been integrated. As described herein, the CMOS devices are integrated into the assembly substrate by a process in which the assembly substrate or wafer is processed utilizing processes associated with CMOS processing. At a predetermined stage of the CMOS process, the process is stopped and III-V devices are bonded to the fully or partially processed assembly substrate including CMOS devices. Referring to FIG. 11A, a silicon-based substrate (i.e., an assembly substrate 1100) including a base layer 1110 is processed to form a plurality of CMOS devices in a device layer 1112. Thus, according to embodiments of the present invention, in addition to CMOS devices that can be implemented on the SOI substrate, a variety of CMOS devices can be implemented on the assembly substrate in addition to, in place of, or in combination with CMOS devices implemented on the SOI substrate. It will be appreciated that CMOS devices can be fabricated on the SOI substrate only, the assembly substrate only, or on both the SOI substrate and the assembly substrate. The ability to integrate devices on the assembly substrate enables the fabrication of CMOS devices that it may not be possible to implement on the SOI substrate. One of ordinary skill in the art would recognize many variations, modifications, and alternatives. Examples of the CMOS devices that can be fabricated include a variety of CMOS circuits including transistor-based devices such as amplifiers that can be used to drive photonic elements associated with the III-V devices, CMOS electronics, and the like.

[0092] Referring to FIG. 11A, the III-V device matrix 1120 that is bonded to the assembly wafer can include III-V devices that are bonded to portions of the CMOS devices, disposed between the various CMOS devices that are fabricated on the assembly substrate, driven by the CMOS devices and circuits, combinations thereof, or the like. As illustrated in FIG. 11A, the SOI substrate 1130 and the assembly substrate are prepared, using techniques described, for example, in relation to processes 220 and 230 in FIG. 2. It should be noted that the III-V

device matrix can include a variety of device types from unprocessed epitaxial material to finished devices as well as the range in between these types.

[0093] As described in relation to process 230 in FIG. 2, the SOI substrate can be processed to include a variety of devices and elements including CMOS devices (not shown). These can include optical structures, integrated circuits, microprocessors, memory, and the like. In some embodiments, recessed regions are formed on the processed SOI substrate (also referred to as a device wafer), but this is not required by the present invention.

[0094] Referring to FIG. 11B, the SOI substrate and the assembly substrate including the CMOS devices and the bonded III-V device matrix is aligned and bonded. The template assisted bonding process described herein thus provides a device layer of the assembly substrate that includes CMOS devices in which the assembly substrate is bonded to the SOI substrate.

[0095] Referring to FIG. 11C, portions of the assembly substrate, for example, portions of the template or assembly substrate (e.g., the base layer 1110 or backside of the substrate) can be removed to expose the device layer 1112 of the assembly substrate 1100. A variety of material removal techniques can be utilized, including CMP processes, etching, or the like. As illustrated in FIG. 11C, the CMOS devices are present in the device layer after the removal process and are vertically integrated with the device layer as well as with the elements fabricated in the SOI substrate, which can include photonic devices. After removal of the desired portions of the assembly substrate, metallization for interconnects and other post-processing steps, including CMOS processing steps such as implantation, etching, deposition, planarization, combinations thereof, or the like, can be performed as appropriate to the particular application. One of ordinary skill in the art would recognize many variations, modifications, and alternatives.

[0096] In addition to modification of FIG. 2 to incorporate the vertical integration of CMOS devices as part of the template assisted bonding process, other processes described herein can be modified to provide an assembly substrate with CMOS devices. As an example, processes described in relation to FIG. 6 can be modified to utilize an assembly substrate with CMOS devices fabricated thereon. In this example, process 620 can be modified to fabricate an assembly substrate with CMOS devices to which the device elements are attached in order to provide a process in which the unprocessed dies are attached to the pedestals after pedestal formation. Alternatively, in a process in which the pedestals are formed after die attachment, an additional step between process 622 and 640 would be added

to form the pedestals prior to bonding to the SOI substrate (642). Moreover, modification of processes illustrated in FIG. 8 can be performed to utilize an assembly substrate including a device layer in which CMOS devices have been fabricated. As an example, process 820 can be modified to prepare an assembly substrate including CMOS devices in which the assembly substrate has pedestals to which the seed material dies are mounted or attached. In this example, all or portions of the pedestals can be removed along with other features including source roughness in process 846. One of ordinary skill in the art would recognize many variations, modifications, and alternatives.

[0097] FIG. 12 is a simplified flowchart illustrating a method of vertically integrating CMOS devices using a template assisted bonding process according to an embodiment of the present invention. The method includes processing a III-V substrate to form III-V devices (1210), such as lasers, optical gain media, detectors, modulators, optical elements, or the like. In addition to the formation of III-V devices other materials can be processed to form magnetic device elements for devices such as optical circulators or isolators, other optoelectronic elements, and the like. After device processing, the III-V substrate can be lapped to form a uniform thickness and diced to provide III-V dies (1212). Lapping is not required.

[0098] The method also includes preparing an assembly substrate (1220). In an embodiment, a silicon substrate is oxidized, implanted, and patterned to provide mounting locations for the III-V dies discussed above as well as processed to form one or more CMOS devices. The assembly substrate in this embodiment includes a base region and a device region separated by a split plane defined by the peak of the implant dose (e.g., formed during a hydrogen implantation process). The patterning process can include definition of metal patterns on the template wafer that define locations where the semiconductor pieces (e.g., III-V semiconductor devices) are bonded. In some embodiments, in addition to or in place of metal patterns, targets are formed during the patterning process to provide an indication of locations at which the semiconductor pieces (e.g., III-V semiconductor devices) are directly bonded.

[0099] One or more CMOS devices can be fabricated on the assembly or template substrate, providing for electronic functionality that can be utilized in conjunction with the III-V dies provided in process 1212 and mounted on the assembly substrate in process 1222. Thus, the III-V devices can interact with CMOS electronics that are fabricated on the assembly substrate, particularly the CMOS device layer of the assembly substrate. As described more fully throughout the present specification, the device region, which can

include the CMOS devices, is bonded to the processed SOI substrate and used for device fabrication and the base region is removed and potentially reused.

[0100] In an embodiment, an SOI substrate is processed (1230) to provide CMOS devices, electronics, photonic elements, and the like. In some embodiments, the SOI substrate does not receive this processing since these devices and elements, including CMOS devices, are fabricated on the template substrate. The SOI substrate is prepared for wafer bonding operations including surface preparation (1232). The assembly substrate and the SOI substrate are aligned (1240) and a wafer bonding process is performed to join the two substrates and form a composite substrate structure (1242).

[0101] An anneal process is then used to split the assembly substrate at the depth at which the peak of the implant dose lies (1244). In some embodiments, this step is omitted since the assembly substrate splits as a result of the wafer bonding process (1242). In some embodiments, the substrate after splitting is polished (1246) to remove surface roughness resulting from the splitting process. Subsequent processing can also be performed to pattern optical waveguides in the device layer of the assembly substrate (1248) and to form electrical interconnects (1250). The bonds between the bond pads, the SOI substrate, and the III-V dies, as well as the bonds between the III-V dies and the SOI substrate can be metal-assisted bonds, semiconductor-semiconductor bonds, or the like, as described herein.

[0102] Although the assembly substrate can be split at or near the depth of the implant dose peak, embodiments of the present invention are not limited to this particular split depth and other depths other than the peak of the implant dose can be achieved. Also, it should be noted that while splitting using an anneal process is described herein as a method of removing the assembly substrate, other methods are included within the scope of the present invention, for example, without limitation, lapping to remove the bulk of the assembly substrate, or other suitable techniques.

[0103] It should be appreciated that the specific steps illustrated in FIG. 12 provide a particular method of vertically integrating CMOS devices using a template assisted bonding process according to an embodiment of the present invention. Other sequences of steps may also be performed according to alternative embodiments. For example, alternative embodiments of the present invention may perform the steps outlined above in a different order. Moreover, the individual steps illustrated in FIG. 12 may include multiple sub-steps that may be performed in various sequences as appropriate to the individual step. Furthermore, additional steps may be added or removed depending on the particular

applications. One of ordinary skill in the art would recognize many variations, modifications, and alternatives.

[0104] According to an embodiment of the present invention, a method of fabricating a composite semiconductor structure is provided as illustrated in FIG. 13. The method includes providing an SOI substrate including a plurality of silicon-based devices (1310), providing a compound semiconductor substrate (e.g., a III-V wafer or a II-VI wafer) including a plurality of photonic devices (1312), and dicing the compound semiconductor substrate to provide a plurality of photonic dies (1314). Each die includes one or more of the plurality of photonics devices. As an example, the plurality of silicon-based devices can include CMOS devices fabricated on the SOI substrate. Additionally, the plurality of silicon-based devices can include at least one of a detector, a CCD, logic circuits, emitter coupled logic circuits, BiCMOS circuits, SiGe BiCMOS circuits, NMOS circuits, PMOS circuits, or other silicon-based devices or circuits.

[0105] As an example, the plurality of photonic devices can include lasers, detectors, modulators, or the like. Additionally, the compound semiconductor substrate can include electronic devices such as HBTs, HEMTs, or FETs. The plurality of photonic devices can include a variety of devices including imaging optics, magnetic materials, birefringent materials, or non-linear optical materials.

[0106] The method also includes providing an assembly substrate having a base layer and a device layer including a plurality of CMOS devices (1316). The plurality of CMOS devices can include a variety of electronic circuits including silicon-based CMOS devices or silicon/germanium CMOS devices. These CMOS devices can include detectors, elements useful for a CCD, logic circuits, emitter coupled logic circuits, BiCMOS circuits, NMOS circuits, PMOS circuits, or the like.

[0107] Fabrication of the assembly substrate can include oxidizing a silicon substrate, implanting the oxidized silicon substrate to form an implant region, and patterning the implanted substrate to form the predetermined portions. As an example, implanting the oxidized silicon substrate can include implanting at least one of hydrogen or helium.

[0108] The method further includes mounting the plurality of photonic dies on predetermined portions of the assembly substrate (1318), aligning the SOI substrate and the assembly substrate (1320), joining the SOI substrate and the assembly substrate to form a composite substrate structure (1322), and removing at least the base layer of the assembly substrate from the composite substrate structure (1324). In an embodiment, the

predetermined portions of the assembly substrate on which the plurality of photonic dies are mounted is the device layer that includes the plurality of CMOS devices. Additionally, removing at least the base layer of the assembly substrate can include annealing the composite substrate structure to split the assembly substrate at the implant region. Alternatively, removing at least the base layer of the assembly substrate can include lapping a portion of the assembly substrate.

[0109] It should be appreciated that the specific steps illustrated in FIG. 13 provide a particular method of fabricating a composite semiconductor structure according to an embodiment of the present invention. Other sequences of steps may also be performed according to alternative embodiments. For example, alternative embodiments of the present invention may perform the steps outlined above in a different order. Moreover, the individual steps illustrated in FIG. 13 may include multiple sub-steps that may be performed in various sequences as appropriate to the individual step. Furthermore, additional steps may be added or removed depending on the particular applications. One of ordinary skill in the art would recognize many variations, modifications, and alternatives.

[0110] According to another embodiment of the present invention, a method of growing a compound semiconductor structure on a silicon-based substrate is provided is provided as illustrated in FIG. 14. The method includes providing an SOI base wafer having a bonding surface (1410), providing a seed wafer (e.g., a III-V or II-VI wafer) (1412), and dicing the seed wafer to provide a plurality of seed dies (1414). The SOI base wafer can include doped regions associated with transistors, which can be fabricated using CMOS processes.

[0111] The method also includes providing a template wafer including a plurality of CMOS devices (1416), mounting the plurality of seed dies on the template wafer (1418), and bonding the template wafer to the SOI base wafer (1420). The plurality of seed dies are joined to the bonding surface of the SOI base wafer. The plurality of CMOS devices can include silicon-based CMOS devices, silicon/germanium CMOS devices, or the like. As an example of the variety of CMOS devices included within the scope of the present invention, the CMOS devices can include detectors, CCDs, logic circuits, emitter coupled logic circuits, BiCMOS circuits, NMOS circuits, PMOS circuits, or the like. Mounting the plurality of seed dies on the template wafer can include mounting the plurality of seed dies on predetermined regions of the template wafer.

[0112] Providing the template wafer can include oxidizing a silicon substrate, implanting a dopant into the oxidized silicon substrate to form an implant region, and patterning the

implanted substrate to form the predetermined portions. As an example, the implant region can be positioned in a range from about 0.1 μm to about 5 μm from a surface of the template wafer. Bonding the template wafer to the SOI base wafer can forming at least one of a semiconductor-semiconductor bond or a metal assisted semiconductor-semiconductor bond. As an example, a metal assisted semiconductor bond could include one or more layers of In_xPd_y, for example, $In_{0.7}Pd_{0.3}$. Additional description related to metal assisted semiconductor-semiconductor bonds is provided in U.S. Patent Application No. 12/902,621, filed on October 12, 2010, the disclosure of which is hereby incorporated by reference in its entirety for all purposes. The use of In_xPd_y materials is not limited to the devices discussed in relation to FIG. 14 and can be used in conjunction with other devices as described throughout the present specification.

[0113] The method further includes removing at least a portion of the template wafer to expose at least a portion of a surface of the plurality of seed dies (1422), and growing the compound semiconductor structure on the exposed seed dies (1424), for example by performing an epitaxial growth process. As an example, removing at least a portion of the template wafer can include annealing the bonded template wafer and SOI base wafer and splitting the template wafer at the implant region. The plurality of CMOS devices can remain bonded to the SOI base wafer in some embodiments. Additionally, some embodiments perform a CMP process after splitting the template wafer.

[0114] Exposing at least a portion of a surface of the plurality of seed dies can include patterning and etching portions of the template wafer. In some embodiments, the method also includes fabricating gate metals or fabricating transistor interconnects after growing the compound semiconductor structure.

[0115] It should be appreciated that the specific steps illustrated in FIG. 14 provide a particular method of growing a compound semiconductor structure on a silicon-based substrate according to an embodiment of the present invention. Other sequences of steps may also be performed according to alternative embodiments. For example, alternative embodiments of the present invention may perform the steps outlined above in a different order. Moreover, the individual steps illustrated in FIG. 14 may include multiple sub-steps that may be performed in various sequences as appropriate to the individual step. Furthermore, additional steps may be added or removed depending on the particular applications. One of ordinary skill in the art would recognize many variations, modifications, and alternatives.

[0116] It should be noted that III-V devices discussed herein may have other than photonic functions. For example, embodiments of the present invention can be used to bond III-V materials for high-speed devices such as cell phone power amplifiers onto a silicon or SOI wafer with other functions. Other non-photonic applications are included within the scope of the present invention as well.

[0117] It is also understood that the examples and embodiments described herein are for illustrative purposes only and that various modifications or changes in light thereof will be suggested to persons skilled in the art and are to be included within the spirit and purview of this application and scope of the appended claims.

WHAT IS CLAIMED IS:

1. A method of fabricating a composite semiconductor structure, the method comprising:

providing an SOI substrate including a plurality of silicon-based devices;

providing a compound semiconductor substrate including a plurality of photonic devices;

dicing the compound semiconductor substrate to provide a plurality of photonic dies, each die including one or more of the plurality of photonics devices;

providing an assembly substrate having a base layer and a device layer including a plurality of CMOS devices;

mounting the plurality of photonic dies on predetermined portions of the assembly substrate;

aligning the SOI substrate and the assembly substrate;

joining the SOI substrate and the assembly substrate to form a composite substrate structure; and

removing at least the base layer of the assembly substrate from the composite substrate structure.

2. The method of claim 1 wherein the plurality of silicon-based devices comprise CMOS devices.

3. The method of claim 1 wherein the plurality of silicon-based devices comprise at least one of a detector, a CCD, logic circuits, emitter coupled logic circuits, BiCMOS circuits, NMOS circuits, PMOS circuits, or other silicon-based devices or circuits.

4. The method of claim 1 wherein the compound semiconductor substrate comprises a III-V wafer.

5. The method of claim 1 wherein the compound semiconductor substrate comprises a II-VI wafer.

6. The method of claim 1 wherein the plurality of photonic devices include at least one of a laser, a detector, or a modulator.

7. The method of claim 1 wherein the compound semiconductor substrate further includes electronic devices.

8. The method of claim 7 wherein the electronic devices include at least one of HBTs, HEMTs, or FETs.

9. The method of claim 6 wherein the plurality of photonic devices further include at least one of imaging optics, magnetic materials, birefringent materials, or non-linear optical materials.

10. The method of claim 1 wherein the plurality of CMOS devices comprise silicon-based CMOS devices.

11. The method of claim 1 wherein the plurality of CMOS devices comprise silicon/germanium CMOS devices.

12. The method of claim 1 wherein the plurality of CMOS devices comprise at least one of a detector, a CCD, logic circuits, emitter coupled logic circuits, BiCMOS circuits, SiGe BiCMOS circuits, NMOS circuits, or PMOS circuits.

13. The method of claim 1 wherein providing the assembly substrate comprises:

oxidizing a silicon substrate;

implanting the oxidized silicon substrate to form an implant region; and

patterning the implanted substrate to form the predetermined portions.

14. The method of claim 13 wherein implanting the oxidized silicon substrate comprises implanting at least one of hydrogen or helium.

15. The method of claim 13 wherein removing at least the base layer of the assembly substrate comprises annealing the composite substrate structure to split the assembly substrate at the implant region.

16. The method of claim 13 wherein removing at least the base layer of the assembly substrate comprises lapping a portion of the assembly substrate.

17. A method of growing a compound semiconductor structure on a silicon-based substrate, the method comprising:

providing an SOI base wafer having a bonding surface;

providing a seed wafer;

dicing the seed wafer to provide a plurality of seed dies;

providing a template wafer including a plurality of CMOS devices;

mounting the plurality of seed dies on the template wafer;

bonding the template wafer to the SOI base wafer, wherein the plurality of seed dies are joined to the bonding surface of the SOI base wafer;

removing at least a portion of the template wafer;

exposing at least a portion of a surface of the plurality of seed dies; and

growing the compound semiconductor structure on the exposed seed dies.

18. The method of claim 17 wherein growing the compound semiconductor structure comprises performing an epitaxial growth process.

19. The method of claim 17 wherein the SOI base wafer comprises doped regions associated with transistors.

20. The method of claim 17 wherein the seed wafer comprises a III-V wafer.

21. The method of claim 17 wherein mounting the plurality of seed dies on the template wafer comprises mounting the plurality of seed dies on predetermined regions of the template wafer.

22. The method of claim 17 wherein providing the template wafer comprises:

oxidizing a silicon substrate;

implanting a dopant into the oxidized silicon substrate to form an implant region; and

patterning the implanted substrate to form the predetermined portions.

23. The method of claim 22 wherein the implant region ranges from about 0.1 μm to about 5 μm from a surface of the template wafer.

24. The method of claim 23 wherein removing at least a portion of the template wafer comprises:

annealing the bonded template wafer and SOI base wafer; and

splitting the template wafer at the implant region, wherein the plurality of CMOS devices remain bonded to the SOI base wafer.

25. The method of claim 24 further comprising performing a CMP process after splitting the template wafer.

26. The method of claim 17 further comprising at least one of fabricating gate metals or fabricating transistor interconnects after growing the compound semiconductor structure.

27. The method of claim 17 wherein exposing at least a portion of a surface of the plurality of seed dies comprises patterning and etching portions of the template wafer.

28. The method of claim 17 wherein bonding the template wafer to the SOI base wafer comprises forming at least one of a semiconductor-semiconductor bond or a metal assisted semiconductor bond.

29. The method of claim 28 wherein the metal assisted semiconductor bond comprises InPd.

30. The method of claim 17 wherein the plurality of CMOS devices comprise silicon-based CMOS devices.

31. The method of claim 17 wherein the plurality of CMOS devices comprise silicon/germanium CMOS devices.

32. The method of claim 17 wherein the plurality of CMOS devices comprise at least one of a detector, a CCD, logic circuits, emitter coupled logic circuits, BiCMOS circuits, NMOS circuits, or PMOS circuits.