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MEMORIES AND THE TESTING THEREOF

DESCRIPTION

The present invention relates to memories and the testing thereof and seeks to provide an efficient test for address line failures in a large scale storage system of an information handling system and equally a storage system having such a test built into it.

It is normally regarded as necessary to test all aspects of the memory section of a data processing system as part of an IPL operation and at other times and thus what is thought to be an adequate test is built into the system - into the memory sub-system itself or into some other part of the system, say, into a service processor or diagnostic unit. The exact nature of the testing depends on the nature of the memory configuration but should cover both the retention capabilities of the storage locations and the functionality of the addressing mechanism. Conventional testing involves comprehensively exercising all aspects of the memory at the same time and, for a large memory, this can prevent the memory, and hence the system, from being available for processing for some appreciable length of time. An additional problem is encountered when the memory is provided with error correcting and avoidance mechanisms in that these operate on data and can mask other malfunction.

The present invention separates addressing mechanism testing from other aspects of testing the memory and provides a system operated memory test comprising testing address lines independently of other memory aspects by systematically testing one memory location per address line relative to a datum location, where the address of the location associated with a particular address line is that of the datum location but with the bit of the particular address line inverted, by writing a

data pattern into the datum location and a divergent, preferably the inverted form, data pattern into the address line associated location, reading out the two patterns with the error mechanisms, if any, disabled and comparing the two accessed patterns, the procedure being repeated with the patterns reversed.

Theoretically, it does not matter which order is followed though the method described hereinafter is thought to be the most reliable.

As to the test data pattern, it is pointed out that with double bit correction provided by the error correcting code logic in a card organised memory, a number of bits can be corrected on a card or a larger number of bits can be corrected on a card pair, where the larger number of bits is somewhat less than double the number of bits which can be corrected on a single card. The address test in accordance with the present invention then produces a pattern that will create a difference greater than that larger number of bits between the data stored in a storage location under test and any address that could be accessed by an address line failure. The test predicts the effect of an address line failure external to the array modules and internal to a card pair and then tests to see if a failure has occurred. The address test does not declare an address failure until a predetermined number of bit failures on a card is found. The test is valid for single and multiple address line failures. Since only one address bit is changed for each path through the test other failing address lines will not be detected until the path with those failing address bits are tested. Thus, even with multiple address line failure the two addresses that are stored to and fetched from are the only one address bit apart.

The present invention also provides a memory system and equally a data processing system having such a test built into it.

U.S. Patent 4,369,511 describes a semi-conductor memory test system which reads a memory under test at an address generated by a pattern

generator and compares data read data from the address with expected data. A block mask memory is read by a portion of the address and the comparing operation of the comparator is inhibited by block mask data read from the block mask memory.

The method for memory testing according to the patent is significantly different from the present invention in that the patent requires a comparison of data read from a memory with data generated and fed through a test memory 22 and compared in comparator 19.

In the method according to the present invention, data is stored in associated locations, whose address lines differ by one inverted bit, and from which the data is read and compared. There is no second memory used to generate an expected storage pattern as in the prior art.

U.S. Patent 4,404,519 provides method and apparatus for testing data stored in a memory array embedded in a large scale integrated circuit. The method and apparatus of the patent do not describe or suggest the method for testing address lines in accordance with the present invention.

U.S. Patent 4,429,389 teaches a test pattern address generator which generates specialised address patterns in which an address generator is complimented and then incremented on a series of increment-compliment actions so that all combinations of row and column drivers in the integrated circuit memory under test are exercised.

The patent does not contemplate the method of testing address lines in accordance with the present invention where each address line bit is separately tested by a two-pass test in which divergent data is stored into the address under test and the address into which data would be stored if there was an address line failure for the address bit under test.

U.S. Patent 4,559,626 teaches a test apparatus for testing memories which includes an internal memory into which data patterns are stored for comparison with data patterns stored in a memory under test. The patterns are then read from the internal memory of the tester and the memory under test and compared.

The patent does not contemplate the method of testing address lines in accordance with the present invention where each address line bit is separately tested by a two-pass test in which divergent data is stored into the address under test and the address into which data would be stored if there was an address line failure for the address bit under test.

The test of the present invention is a simple and efficient method which provides unique failure information for any address bit failure in the memory system.

The present invention will be described further by way of example with reference to an embodiment thereof as illustrated in the accompanying drawings in which:

Fig. 1 is a simplified block diagram of a system including a memory which could support the test method according to the present invention;

Fig. 2 is a logic block diagram of the data flow including address information of a memory card which may be tested by the method according to the present invention;

Fig. 3 is a schematic diagram of an address bus structure which could be used with a preferred embodiment of the present invention; and

Fig. 4 is a flow diagram of the preferred testing method

of the present invention.

In information handling systems including processors and memory systems as shown in Fig. 1, there is a need to adequately test the address lines in the memory system to ensure that the addressing of the memory arrays is correct. Fig. 1 is a simple block diagram that shows processor 10 which is connected to storage system 12 by data, address,error and control lines 14.

It should be understood that the processor 10 and storage system 12 may be implemented in many ways by systems that are currently available from many hardware suppliers such as IBM Corporation. For example, the processor could be an IBM system 370 processor with its own internal storage system, or an IBM 3880 Model 23 with cache storage system 12 or storage sub-system such as might be used to control direct access storage devices (DASD).

In the prior art memory address test methods, unique data such as an incrementing pattern or the address is stored in each memory location starting at the lowest address and ending with the highest address. Each location is then read and compared to ensure that the location has not been overlayed by a write to any other location. The same pattern (or the inverse) is then written starting at the highest address and descending to the lowest. The data is again read and compared to ensure that the data has not been over written by a write to any other location. Failures of address lines are detected either by a parity check or by a comparison of a data pattern read from the array not matching the expected data pattern. This method for testing for address line failures will also detect a large portion of data failures in an array. Several of the prior art patents identified above use this kind of memory testing.

With the type of testing as described above, the time required to test a large memory (such as 256 megabytes) is very prohibitive. For

example, the projected time required to test a 256 megabyte storage system will be 1 hour 48 minutes and 32 seconds. The method of the present invention is to remove as much dependency on the data as possible when testing the address lines. With this method, the testing of the address lines can be accomplished in as little as one second. Upon successful completion of the addressing test, a separate data test must be performed, but such a data test can be run concurrently with normal system operation.

Referring now to Fig. 2, a typical memory card 16 will be described in which the address lines between the buffers 20, 22, and 24 and the memory arrays 26 a, b, c, and d, are tested. Card 16 also includes a set of bi-directional drivers 28 for handling the transmission of data on and off the card. Control lines are connected as inputs to control block 18 which controls the read, write, enable, test, card select and addressing of the arrays 26 a, b, c, d inclusive on card 16.

The discussion above with respect to the hardware environment, specifically the description with respect to Figs. 1 and 2 is for the purpose of indicating a typical system in which the method according to the present invention might be efficiently employed.

Fig. 3 shows a typical address bus structure for a large memory sub-system might include 24 bits wherein 20 bits address locations unique to each card and 4 bits provide card select. Thus, there would be a possibility of 16 cards each card having one million addressable locations.

The address bus structure of Fig. 3 is shown merely for illustration of a typical addressing scheme for a large scale memory and is not intended to in any way limit the application of the present invention.

The method of the present invention is to be described more fully with respect to a preferred embodiment thereof which is shown in the flow chart of Fig. 4.

When an address line test is to be performed, an appropriate request is sent to the memory control processor 10 in the memory subsystem. The control processor 10 then begins the address test by setting a first bit in the address to a one as the active address line. A first data pattern such as an all zeros data pattern is then stored into that active address line position.

At each step of the process, normal hardware error checks such as parity are being performed to ensure that other failures unrelated to the address test do not occur which could mask the address test being performed. Next, a different data pattern having a maximum pattern separation from the first pattern is stored into the inactive address line position for the bit address bit under test.

For example, an all ones pattern might be stored into address zero where the active address line position and the bit under test is the low order bit of the address.

With reference to Fig. 3, the structure of the address on the address bus, the low order address bit position would be identified as bit 23. Thus, with bit 23 on, the active address line position would be address 1 and the inactive address line position would be address 0. Again as before, the normal hardware error correction is performed. At any step in this process if there is an error indicated from the hardware error checking the test ends with an isolation code indicating the cause of the error is generated.

Next, all error correction circuitry is disabled in the memory system and the data stored into the active and inactive address line positions

are then read and compared. The data are compared bit by bit and the total number of data bits in error is determined.

A predetermined number of acceptable data bit errors is set that the system can detect and correct. If the number of data bits in any particular compare exceeds that number, an address line failure is indicated and the test is ended with an appropriate error code. In a preferred embodiment of the present invention, six errors per card may be accepted before address line failure is indicated.

If all address lines have not been tested, the test then increments to the next bit in the address as the active line and the above steps are repeated. These steps are repeated until all of the address bits in the storage address have been tested for a particular card. It should be noted, that when a next card is to be tested, there will be a change in the card select bits which are at the high order at the address and each of the 20 low order address bits must be again tested as above for each card in the system.

After the first pass is completed through all address lines in the system, a second pass is then conducted in which the active address line is again set to the low order address bit and the second data pattern such as all zeros is stored into the inactive address line position address zero and the data pattern that was stored into the inactive address line position for the first pass is now stored into the active address line position such as storing all ones in address one. Again, as before, the low order address bit referred to is bit 23 as shown in Fig. 3. Also, as before, hardware error checks such as parity are active to ensure that no unrelated error masks the errors which may occur as a result of the test being conducted.

As with the first pass, the data stored in the two addresses are then read and compared bit by bit and the number of error bits are counted to determine if the predetermined number of acceptable and correctable

errors has been exceeded. If such number of error bits has been exceeded, the test is ended indicating an address line failure error code.

If all address lines have not been tested for the second pass the next address bit is then made the active address bit position and the second pass is conducted for such next bit position in the address.

The steps are repeated for the second pass until all address bits in the address have been completely tested. It should be noted that the card select bits at the high end of the address must be independently exercised in that each card must be separately tested for all active address lines on that card such that the twenty lines of address will be tested independently and separately for each card selected.

As was commented upon earlier, the above sequence is the one preferred but is not the only one, theory requiring the action to be completed. The above sequence give an address line failure indication virtually immediately so that the test could be halted, but the total test time is small enough for this not to be essential. It could be arranged that each location used could have its comparison performed with one order of the patterns before any comparison is performed with the patterns reversed. This could mean that the datum location only needed writing twice, one for each order of the patterns.

It should be further noted that the card select lines at the high end of the address, and, obviously, these could be module or sub-unit select lines depending on the memory structure, should be verified by separate select test prior to the address line test which is the subject of the present invention.

It should also be noted that the number of acceptable data bit errors is dependent on the error correction capability of the storage system and the number of spare memory locations per card/module/sub-unit, as

described, the number of spare chips on each memory card. For example, if double bit correction is provided by a storage system, and each memory card has one spare chip and one bit is read from each chip, then the number of acceptable data errors is three.

Trivially, the address line test of the present invention is only valid on storage systems in which each address line partially selects more memory locations than the number of acceptable data bit errors as discussed above.

While the invention has been particularly shown and described with reference to a preferred embodiment thereof, it will be understood by those skilled in the art that various changes in the form and detail may be made therein without departing from the scope of the appended claims.

CLAIMS

1. A system operated memory test comprising testing address lines independently of other memory aspects by systematically testing one memory location per address line relative to a datum location, where the address of the location associated with a particular address line is that of the datum location but with the bit of the particular address line inverted, by writing a data pattern into the datum location and a divergent, preferably the inverted form, data pattern into the address line associated location, reading out the two patterns with the error mechanisms, if any, disabled and comparing the two accessed patterns, the procedure being repeated with the patterns reversed.

2. A test as claimed in claim 1, comprising the steps of:

writing a first bit pattern into a first memory word at an address formed with a bit under test on;

writing a second bit pattern into a second memory word at an address formed with a bit under test off;

reading data from both of the addresses;

checking for a predetermined number of bit errors which constitute a permanent error;

repeating the above steps for each bit in the address until all address lines have been tested;

writing the first data pattern to the second memory word at the address formed with the bit under test off;

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writing the second data pattern to the first memory word at the address formed with the bit under test on;

reading data from both of the addresses;

checking for a predetermined number of bit errors which constitute a permanent error; and

repeating the above steps for each bit in the address until all address lines have been tested.

3. A test as claimed in claim 2, wherein the first bit pattern is an all zeros pattern and the second bit pattern is an all ones pattern.

4. A test as claimed in claim 2, where the memory is a multi-card storage array and wherein the predetermined number of bit errors which constitute a permanent error is six errors for each card in the multi-card storage array.

5. A test as claimed in claim 4, further comprising the steps of:

selecting a memory card in said multicard storage array by setting one or more predetermined card select lines on; and

repeating each of the above steps for testing for address line failures separately for each card in said multicard storage array.

6. A memory system incorporating a test as claimed in any preceding claim.

7. A data processing system including a memory and incorporating a test as claimed in any preceding claim.

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8. A system as claimed in either claim 6 or claim 7, arranged to perform the test automatically on IPL.

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