Description

Title of Invention: CONTROL METHOD FOR DIRECT POWER CONVERTER~~CONVERSION DEVICE~~

Technical Field

[0001] The present invention relates to a method for controlling a direct power converter.

Background Art

[0002] Patent Documents 1 and 2 and Non-Patent Documents 1, 2 and 3 each describe a direct power converter. The direct power converter includes a diode rectifier, an inverter and a charge and discharge circuit.

[0003] A single-phase AC voltage is full-wave rectified by the diode rectifier, is thus output to a pair of DC power supply lines (a DC link).

[0004] The charge and discharge circuit is provided in the DC link and includes a buffer circuit and a boost circuit. The buffer circuit includes a switch and a capacitor connected in series with each other between the pair of DC power supply lines. The capacitor is discharged by conduction of the switch, thus providing power to the DC link.

[0005] The boost circuit boosts a rectified voltage from the diode rectifier to charge the capacitor. The charge and discharge circuit accordingly receives power from the DC link. The inverter receives a DC voltage of the DC link and converts it into an AC voltage to be output.

Prior Art Documents

Patent Documents

[0006] Patent Document 1: Japanese Patent Application Laid-Open No. 2011-193678

Patent Document 2: Japanese Patent Application Laid-Open No. 2012-135184

Non-Patent Documents

[0007] Non-Patent Document 1: Yoshiya Ohnuma, Jun-ichi Itoh, "Circuit Configuration and Control Strategy of single-to-three Phase Power Converter with Active Buffer and Charge Circuit", The 2010 Annual Meeting of the Institute of Electrical Engineers of Japan, No. 4-057 (2010)

Non-Patent Document 2: Yoshiya Ohnuma, Jun-ichi Itoh, "Experimental Verification of Single Phase to Three Phase Converter Using an Active Buffer circuit with a Charge Circuit", 2010 IEEJ Industry Applications Society Conference 1-124 (2010)

Non-Patent Document 3: Yoshiya Ohnuma, Jun-ichi Itoh, "Comparison of Boost Chopper and Active Buffer as Single to Three Phase Converter", The 2011 Annual Meeting of the Institute of Electrical Engineers of Japan, No. 4-042 (2011)

Summary of Invention

Problem to be Solved by the Invention

[0008] Unfortunately, the charge and discharge circuits proposed in these documents require high power capacity to compensate for the pulsating components of a single-phase AC voltage.

[0009] Typical electrolytic capacitors allow only a small ripple current, although they are inexpensive. Thus, the capacitor of the charge and discharge circuit proposed above is desirably, for example, a film capacitor or a laminated ceramic capacitor as in Non-Patent Document 3. From such a point of view, it is difficult to configure a charge and discharge circuit inexpensively.

[0010] ~~This application therefore has an object~~ Embodiments of the present application seek to provide a technique of reducing power provided/received between a charge and discharge circuit and a DC link to reduce

power capacity required for the charge and discharge circuit.

Means to Solve the Problem

[0011] ~~A method for controlling a direct power converter a~~According to an aspect of the present invention, there is provided ~~is~~ a method for controlling a direct power converter including: a first power supply line (LH); a second power supply line (LL) which is applied with a potential lower than that of the first power supply line is applied; a converter (3) including an input side connected with a single-phase AC power supply (1, 2) and an output side connected with the first power supply line and the second power supply line, and performing single-phase full-wave rectification; a charge and discharge circuit (4) located between the first power supply line and the second power supply line; and an inverter (5) that converts a DC voltage between the first power supply line and the second power supply line into an AC voltage.

[0012] In the direct power converter, the charge and discharge circuit includes: a buffer circuit (4a) including a capacitor (C4) and a first switch (Sc, D42) connected in series with the capacitor at a side close to the first power supply line between the first power supply line and the second power supply line, and providing and receiving power between the first power supply line and the second power supply line; and a boost circuit (4b) that boosts a rectified voltage (Vrec) from the converter (3) to charge the capacitor.

[0013] The buffer circuit (4a) provides power to the first power supply line and the second power supply line in a first period (T1) in which a cosine value ($\cos(2\omega t)$) to a value ($2\omega t$) of twice a phase angle (ωt) of an AC waveform output from the single-phase AC power supply (1, 2) is positive when the AC waveform is regarded as a sine value ($\sin(\omega t)$) of the phase angle (ωt); receives power from the first power supply line and the second power supply line in a second period (T2) in which the cosine value is negative.

[0014] The converter (3) is conductive at a rectifying duty (drec), where the rectifying

duty takes a value of $\sqrt{2}$ -times an absolute value ($|\sin(\omega t)|$) of the sine value in the first period.

[0015] ~~A first aspect of the control~~ The method determines power ($Vdc \cdot Idc$) input to the inverter (5) as a product of an absolute value ($Im/\sqrt{2}$) of an input current input to the converter (3) at a boundary between the first period and the second period, an effective value ($Vm/\sqrt{2}$) of an AC voltage (Vin) of the single-phase AC power supply, and a value ($(1-(1 - k)\cdot\cos(2\omega t))$) obtained by subtracting, from one, a value obtained by multiplying the cosine value ($\cos(2\omega t)$) by a positive constant (1 - k) less than one.

[0016] ~~In a second aspect of the method for controlling a direct power converter a~~According to an embodiment of the present invention~~, in the first aspect~~, the rectifying duty (drec) takes an inverse number ($1/(\sqrt{2}|\sin(\omega t)|)$) of the value of $\sqrt{2}$ -times the absolute value ($|\sin(\omega t)|$) of the sine value in the second period (T2). The first switch (Sc, D42) is rendered conductive to discharge the capacitor (C4) in the first period (T1) at a discharge duty (dc) taking a value obtained by dividing, by $\sqrt{2}$, a product of the cosine value ($\cos(2\omega t)$) and a value (Vm/Vc) obtained by dividing a crest value (Vm) of the AC voltage (Vin) of the single-phase AC power supply by a both-end voltage (Vc) of the capacitor.

[0017] ~~In a third aspect of the method for controlling a direct power converter a~~According to an embodiment of the present invention, ~~in the first aspect,~~ the rectifying duty (drec) takes a value 1 in the second period (T2). The first switch (Sc, D42) is rendered conductive to discharge the capacitor (C4) in the first period (T1) at a discharge duty (dc) taking a product of the cosine value ($\cos(2\omega t)$) and a value (Vm/Vc) obtained by dividing a crest value (Vm) of the AC voltage (Vin) of the single-phase AC power supply by a both-end voltage (Vc) of the capacitor.

[0018] For example, the boost circuit (4b) includes: a diode (D40) including an anode and a cathode that is connected between the first switch (Sc, D42) and the capacitor (C4);

a reactor (L4) connected between the first power supply line (LH) and the anode, through which a current input to the boost circuit flows; and a second switch (S1, D41) connected between the second power supply line (LL) and the anode.

[0019] In the second period (T2), the second switch of the boost circuit is controlled to control a current (il) flowing through the reactor (L4).

Effects of the Invention

[0020] According to the ~~first~~ aspect of the method for controlling a direct power converter of the present invention, the power provided/received by the buffer circuit ~~is~~may be reduced, thereby reducing a power capacity required for the buffer circuit.

[0021] ~~According to the second aspect of the method for controlling a direct power converter of the present invention, a~~An average value of a virtual DC voltage can be made constant in a period in which the inverter is capable of power conversion.

[0022] ~~According to the third aspect of the method for controlling a direct power converter of the present invention, a~~ A voltage utilization ratio can be improved.

[0023] The object, features~~, aspects~~ and advantages of the present invention will become more apparent from the following detailed description and the attached drawings.

Brief Description of Drawings

[0024] ~~[FIG. 1] A~~FIG. 1 is a block diagram showing the configuration of a direct power converter to which a control method described in an embodiment is applied~~.~~;

~~[FIG. 2] A~~FIG. 2 is a circuit diagram showing an equivalent circuit of a circuit shown in FIG. 1~~.~~;

~~[FIG. 3] A~~FIGS. 3 and 4 are graphs showing the operation of the direct power converter shown in FIG. 1 in first setting~~.~~;

~~[FIG. 4] A graph showing the operation of the direct power converter shown in~~

~~FIG. 1 in the first setting.~~

~~[FIG. 5] A~~FIGS. 5 and 6 are graphs showing the operation of the direct power converter shown in FIG. 1 in second setting~~.~~;

~~[FIG. 6] A graph showing the operation of the direct power converter shown in FIG. 1 in the second setting.~~

~~[FIG. 7] A~~FIG. 7 is a block diagram showing an example configuration for control on a DC current, which is described in the embodiment~~.~~;

~~[FIG. 8] A~~FIG. 8 is a graph showing the relationship among an input power, the electrostatic capacitance of a capacitor and a ripple current in the direct power converter~~.~~; and

~~[FIG. 9] A~~FIG. 9 is a circuit diagram showing a modification of the direct power converter shown in FIG. 1.

Description of Embodiments

[0025] A. Configuration of Direct Power Converter

FIG. 1 is a block diagram showing the configuration of a direct power converter to which a control method described in this embodiment is applied. The direct power converter includes a converter 3, a charge and discharge circuit 4 and an inverter 5.

[0026] The converter 3 is connected with a single-phase AC power supply 1 via, for example, a filter 2. The filter 2 includes a reactor L2 and a capacitor C2. The reactor L2 is provided between the converter 3 and one of two output terminals of the single-phase AC power supply 1. The capacitor C2 is provided between the two output terminals of the single-phase AC power supply 1. The filter 2 removes the high frequency components of a current. The filter 2 may be omitted. For the sake of brevity, the following description will be made ignoring the function of the filter 2.

[0027] The converter 3 uses a diode bridge, for example, and includes diodes D31 to

inverter and includes six diodes Dup, Dvp, Dwp, Dun, Dvn and Dwn.

[0036] The diodes Dup, Dvp, Dwp, Dun, Dvn and Dwn are disposed, with their cathodes toward the DC power supply line LH and their anodes toward the DC power supply line LL. The diode Dup is connected in parallel with the switching element Sup between the output terminal Pu and the DC power supply line LH. Similarly, the diodes Dvp, Dwp, Dun, Dvn and Dwn are respectively connected in parallel with the switching elements Svp, Swp, Sun, Svn and Swn.

[0037] For example, the switching elements Sup, Svp, Swp, Sun, Svn and Swn may use IGBTs.

[0038] An inductive load 6 is a rotating machine, for example, and is illustrated as an equivalent circuit indicative of an inductive load. Specifically, a reactor Lu and a resistor Ru are connected in series with each other, and one end of the series body is connected with the output terminal Pu. This holds true for a reactor Lv and a resistor Rv and for a reactor Lw and a resistor Rw. The other ends of the series bodies are connected with each other.

[0039] B. Control Method

(b-1) Basic Concept of Power Reduction

An instantaneous input power Pin input to the converter 3 is expressed by the following formula with an input power factor being one, where a crest value Vm and a power supply angular velocity ω of the single-phase AC voltage Vin, a crest value Im of the input current Iin, and a time t are introduced. A product ωt of the power supply angular velocity ω and the time t represents a phase angle of the single-phase AC voltage Vin. An AC waveform is regarded as the product of a sine value of the phase angle ωt of the AC waveform and a crest value.

[0040] ~~[Math 1]~~

$$Pin = Vm \cdot Im \cdot \sin^2(\omega t)$$
$$= \frac{1}{2} Vm \cdot Im - \frac{1}{2} Vm \cdot Im \cdot \cos(2\omega t) \quad \cdots \quad (1)$$

[0041] The second term of the right-hand side of the formula (1) represents power pulsations. In conventional techniques, to cancel out such power pulsations, the buffer circuit 4a provides and receives, between the DC power supply lines LH and LL therewith, the power that has the same value as that of the second term of the right-hand side of the formula (1) and has an opposite polarity. The power capacity of the charge and discharge circuit 4 therefore needs to be selected so as to be greater than or equal to the second term of the right-hand side of the formula (1).

[0042] Description will thus be made on which technique should be used for allowing to reduce the power (hereinafter referred to as "instantaneously provided/received power Pbuf") provided/received as described above in order to reduce the power capacity of the charge and discharge circuit 4.

[0043] Needless to say, setting the instantaneously provided/received power Pbuf to completely zero is not desirable because the power input to the inverter 5 pulsates with the second term of the right-hand side of the formula (1) and, in the first place, reducing the power capacity of the charge and discharge circuit 4 is not required. A positive constant k less than one is thus introduced (a value (1 - k) is accordingly also a positive constant less than one) to determine the instantaneously provided/received power Pbuf by the following formula. In other words, a characteristic approach for achieving such instantaneously provided/received power Pbuf will be described below.

[0044] ~~[Math 2]~~

$$Pbuf = \frac{1}{2} Vm \cdot Im \cdot \cos(2\omega t) \cdot k \cdots \quad (2)$$

[0045] That is to say, the instantaneously provided/received power Pbuf is represented

inductive load 6 via the inverter 5 when the output terminals Pu, Pv and Pw are connected in common to any one of the DC power supply lines LH and LL in the inverter 5, is equivalently expressed as a zero-phase current iz flowing through a switch Sz when the switch Sz is conductive. FIG. 2 also shows the reactor L4, the diode D40 and the switch Sl constituting the boost circuit 4b, and additionally shows a current il flowing through the reactor L4.

[0049] Duties drec, dc and dz at which the switches Srec, Sc and Sz are respectively conductive and a DC current Idc input to the inverter 5 are introduced in the equivalent circuit thus obtained, and accordingly, the following formula holds.

[0050] ~~[Math 3]~~

$$\begin{bmatrix} irec \\ icd \\ iz \end{bmatrix} = \begin{bmatrix} drec & 1 \\ dc & 0 \\ dz & 0 \end{bmatrix} \cdot \begin{bmatrix} Idc \\ il \end{bmatrix} \quad \cdots \quad (3)$$

[0051] The currents irec1, icd and iz are obtained by multiplying the DC current Idc respectively by the duties drec, dc and dz, and thus, these are respectively average values in the switching cycles of the switches Srec, Sc and Sz. The current il is also an average value in the switching cycle of the switch Sl.

[0052] The DC current Idc is the sum of the currents irec1, icd and iz flowing through~~conducted by~~ the respective switches Srec, Sc and Sz, and thus, the following equation holds, where $0 \leq drec1$, $0 \leq dc \leq 1$ and $0 \leq dz \leq 1$.

[0053] ~~[Math 4]~~

$$drec + dc + dz = 1 \quad \cdots \quad (4)$$

[0054] The duties drec, dc and dz are thus considered as current distribution ratios of the DC current Idc to the respective currents irec1, icd and iz. The duty drec is a duty at which a period, in which the converter 3 is connected with the DC power supply lines LH

and LL and allows a current to flow into the inverter 5, is set, and thus may be referred to as a rectifying duty drec below. The duty dc is a duty at which the capacitor C4 is discharged, and thus may be referred to as a discharge duty dc below. The duty dz is a duty at which the zero-phase current iz always flows in the inverter 5 irrespective of the voltage output by the inverter 5, and thus may be referred to as a zero duty dz below.

[0055] The inverter 5 cannot utilize a DC voltage between the DC power supply lines LH and LL in the period in which a zero-phase current iz flows. Of the DC voltage between the DC power supply lines LH and LL, thus, a virtual DC voltage (hereinafter referred to as a "virtual DC voltage") Vdc in a period in which the inverter 5 is capable of power conversion is conceivable as follows. The virtual DC voltage Vdc can be regarded as a voltage applied across the DC power supply lines LH and LL as an average of the maximum values of the voltages that can be output by the inverter 5, with respect to the cycle of controlling switching of the switches Sc and Sl and the inverter 5.

[0056] ~~[Math 5]~~

$$Vdc = Vrec \cdot drec + Vc \cdot dc + 0 \cdot dz$$
$$\text{where } Vrec = Vm \cdot |\sin(\omega t)| \qquad \cdots(5)$$

[0057] Hereinafter, a ratio R (= Vdc/Vm) of a virtual DC voltage Vdc to a crest value Vm is referred to as a voltage utilization ratio.

[0058] (b-2) First Setting of Duty for Maximizing Voltage Utilization Ratio R

According to the first document group, the rectifying duty drec and the discharge duty dc for maximizing the voltage utilization ratio R are each set in the providing period and the receiving period by the formulas (6) and (7), respectively. As suggested in Patent Document 1, however, this is the setting that maximizes a voltage utilization ratio R for the virtual DC voltage Vdc that is constant. The voltage utilization ratio R is $(1/\sqrt{2})$ in this case. In the receiving period, dc = 0, so that the switch Sc is not

conductive. In the providing period, the capacitor C4 is not charged, so that the current il does not flow.

[0059] ~~[Math 6]~~

$$\left.\begin{aligned} drec &= \sqrt{2}\,|\sin(\omega t)| \\ dc &= \frac{Vm}{vc}\cdot\frac{\cos(2\omega t)}{\sqrt{2}} \end{aligned}\right\} \quad \cdots \quad (6)$$

[0060] ~~[Math 7]~~

$$\left.\begin{aligned} drec &= \frac{1}{\sqrt{2}\,|\sin(\omega t)|} \\ dc &= 0 \end{aligned}\right\} \quad \cdots \quad (7)$$

[0061] In the "first setting", the DC current Idc input to the inverter 5 is caused to pulsate with the voltage utilization ratio R above kept, that is, the duties of the formulas (6) and (7) kept, thus obtaining an instantaneously provided/received power Pbuf that satisfies the formula (2).

[0062] Specifically, the DC current Idc that satisfies the following formula is caused to be input to the inverter 5. The control of the converter 5 for satisfying the following formula can be achieved by controlling a current command value. The control of the current command value will be described below.

[0063] ~~[Math 8]~~

$$Idc = \frac{Vm\cdot Im}{2Vdc}(1-(1-k)\cdot\cos(2\omega t)) \quad \cdots \quad (8)$$

[0064] In the providing period, the current il is set to zero as described above, so the current irec is equal to the current irec1, and the current irec is equal to the product drec·idc. The following formula therefore holds, where Vm/Vdc = $\sqrt{2}$ is adopted in view of the voltage utilization ratio R.

[0065] ~~[Math 9]~~

$$irec = irecl = drec \cdot Idc$$
$$= \sqrt{2}\left|\sin(\omega t)\right| \cdot \frac{Vm}{2Vdc} \cdot Im(1-(1-k)\cdot\cos(2\omega t))$$
$$= Im\left|\sin(\omega t)\right| \cdot (1-(1-k)\cdot\cos(2\omega t)) \quad \cdots \quad (9)$$

[0066] Since the current irec appears as the absolute value of the input current Iin, as opposed to the technique described in the first document group (hereinafter referred to as a "basic technique"), the input current Iin differs from a sinusoidal current. In this embodiment (including not only the "first setting" but also the "second setting", which holds true for the description below), thus, the crest value Im is a crest value of the current that shows a sine wave and has an effective value of the input current Iin (i.e., a time average of the powers of the input current Iin) as an effective value.

[0067] In the formula (9), regardless of the value of k, $\left|\sin(\omega t)\right| = 1/\sqrt{2}$ and the current irec takes a value $Im/\sqrt{2}$ when $\cos(2\omega t) = 0$. In this embodiment, accordingly, the crest value Im of the current irec can be regarded as being $\sqrt{2}$ times a value of the current irec (i.e., an absolute value of the current Iin) when the phase angle ωt is $\pi/4$ and $3\pi/4$ (i.e., a boundary between the providing period and the receiving period).

[0068] From the formula (9), the power input from the single-phase AC power supply 1 in the providing period can be obtained by the formula (10).

[0069] ~~[Math 10]~~

$$Pin = Vm \cdot Im \cdot \sin^2(\omega t) \cdot (1-(1-k)\cdot\cos(2\omega t)) \quad \cdots \quad (10)$$

[0070] The power input to the inverter 5, that is, instantaneous output power Pout consumed by the inverter 5 is obtained as the product of the DC current Idc and the virtual DC voltage Vdc, which is obtained by the formula (11).

[0071] ~~[Math 11]~~

$$\begin{aligned} \text{Pout} &= \text{Vdc} \cdot \text{Idc} \\ &= \frac{\text{Vm} \cdot \text{Im}}{2}(1-(1-\text{k}) \cdot \cos(2\omega t)) \quad \cdots \quad (11) \end{aligned}$$

[0072] A difference between the formulas (10) and (11) is thus obtained as being expressed by the formula (12), which matches the formula (2).

[0073] ~~[Math 12]~~

$$\begin{aligned} \text{Pout} - \text{Pin} &= \frac{\text{Vm} \cdot \text{Im}}{2}\left[(1-(1-\text{k}) \cdot \cos(2\omega t)) - 2\sin^2(\omega t)\right] \\ &= \frac{\text{Vm} \cdot \text{Im}}{2} \cdot \cos(2\omega t) \cdot \text{k} \qquad \cdots \quad (12) \end{aligned}$$

[0074] The validity of setting the DC current Idc by the formula (8) has therefore been described.

[0075] In the receiving period, the current il is set as being expressed by the formula (13). The power stored in the charge and discharge circuit 4 in the receiving period is accordingly calculated as the formula (14), and is equal in an absolute value to and a polarity opposite to those of the formula (2) expressing the instantaneously provided/received power Pbuf. The validity of setting the current il by the formula (13) is therefore revealed.

[0076] ~~[Math 13]~~

$$\text{il} = \text{k} \cdot \text{Im} \cdot \left[|\sin(\omega t)| - \frac{1}{2|\sin(\omega t)|} \right] \quad \cdots \quad (13)$$

[0077] ~~[Math 14]~~

$$\begin{aligned} |\text{Vin}| \cdot \text{il} &= \text{Vm}|\sin(\omega t)| \cdot \text{k} \cdot \text{Im} \cdot \left[|\sin(\omega t)| - \frac{1}{2|\sin(\omega t)|} \right] \\ &= \text{Vm} \cdot \text{Im} \cdot \text{k} \cdot \left[\sin^2(\omega t) - \frac{1}{2} \right] \\ &= \frac{1}{2}\text{Vm} \cdot \text{Im} \cdot \text{k} \cdot \left[-\cos(2\omega t) \right] \qquad \cdots \quad (14) \end{aligned}$$

individually controlled at the discharge duty dc and the switching of the inverter 5 is controlled at the zero duty dz (i.e., a zero-phase current flows in the period equivalent to the zero duty dz, irrespective of the voltage output from the inverter 5) in accordance with the formula (15) in the providing period and the formula (16) in the receiving period, thus achieving a rectifying duty drec. Also in this case, the switch Sci is not conductive in the receiving period.

[0083] ~~[Math 15]~~

$$\left.\begin{aligned} dc &= \frac{Vm}{vc}\cdot\frac{\cos(2\omega t)}{\sqrt{2}} \\ dz &= 1 - dc - \sqrt{2}\left|\sin(\omega t)\right| \end{aligned}\right\} \quad \cdots \quad (15)$$

[0084] ~~[Math 16]~~

$$\left.\begin{aligned} dc &= 0 \\ dz &= 1 - \frac{1}{\sqrt{2}\left|\sin(\omega t)\right|} \end{aligned}\right\} \quad \cdots \quad (16)$$

[0085] More specific approaches for (iv) and (v) above are described in the first document group and are thus omitted herein.

[0086] FIGs. 3 and 4 are graphs each showing the operation of the direct power converter shown in FIG. 1. FIG. 3 shows the case where the basic technique is employed, and FIG. 4 shows the case where (i) to (iv) are employed, where setting is made such that k = 1/3. An equal voltage ratio Vc/Vm is set in FIGs. 3 and 4. The basic technique corresponds to the case where k = 1 in the "first setting" (see the formulas (8) to (14)).

[0087] In both of FIGs. 3 and 4, the uppermost tier shows the duties drec, dc and dz, the second tier from the top shows the voltages Vrec·drec and Vc·dc, the virtual DC

[0097] ~~[Math 17]~~

$$Ra = \int_{\pi/4}^{3\pi/4} |\sin(\omega t)| d(\omega t)/(\pi/2) = \frac{2\sqrt{2}}{\pi} \quad \cdots \quad (17)$$

[0098] Similarly, the waveform of the virtual DC voltage Vdc in the providing period is set by the formula (18).

[0099] ~~[Math 18]~~

$$Vdc = Vm \cdot |\cos(\omega t)| \quad \cdots \quad (18)$$

[0100] That is to say, in the "second setting", the waveform of the virtual DC voltage Vdc is a waveform (hereinafter referred to as a "two-phase full-wave rectification waveform") obtained by performing full-wave rectification on a two-phase AC voltage having a crest value Vm.

[0101] There is a phase difference of π/2 between the providing period and the receiving period, and also, there is a phase difference of π/2 between the sine waveform and the cosine waveform. The average value Ra in the providing period is accordingly equal to that of the receiving period. The average value Ra can be thus obtained by the formula (17) in any of the providing period and the receiving period. This means that the average value Ra is improved to be $(2\sqrt{2}/\pi)/(1/\sqrt{2}) = 4/\pi$ times, that is, approximately 1.11 times ~~compared with~~that of the basic technique or the "first setting".

[0102] Not only the average value Ra but also the voltage utilization ratio R is improved per se compared with the basic technique or the "first setting", irrespective of the phase angle ωt. This is revealed from the fact that the virtual DC voltage Vdc, as it takes the two-phase full-wave rectification waveform whose minimum value is $Vm/\sqrt{2}$, is greater than or equal to a (constant) virtual DC voltage Vdc (= $Vm/\sqrt{2}$) obtained in the basic technique or the "first setting".

[0103] A specific approach for approximately making the waveform of the virtual DC

voltage Vdc the two-phase full-wave rectification waveform will now be described. First, in the receiving period, the waveform of the virtual DC voltage Vdc is set to be equal to the absolute value of the input voltage Vin, so the rectifying duty drec should be set to one. More specifically, both of the discharge duty dc and the zero duty dz should be set to zero in view of the formula (4). That is to say, in the receiving period, the switch Sc is not conductive, and the inverter 5 can operate in response to requests for the currents Iu, Iv and Iw caused to flow into the inductive load 6 (without such a limitation to cause the zero-phase current iz to flow for setting a virtual DC voltage Vdc).

[0104] In the providing period, the rectifying duty drec is set similar to the "first setting", and the discharge duty dc is set to $\sqrt{2}$ times the value set in the "first setting". More specifically, the switch Sc should be switched at the discharge duty dc expressed by the formula (19) and the inverter 5 should be operated at the zero duty dz.

[0105] ~~[Math 19]~~

$$\left.\begin{aligned} dc &= \frac{Vm}{vc}\cdot\cos(2\omega t) \\ dz &= 1 - dc - \sqrt{2}\left|\sin(\omega t)\right| \end{aligned}\right\} \quad \cdots \quad (19)$$

[0106] The DC current Idc pulsates, and thus, Im/Idc does not have a constant value as in the basic technique. Even when the rectifying duty drec is set in the providing period as in the "first setting", however, the pulsation of the DC current Idc is small (a maximum value of pulsation is obtained by $1-1/\sqrt{2}$, which is approximately 30%) if k = 1, and the rectifying duty drec is less than or equal to one. In the providing period, accordingly, |Iin| = irec = irec1 = Idc·drec is little distorted.

[0107] The virtual DC voltage Vdc in the providing period can be thus obtained by the formula (20).

[0108] ~~[Math 20]~~

$$Vdc = Vm \cdot \sqrt{2} \cdot \sin^2(\omega t) + Vm \cdot |\cos(2\omega t)|$$
$$= \frac{Vm}{\sqrt{2}} \left\{ 1 + (\sqrt{2} - 1) |\cos(2\omega t)| \right\} \quad \cdots \quad (20)$$

[0109] The formula (20) is approximated closely to the formula (18) at the phase angles ωt of, for example, values 3π/4 to 5π/4 in the providing period. Specifically, it is revealed that there is a less than 1% difference between the value of integral of the virtual DC voltage Vdc expressed by the formula (18) over the providing period and the value of integral of the virtual DC voltage Vdc expressed by the formula (20) over the providing period.

[0110] The above reveals that by setting dc = dz = 0 in the receiving period and using the duties expressed by the formula (19) in the providing period, the waveform of the virtual DC voltage Vdc can be approximated to a two-phase full-wave rectification waveform, thus improving the voltage utilization ratio R.

[0111] The DC current Idc set by the formula (8) is adopted also in the "second setting", so the formula (11) holds. That is to say, the right-hand side of the formula (11) needs to be obtained in the "second setting" as well as in the "first setting". Letting Vdc1 and Idc1 be the respective average values per cycle of the power supply phase of the virtual DC voltage Vdc and the DC current Idc in the "first setting", and letting Vdc2 and Idc2 be the respective average values per cycle of the power supply phase of the virtual DC voltage Vdc and the DC current Idc in the "second setting", the formula (21) holds.

[0112] ~~[Math 21]~~

$$Vdc1 \cdot Idc1 = Vdc2 \cdot Idc2 \quad \cdots \quad (21)$$

[0113] $Vdc1 = Vm/\sqrt{2}$ and $Vdc2 = (2\sqrt{2}/\pi)Vm$ in the description above, revealing a relationship $Idc2 = (\pi/4)Idc1$.

[0114] The current il in the "second setting" thus needs to be corrected, with respect to the current il in the "first setting" expressed by the formula (13), by a product $\pi/(2\sqrt{2})$ of a ratio Idc2/Idc1 = $\pi/4$ and a ratio $\sqrt{2}$ of the discharge duty dc in the "second setting" expressed by the formula (19) to the discharge duty dc in the "first setting" expressed by the formula (15). That is to say, the current il in the "second setting" is set by the formula (22).

[0115] ~~[Math 22]~~

$$il = k \cdot Im \cdot \left[|\sin(\omega t)| - \frac{1}{2|\sin(\omega t)|} \right] \cdot \frac{\pi}{2\sqrt{2}} \quad \cdots \quad (22)$$

[0116] The above reveals that when control is being performed so that the rectifying duty drec expressed by the formula (6) is satisfied to cause the current irec1 to flow from the converter 3 to the inverter 5 in the providing period, further performing control below can increase a voltage utilization ratio while reducing the instantaneously provided/received power Pbuf.

[0117] (i) The inverter 5 is caused to receive the current Idc that satisfies the formula (8).

(iii) The current il that satisfies the formula (22) is input to the buffer circuit 4a in the receiving period.

[0118] In order to allow the pulsation of the virtual DC voltage Vdc utilized by the inverter 5 to further increase the voltage utilization ratio R, further,

(vi) the switch Sc is rendered conductive at the discharge duty dc that satisfies the formula (19) to discharge the capacitor C4 in the providing period, and

(vii) in the receiving period, not only the discharge duty dc but also the zero duty dz is set to zero, and the rectifying duty drec is set to one.

[0119] Specific approaches for (vi) and (vii) above can be achieved easily based on the

[0132] (b-4) Example of Technique for Inputting Current Idc to Inverter 5

This section will describe an example for achieving the formula (8) adopted for the current Idc commonly in the "first setting" and the "second setting" regarding duties.

[0133] Described below is an example in which well-known dq-axis control is performed as for the operation of a normal AC load. The power formula on the dq axes is typically expressed by the formula (23). Symbols V* and I respectively represent a command value of a voltage applied to the AC load and a current flowing through the AC load. They both are alternating, and thus, dots indicating that they are represented as complex numbers are placed above both of the symbols V* and I. Note that the q-axis voltage ideally follows a command value Vq* thereof, and the d-axis voltage ideally follows a command value Vd* thereof.

[0134] ~~[Math 23]~~

$$P + jQ = \dot{V}^{*} \cdot \dot{I} = Vd^{*} \cdot Id + Vq^{*} \cdot Iq + j(Vq^{*} \cdot Id - Vd^{*} \cdot Iq) \quad \cdots \quad (23)$$

[0135] The power supplied from the DC power supply lines LH and LL to the inverter 5 has no reactive power, and thus, the power is expressed by the formula (24) ignoring the third term of the formula (23).

[0136] ~~[Math 24]~~

$$Pdc = Vd^{*} \cdot Id + Vq^{*} \cdot Iq \quad \cdots \quad (24)$$

[0137] The instantaneous output power Pout expressed by the formula (11) matches the formula (24), so the formula (25) holds.

[0138] ~~[Math 25]~~

$$Pdc = Pout = \frac{Vm \cdot Im}{2}(1 - (1 - k) \cdot \cos(2\omega t)) = \frac{Vm \cdot Im}{2} - \frac{(1 - k)Vm \cdot Im}{2}\cos(2\omega t) \quad \cdots \quad (25)$$

[0139] Control to achieve the formula (8) can thus be performed by performing control

the operations of the switches Sc and Sl, which are generated based on the duties drec, dc, dz and dl (e.g., see the first document group).

[0144] Described below is a processor 71 for performing control so that the AC component of the formula (24) and the second term of the rightmost-hand side of the formula (25) match each other. The processor 71 includes a DC power calculator 711, a pulsating component extractor 712, a pulsating component calculator 713, a subtracter 714, an adder 715 and a PI processor 716.

[0145] The DC power calculator 711 receives the q-axis voltage command value Vq* and the d-axis voltage command value Vd*, and the q-axis current Iq and the d-axis current Id, and calculates DC power Pdc based on the formula (24) above, thus providing the DC power Pdc~~it~~ to the pulsating component extractor 712.

[0146] The pulsating component extractor 712 extracts and outputs the AC component of the formula (24). The pulsating component extractor 712 is achieved by, for example, a highpass filter HPF.

[0147] The pulsating component calculator 713 receives the crest values Vm and Im, the power supply angular velocity ω, and the constant k, thus obtaining the second term of the rightmost-hand side of the formula (25). The crest values Vm and Im and the power supply angular velocity ω can be input to the pulsating component calculator 713 as the information obtained from the single-phase AC power supply 1 (see FIG. 1).

[0148] As described above, desired processing is causing the AC component of the formula (24) and the second term of the rightmost-hand side of the formula (25) to match each other, and thus, control should be performed so as to reduce a difference between the output of the pulsating component extractor 712 and the output of the pulsating component calculator 713. The subtracter 714 thus obtains the difference, thus outputting, to the adder 715, a value obtained by the PI processor 716 performing integral

ripple current and its allowable value (right vertical axis).

[0153] Symbols H1 and H2 each represent the capacitor capacity used in the case where a single-phase power factor correction circuit is used. The symbols H1 and H2 respectively ~~are~~ represent data in the case where air conditioners have air conditioning abilities of 6 kW and 11.2 kW. The power factor correction circuit can herein be regarded as having a configuration in which the switch Sc is shorted and removed from the charge and discharge circuit 4, and a connection point between the reactor L4 and the converter 3 is not directly connected with the inverter 5. In this configuration, a series connection of the diode D40 and the reactor L4 is provided between the converter 3 and the inverter 5 in the DC power supply line LH, and the capacitor C4 is connected in parallel with the inverter 5 between the DC power supply lines LH and LL.

[0154] According to Non-Patent Documents 2 and 3, the capacitor capacity C required in the basic technique is obtained by the formula (26). Note that a maximum value Vcmax and a minimum value Vcmin of the both-end voltage Vc are introduced.

[0155] ~~[Math 26]~~

$$C = \frac{Vm \cdot Im}{\omega(Vcmax^2 - Vcmin^2)} \quad \cdots \quad (26)$$

[0156] On a graph G1, values obtained by calculating capacitor capacities required in the basic technique (the case where k = 1 in the "first setting") are plotted. Note that maximum value Vcmax = 400 + 50 = 450 (V) and minimum value Vcmin = 400 - 50 = 350 (V) hold. Solid circles on the graph G1 indicate the same cases indicated by the symbols H1 and H2 in input power. However, actually used capacitor capacities are plotted as the symbols H1 and H2, and back calculation of them from the formula (26) yields a deviation of approximately ±5% in the both-end voltage Vc.

[0157] As can be seen from the comparison between the symbols H1 and H2 and the

solid circles on the graph G1, in the basic technique, capacitor capacities are reduced to approximately 1/3 to 1/4 times compared with a normal power factor correction circuit.

[0158] In the basic technique, however, a ripple current shown by a graph G2 flows through the capacitor C4. A graph G3, meanwhile, shows a ripple current (e.g., values at 45°C using an electrolytic capacitor of GW-series (105°C specifications) from Nichicon Corporation) allowable when the capacitor capacity obtained by the graph G1 is obtained by the electrolytic capacitor. The comparison between the graphs G2 and G3 reveals that in the basic technique, the capacitor C4 cannot be achieved by an electrolytic capacitor from the perspective of whether a ripple current is allowable.

[0159] In the "first setting" and "second setting" above, however, by introducing a constant k (< 1), an amount of pulsations of the power stored in the capacitor C4 can be reduced more than in the basic technique (the case where k = 1 in the "first setting"). This achieves the capacitor C4 by an electrolytic capacitor by setting the constant k in accordance with a desired capacitor capacity, contributing to achieving the charge and discharge circuit 4 inexpensively.

[0160] (c-2) Description of Advantages in Boost circuit 4b

This section will describe that the instantaneously provided/received power Pbuf is reduced to achieve the boost circuit 4b inexpensively.

[0161] Even the basic technique requires lower power capacity than a normal power factor correction circuit does, which will be described first. From the formula (1), the power passing through a power factor correction circuit is obtained by the formula (27).

[0162] ~~[Math 27]~~

$$\frac{Vm \cdot Im}{\pi}\int_0^{\pi}\frac{1}{2}(1-\cos 2\theta)d\theta = \frac{Vm \cdot Im}{2} \quad \cdots \quad (27)$$

[0163] In the basic technique, meanwhile, the power provided to the capacitor C4 via

the boost circuit 4b is obtained by the formula (28) based on the formula (2).

[0164] ~~[Math 28]~~

$$\frac{Vm \cdot Im}{\pi}\int_{\pi/4}^{3\pi/4}\left(-\frac{1}{2}\cos 2\theta\right)d\theta = \frac{Vm \cdot Im}{2\pi} \quad \cdots \quad (28)$$

[0165] As revealed from the comparison between the formulas (27) and (28), in the basic technique, the power capacity required for the boost circuit 4b is reduced to $1/\pi$ times (approximately 1/3 times) compared with the power factor correction circuit.

[0166] Introducing a constant k (< 1) in the "first setting" and "second setting" reduces the instantaneously provided/received power Pbuf more than in the basic technique, thus revealing that the power capacity is more reduced.

[0167] Even in the basic technique, the peak value of the current il flowing through the reactor L4 is also reduced to 1/2 times the peak value (which is a crest value Im) in the case of the power factor correction circuit, as expressed by the formula (29).

[0168] ~~[Math 29]~~

$$il = Im\left(|\sin(\omega t)| - \frac{1}{2|\sin(\omega t)|}\right)$$
$$\leq \frac{Im}{2}(\omega t = \pi/2, 3\pi/2) \quad \cdots \quad (29)$$

[0169] Introducing the constant k (< 1) in the "first setting" and the "second setting" can reduce a current il compared with the basic technique, thus revealing that the power capacity required for the reactor L4 is further reduced in view of the formula (29).

[0170] D. Modifications

In the basic technique as well as the technique involving introducing the constant k (< 1) in the "first setting" and the "second setting", the filter 2 can also be provided between the converter 3 and the charge and discharge circuit 4.

[0171] FIG. 9 is a circuit diagram in a case where the filter 2 is provided between the

CLAIMS

1. A method for controlling a direct power converter,

said direct power converter comprising:

a first power supply line ~~(LH)~~;

a second power supply line ~~(LL)~~ which is applied with a potential lower than said first power supply line is applied;

a converter ~~(3)~~ including an input side connected with a single-phase AC power supply ~~(1, 2)~~ and an output side connected with said first power supply line and said second power supply line, and performing single-phase full-wave rectification;

a charge and discharge circuit ~~(4)~~ located between said first power supply line and said second power supply line; and

an inverter ~~(5)~~ that converts a DC voltage between said first power supply line and said second power supply line into an AC voltage,

said charge and discharge circuit comprising

a buffer circuit ~~(4a)~~ including a capacitor ~~(C4)~~ and a first switch ~~(Sc, D42)~~ connected in series with said capacitor at a side close to said first power supply line between said first power supply line and said second power supply line, and providing and receiving power between said first power supply line and said second power supply line, and

a boost circuit ~~(4b)~~ that boosts a rectified voltage ~~(Vrec)~~ from said converter ~~(3)~~ to charge said capacitor,

said buffer circuit ~~(4a)~~ providing power to said first power supply line and said second power supply line in a first period ~~(T1)~~ in which a cosine value ~~(cos(2ωt))~~ to a value ~~(2ωt)~~ of twice a phase angle ~~(ωt)~~ of an AC waveform output from said single-phase AC power supply ~~(1, 2)~~ is positive when the AC waveform is regarded as a sine value

(sin(ωt)) of the phase angle (ωt); receiving power from said first power supply line and said second power supply line in a second period (T2) in which said cosine value is negative,

said converter (3) being conductive at a rectifying duty (dree), said rectifying duty taking a value of $\sqrt{2}$ -times an absolute value (|sin(ωt)|) of said sine value in said first period,

said method determining power (Vdc·Idc) input to said inverter (5) as a product of an absolute value ($Im/\sqrt{2}$) of an input current input to said converter (3) at a boundary between said first period and said second period, an effective value ($Vm/\sqrt{2}$) of an AC voltage (Vin) of said single-phase AC power supply, and a value ((1-(1-k)·cos(2ωt)) obtained by subtracting, from one, a value obtained by multiplying said cosine value (cos(2ωt)) by a positive constant (1-k) less than one.

2. The method for controlling a direct power converter according to claim 1, wherein

said rectifying duty (dree) takes an inverse number ($1/(\sqrt{2}|\sin(\omega t)|)$) of the value of $\sqrt{2}$ -times the absolute value (|sin(ωt)|) of said sine value in said second period (T2), and

said first switch (Sc, D42) is rendered conductive to discharge said capacitor (C4) in said first period (T1) at a discharge duty (dc) taking a value obtained by dividing, by $\sqrt{2}$, a product of said cosine value (cos(2ωt)) and a value (Vm/Vc) obtained by dividing a crest value (Vm) of the AC voltage (Vin) of said single-phase AC power supply by a both-end voltage (Vc) of said capacitor.

3. The method for controlling a direct power converter according to claim 1,

wherein

said rectifying duty ~~(drec)~~ takes a value 1 in said second period ~~(T2)~~, and

said first switch ~~(Sc, D42)~~ is rendered conductive to discharge said capacitor ~~(C4)~~ in said first period ~~(T1)~~ at a discharge duty ~~(dc)~~ taking a product of said cosine value ~~(cos(2ωt))~~ and a value ~~(Vm/Vc)~~ obtained by dividing a crest value ~~(Vm)~~ of the AC voltage ~~(Vin)~~ of said single-phase AC power supply by a both-end voltage ~~(Vc)~~ of said capacitor.

4. The method for controlling a direct power converter according to any one of claims 1 to 3, wherein

said boost circuit ~~(4b)~~ comprises:

a diode ~~(D40)~~ including an anode~~a cathode~~ and a cathode~~an anode~~ that is connected between said first switch ~~(Sc, D42)~~ and said capacitor ~~(C4)~~;

a reactor ~~(L4)~~ connected between said first power supply line ~~(LH)~~ and said anode~~cathode~~, through which a current input to said boost circuit flows; and

a second switch ~~(S1, D41)~~ connected between said second power supply line ~~(LL)~~ and said anode~~cathode~~, and

said second switch of said boost circuit is controlled to control a current ~~(il)~~ flowing through said reactor ~~(L4)~~ in said second period ~~(T2)~~.