CLAIMS

[Claim 1] A semiconductor memory device comprising:

a semiconductor layer extending in a first direction;

a gate electrode layer including at least one metal element selected from a group consisting of tungsten (W), molybdenum (Mo), and cobalt (Co);

a charge storage layer provided between the semiconductor layer and the gate electrode layer;

a first insulating layer provided between the charge storage layer and the gate electrode layer, the first insulating layer including a first region and a second region, the first region including aluminum (Al) and oxygen (O), the second region provided between the first region and the gate electrode layer, the first region being crystalline, the second region being amorphous; and

a metal layer provided between the first insulating layer and the gate electrode layer, the metal layer being in contact with the second region and the gate electrode layer, the metal layer including titanium (Ti) and nitrogen (N).

[Claim 2] The semiconductor memory device according to claim 1,

wherein the second region includes at least one of aluminum (Al), hafnium (Hf), or zirconium (Zr).

[Claim 3] The semiconductor memory device according to claim 2,

wherein the second region includes at least one of oxygen (O) or nitrogen (N).

[Claim 4] The semiconductor memory device according

to claim 1,

wherein a thickness of the second region in a second direction from the semiconductor layer to the gate electrode layer is equal to or more than 0.1 nm and equal to or less than 1 nm.

[Claim 5] The semiconductor memory device according to claim 1,

wherein a thickness of the first region in a second direction from the semiconductor layer to the gate electrode layer is equal to or more than 1 nm and equal to or less than 5 nm.

[Claim 6] The semiconductor memory device according to claim 1, further comprising:

a second insulating layer provided between the charge storage layer and the first insulating layer, the second insulating layer including silicon (Si) and oxygen (O).

[Claim 7] The semiconductor memory device according to claim 1, further comprising:

a third insulating layer provided between the charge storage layer and the semiconductor layer.

[Claim 8] The semiconductor memory device according to claim 1, further comprising:

a fourth insulating layer provided in the first direction of the gate electrode layer, the first insulating layer provided between the fourth insulating layer and the gate electrode layer.

[Claim 9] The semiconductor memory device according to claim 1,

wherein a thickness of the metal layer in a second

direction from the semiconductor layer to the gate electrode layer is equal to or more than 1 nm and equal to or less than 5 nm.