ABSTRACT OF THE DISCLOSURE

SRAM CELL WITH THIN FILM TRANSISTOR USING TWO POLYSILICON LAYERS

A TFT formed on a semiconductor substrate of a first conductivity type, includes a first doped portion of a polysilicon layer over FOX regions and a first insulating layer. A buried contact extends through the first portion of a polysilicon layer and the first insulating layer to the surface of the substrate adjacent to a FOX region. A second doped portion of the polysilicon layer overlies the first portion and forms a buried contact between the second portion and the substrate. The polysilicon layer forms a gate electrode and a conductor from the buried contact. Doped source/drain regions in the substrate are juxtaposed with the gate electrode. An interelectrode dielectric layer over the gate electrode and the conductor has a gate opening therethrough down to the substrate. A gate oxide layer is formed on the surface of the substrate at the gate opening. A semiconductor film extends over the interelectrode dielectric layer and over the surface of the substrate through the gate opening. A doped channel region is formed between source/drain regions in the semiconductor film above the gate opening, and above the gate opening of a TFT, with the doped region therebelow comprising the gate of the TFT.

(FIGURE 1 IS SUGGESTED FOR PUBLICATION)