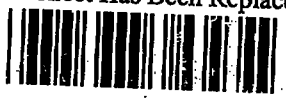
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ABSTRACT

A process for forming salicided CMOS devices, and non-salicide CMOS devices, on the same semiconductor substrate, using only one silicon nitride layer to provide a component for a composite spacer on the sides of the salicided CMOS devices, and to provide a blocking shape during metal silicide formation, for the non-salicided CMOS devices, has been developed. The process features the use of a disposable organic spacer, on the sides of polysilicon gate structures, used to define the heavily doped source/drain regions, for all CMOS devices. A silicon nitride layer, obtained via LPCVD procedures, at a temperature between 800 to 900° C, is then deposited and patterned to provide the needed spacer, on the sides of the CMOS devices experiencing the salicide process, while the same silicon nitride layer is used to provide the blocking shape needed to prevent metal silicide formation for the non-salicided CMOS devices.