structure 600 and selectively remove the first contact layer 616 (*e.g.*, silicon germanium (SiGe)) while very slowly removing the first semiconductor regions 606 (*e.g.*, silicon (Si)). Generally speaking, the SRP described herein is useful for removing $Si_{(1-X)}Ge_X$ (including germanium *i.e.*, X=1) faster than $Si_{(1-Y)}Ge_Y$, for all $X>Y$. In some embodiments, the etch selectivity of silicon germanium results partly from the presence of an ion suppressor (*e.g.*, the perforated partition 422 shown in Figure 4) positioned between a chamber plasma region (*e.g.*, the chamber plasma region 426 shown in Figure 4) and the substrate processing region (*e.g.*, the substrate processing region 428 shown in Figure 4).

[0088] The fluorine-containing precursor includes nitrogen trifluoride, fluorocarbon, atomic fluorine, diatomic fluorine, interhalogen fluoride (*e.g*. bromine trifluoride, chlorine trifluoride), sulfur hexafluoride, xenon difluoride, or a combination thereof. A diluent gas (*e.g.*, argon (Ar), helium (He), nitrogen (N_2), or a combination thereof) is also flowed into the chamber plasma region where it is simultaneously excited in a plasma along with the fluorine-containing precursor. The diluent gas reduces diffusivity of plasma effluents and thus increases the etch selectivity of silicon germanium.

[0089] In some embodiments, the fluorine-containing precursor (*e.g*. nitrogen trifluoride (NF_3)) is supplied at a flow rate of between about 5 sccm (standard cubic centimeters per minute) and about 40 sccm, argon (Ar) at a flow rate of between about 4 sccm and about 1500 sccm, helium (He) at a flow rate of between about 100 sccm and about 5000 sccm, and nitrogen (N_2) at a flow rate of between about 100 sccm and about 5000 sccm. The SRP may be performed at a temperature of between about -20°C and about 60°C and at a pressure of between 1 Torr and 50 Torr. The etch selectivity of silicon germanium (SiGe) with a ratio of germanium (Ge) of 30% may be higher than 200:1 to phosphorus-doped silicon (Si:P), higher than 500:1 to thermal oxide (SiO_x), and higher than 500:1 to silicon nitride (Si_3N_4).

[0090] In block 550, a conventional plasma ashing process is performed to remove the patterning stack 620, as shown in Figure 6E. The plasma ashing process may be performed in a processing chamber, such as the processing chamber 122 shown in Figure 1, or the processing chamber 200 shown in Figure 2.

[0091] The plasma ashing process can use a plasma formed from a gas including oxygen (O_2). The ashing process can use a wet clean process using a solution, such as a mixture of sulfuric acid (H_2SO_4) and hydrogen peroxide (H_2O_2), to remove residue of the patterning stack 620 on the semiconductor structure 600.

[0092] In block 560, a second deposition process is performed, as shown in Figure 6F. The second deposition process may be each performed in a processing chamber, such as the processing chamber 126, 128, or 130 shown in Figure 1, or the processing chamber 300 shown in Figure 3.

[0093] In the second deposition process, a metal layer 622 is formed on the exposed surfaces of the first semiconductor regions 606 and the second contact layer 618. The metal layer 622 contacts the second contact layer 618 and provides an electrical connection between a contact plug to be formed within the second openings 614 and the second semiconductor regions 608, while maintaining an electrical connection therethrough. The metal layer 622 may be formed of a metal material, such as titanium (Ti), cobalt (Co), nickel (Ni), molybdenum (Mo), or tantalum (Ta), or silicide thereof.

[0094] In some embodiments, the metal source may include a precursor that includes titanium (Ti), tantalum (Ta), cobalt (Co), nickel (Ni), or molybdenum (Mo) or combination thereof. The second deposition process may be each performed at a temperature of between about 300°C and about 800°C and at a pressure of between 1 Torr and 50 Torr.

[0095] In the second deposition process, a barrier metal layer 624 can also be formed on the exposed inner surfaces of the first opening 612 and the second opening 614, and the exposed surfaces of the dielectric layer 610. The barrier metal layer 624 protects the metal layer 622 and allow nucleation and growth of contact plugs in the first opening 612 and the second opening 614, as discussed below. The barrier metal layer 624 may be formed of a barrier metal material that is titanium nitride (TiN), or tantalum nitride (TaN). In some embodiments, the metal layer 622 is a silicide layer that is formed from a portion of the barrier metal layer 624 by use of a spike-anneal process. In some other embodiments, the metal layer 622 is a silicide layer that is formed by a separate selective deposition process that is performed before forming the barrier metal layer 624.

[0100] The method 700 begins with a pre-clean process in block 710. The pre-clean process in block 710 is generally the same as the pre-clean process in block 510. The pre-clean process in block 710 may be tailored such that a growth rate of an epitaxial layer of the third material (*e.g.*, silicon germanium (SiGe)) on exposed surfaces of the second semiconductor regions 608 (*e.g.*, silicon germanium (SiGe)) is higher than a growth rate of an epitaxial layer of the third material (*e.g.*, silicon germanium (SiGe)) on exposed surfaces of the first semiconductor regions 606 (*e.g.*, silicon (Si)). Knobs for controlling the pre-clean process may include a gas chemistry, a gas ratio, a gas flow rate, a substrate temperature, temperature gradients, a chamber pressure, power and/or frequency of the power source, RF excitation frequencies, duty cycle and/or frequency of RF powers, etch time, or a combination thereof. As discussed above, the modulation of the growth rate of a subsequently deposited epitaxial layer can be adjusted by controlling or adjusting the composition of the materials disposed at the surfaces of the first semiconductor regions 606 and the second semiconductor regions 608 and/or altering the crystal structure of the material at the surfaces of the first semiconductor regions 606 and the second semiconductor regions 608 after performing the pre-clean process.

[0101] In block 720, a first selective deposition process is performed to epitaxially form a first contact layer 816 on exposed surfaces of the first semiconductor regions 606 within the first opening 612, and a second contact layer 818 on exposed surfaces of the second semiconductor regions 608 within the second opening 614, as shown in Figure 8B. The first selective deposition process in block 720 can in general be the same as the first selective deposition process in block 520. In some embodiments, due to the way the pre-clean process in block 710 was performed and thus the state of the surfaces of the first semiconductor regions 606 and the second semiconductor regions 608 during the first selective deposition process, the second contact layer 818 will grow to a greater thickness than the thickness of the first contact layer 816 during the same processing time period.

[0102] In some other embodiments of block 720, the process parameters used to simultaneously form the second contact layer 818 and the first contact layer 816 are adjusted and/or controlled such that the thickness of the second contact layer 818 formed on the second semiconductor regions 608 is greater than the thickness of the first contact layer 816 formed on the first semiconductor regions 606 during the same

[0106] In block 750, a metal fill process is performed to form the first contact plug 626 in the first opening 612 and the second contact plug 628 in the second opening 614, as shown in Figure 8E. The metal fill process provided in block 750 can be the same as the metal fill process in block 670.

[0107] The embodiments described herein provide methods and system for forming a contact epitaxial layer within a trench on a selected portion of a transistor structure. The contact trench structure includes a metal contact plug formed within a trench between adjacent device modules, and contacts that interface between the contact plug and silicon-based channels in the device modules. The contacts are formed by a selective deposition process, reducing parasitic resistance. The metal contact plug is formed void-free by a deposition-each-deposition process, reducing contact resistance. The contact epitaxial layer may be p-type silicon germanium formed on an exposed surface of a p-type MOS device (*e.g.*, silicon germanium) while no epitaxial layer may be formed on an n-type MOS (*e.g.*, silicon) or a dielectric layer formed over the p-type MOS device and the n-type MOS device. The methods and systems do not require a patterning of an epitaxial layer using a photomask, and thus damages on a fabricated semiconductor structures are reduced.

[0108] While the foregoing is directed to embodiments of the present disclosure, other and further embodiments of the disclosure may be devised without departing from the basic scope thereof, and the scope thereof is determined by the claims that follow.