Method of Minimizing Via Sidewall Damages During Dual Damascene Trench Reactive Ion Etching in a Via First Scheme

ABSTRACT

A method of minimizing undercut of a hard mask in an integrated circuit (IC) structure including steps of providing an IC structure having a substrate, a interlayer dielectric layer, and a hard mask, forming a via in said IC structure, and depositing an organic planarizing layer (OPL) over the IC structure such that it fills the vias formed therein. The method also includes steps of forming a masking structure layer over the OPL, forming an opening in the masking structure that has a critical dimension (CD) smaller than an opening design dimension, anisotropic etching the OPL such that sidewall of the via remains covered with the OPL while forming a trench, and removing any remaining OPL on the sidewalls and trench, wherein the undercut of the sidewalls with respect to the hard mask is minimized by the covering of OPL during the anisotropic etching process.

Figure 1