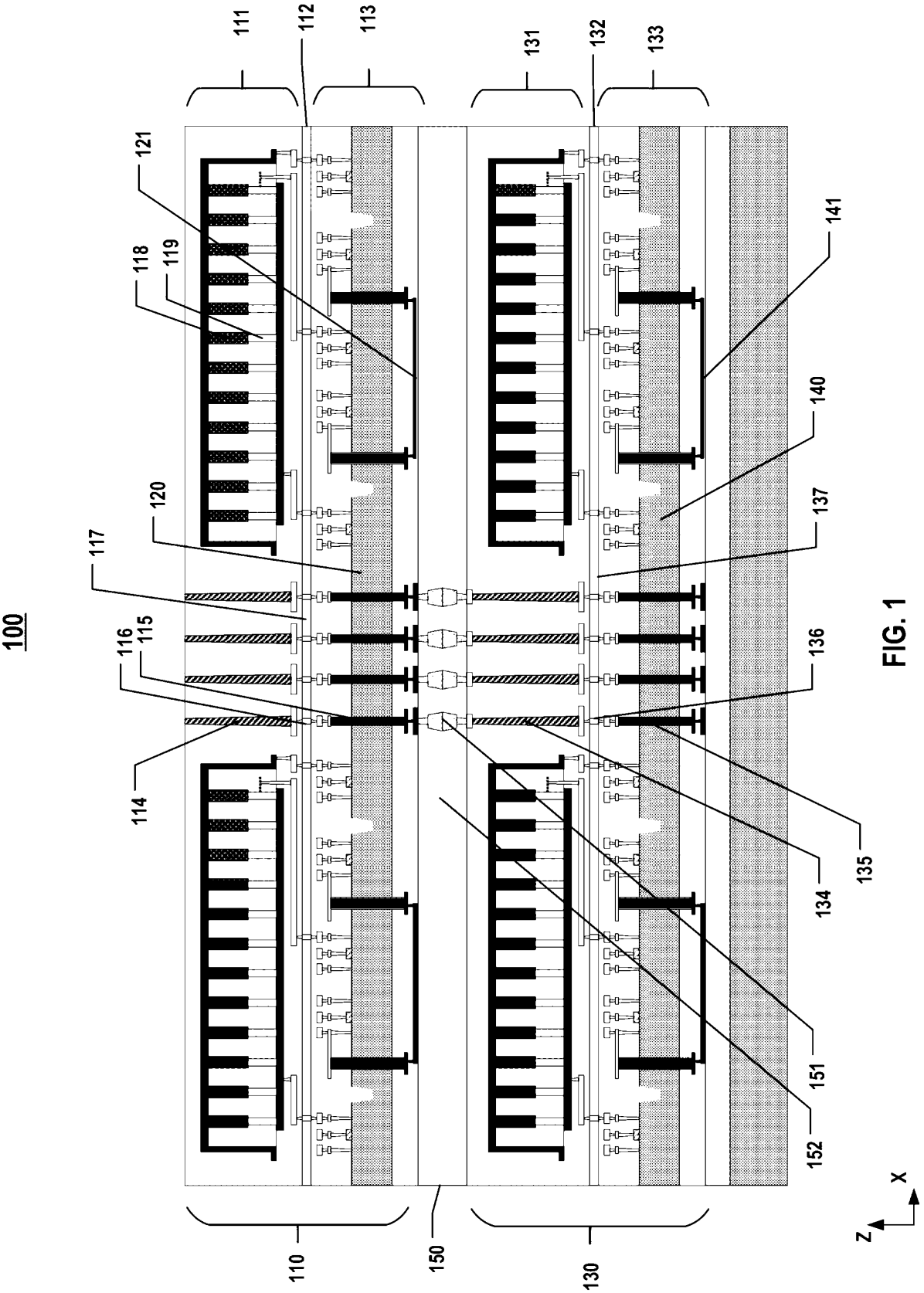

100
111
112
113
131
132
133
121
118
119
141
140
120
137
117
116
115
136
114
135
134
151
152
110
150
130
X
Z

FIG. 1

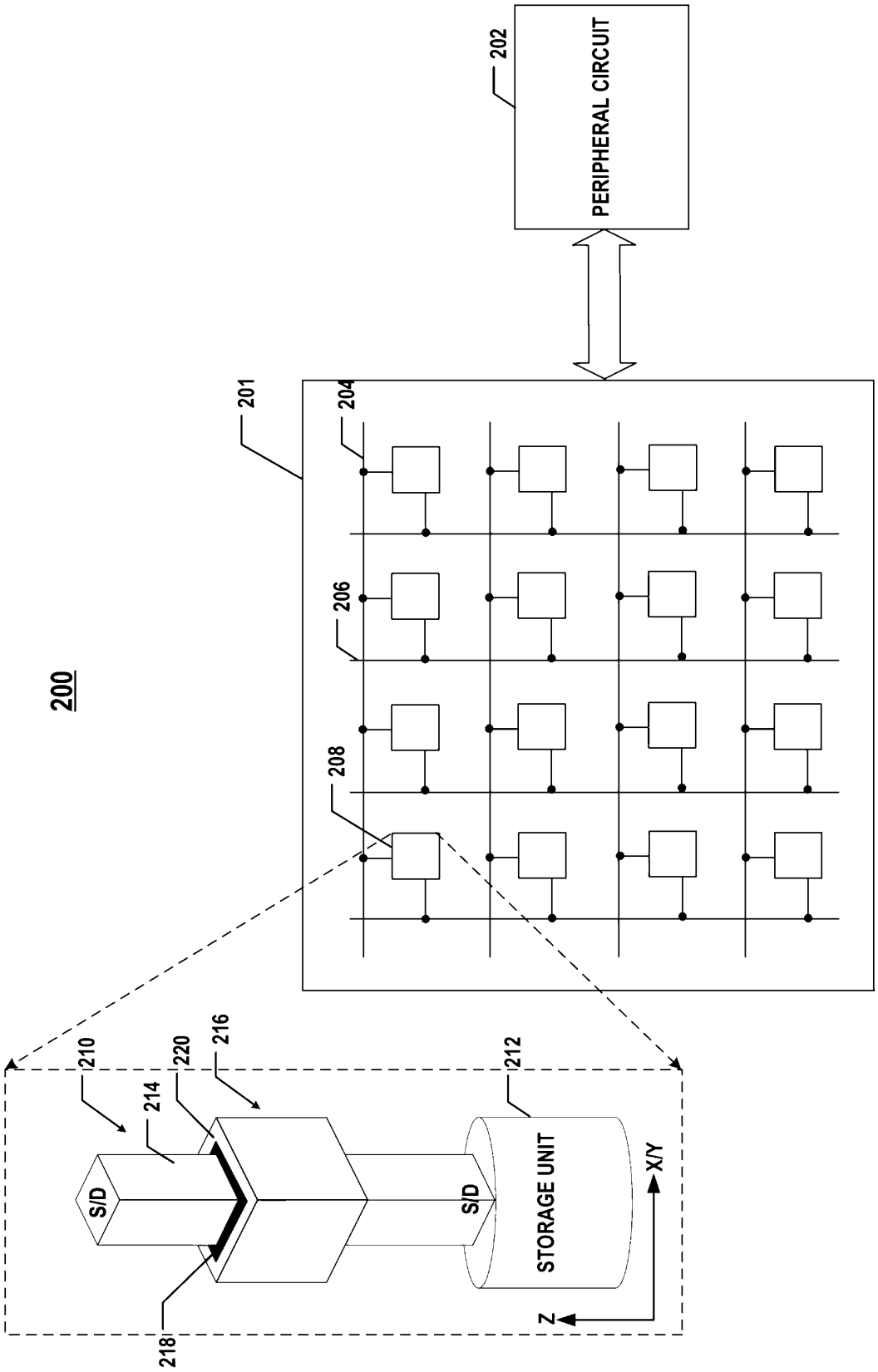

200
202
PERIPHERAL CIRCUIT
201
204
206
208
210
220
216
212
214
S/D
S/D
STORAGE UNIT
X/Y
Z
218

FIG. 2

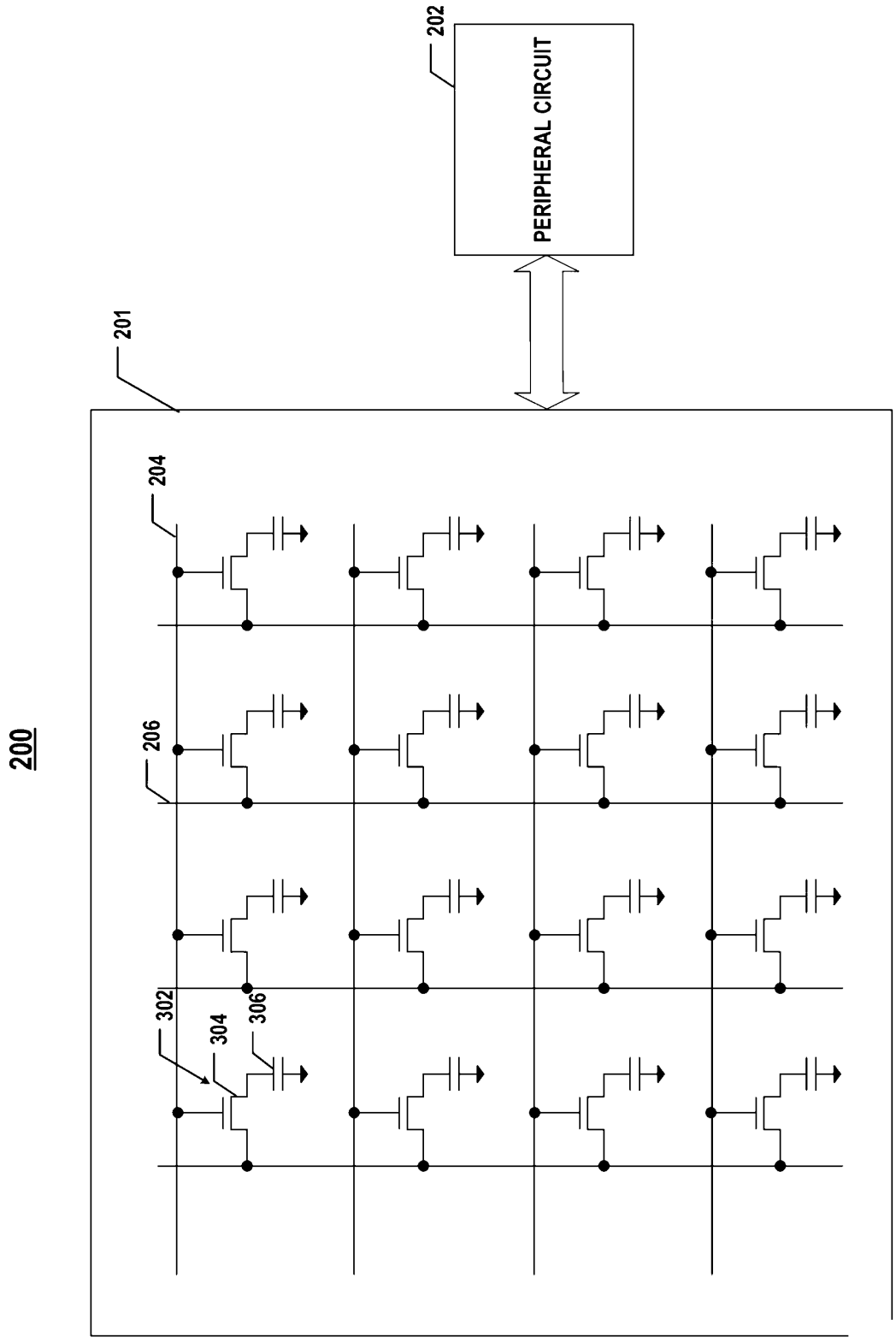


FIG. 3

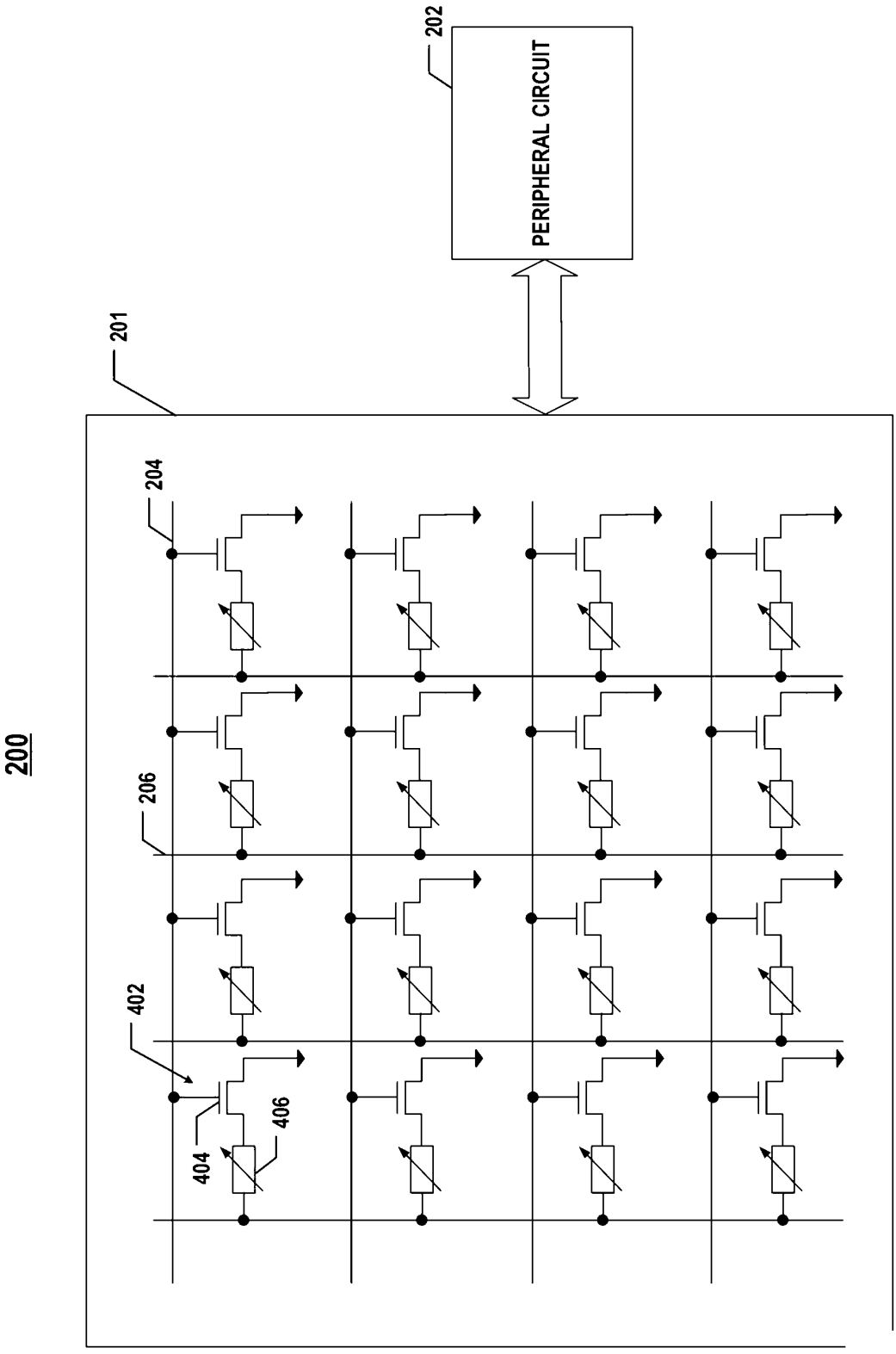


FIG. 4

500

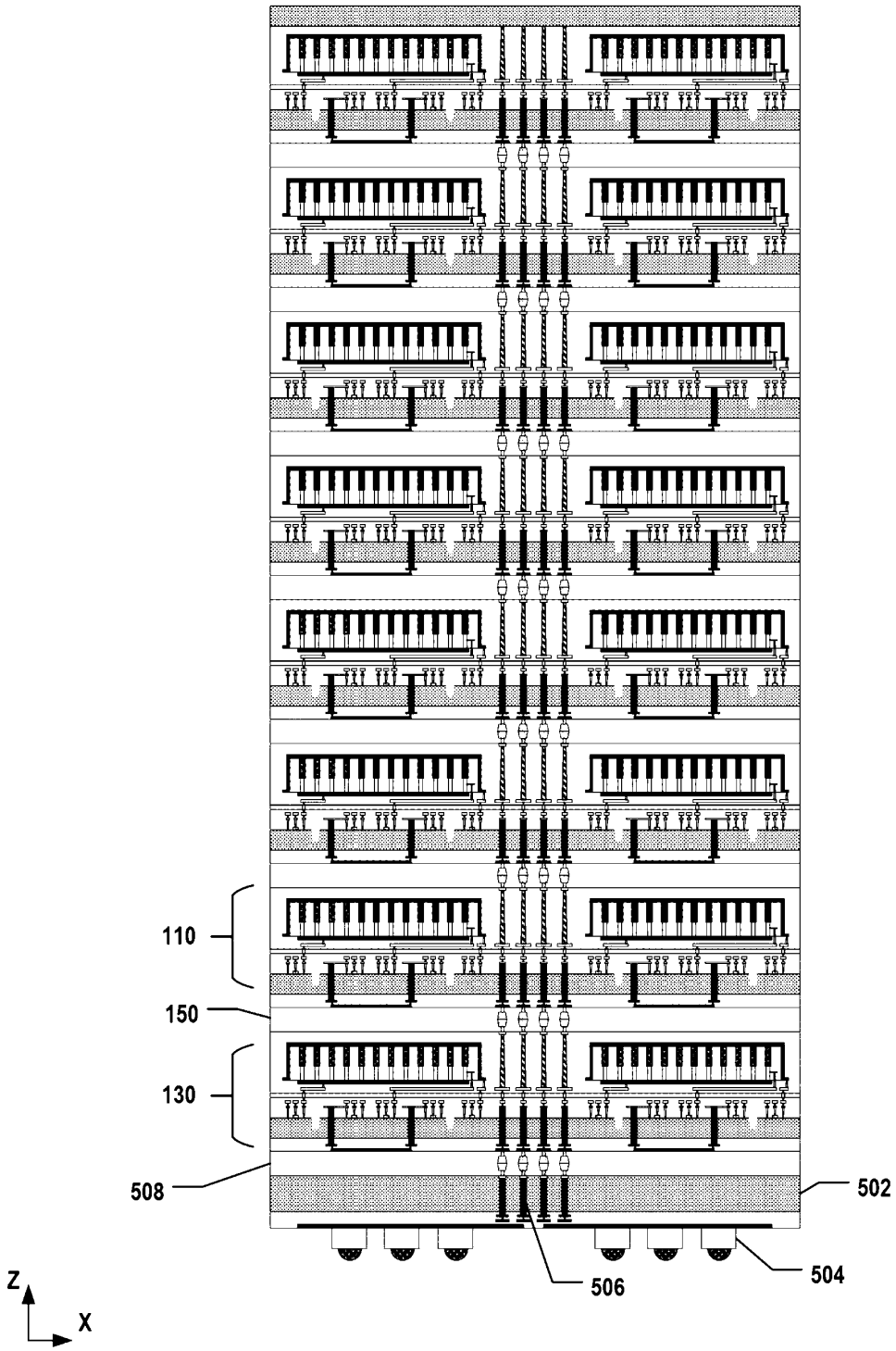


FIG. 5

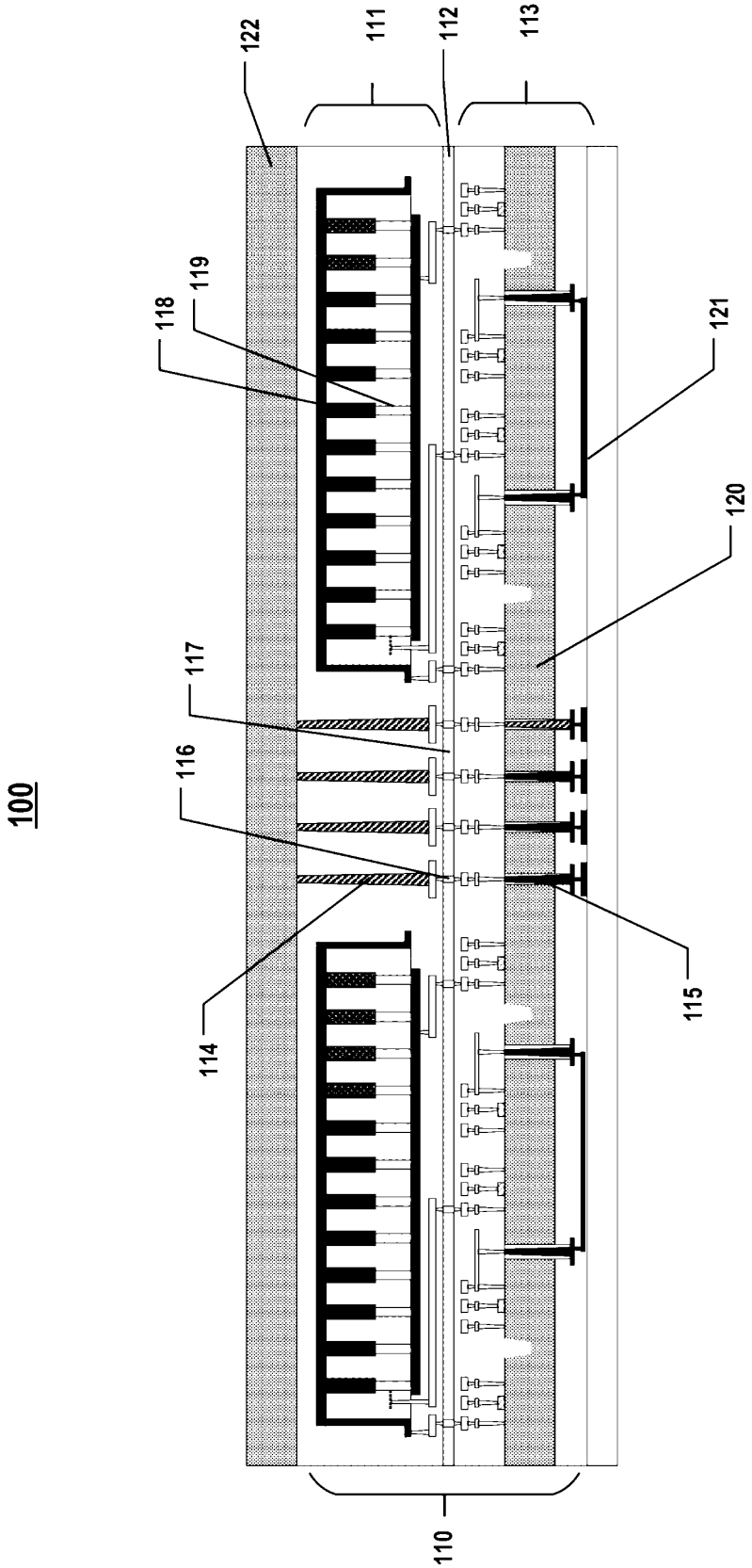


FIG. 6

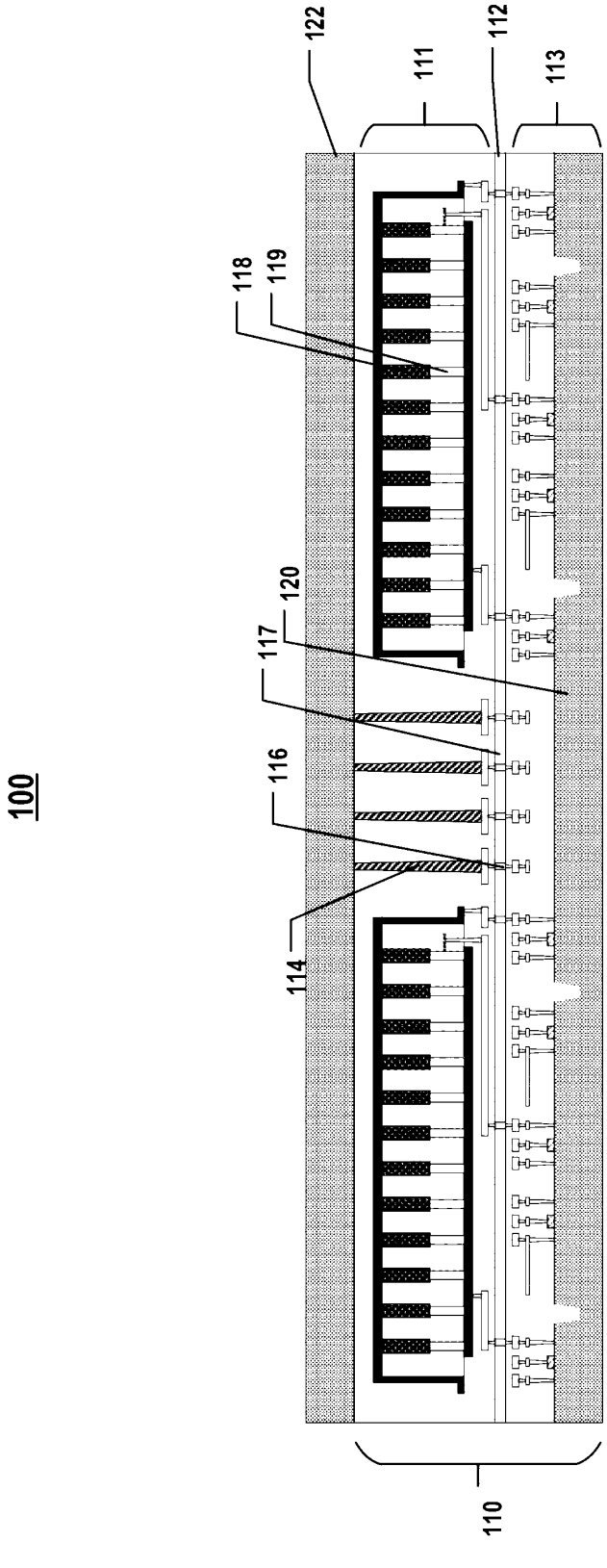


FIG. 7

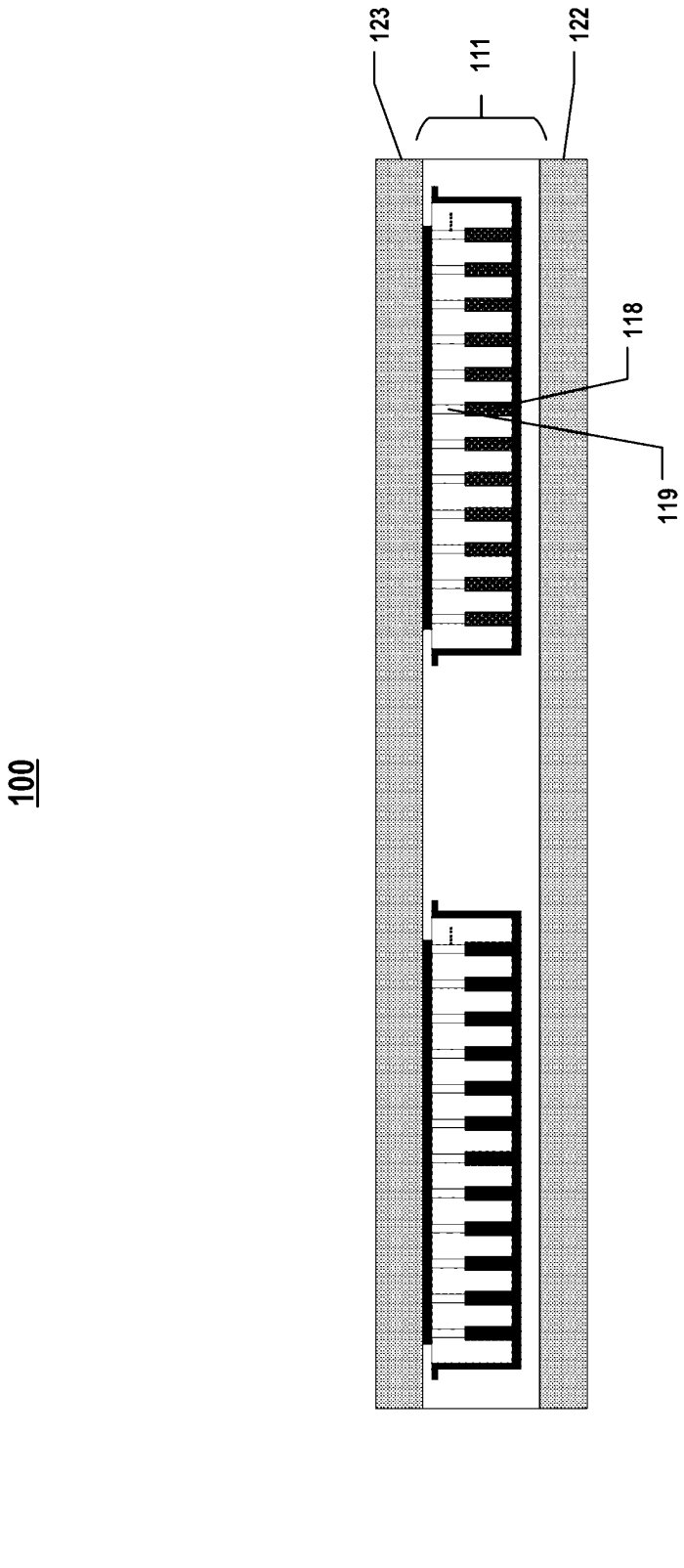


FIG. 8

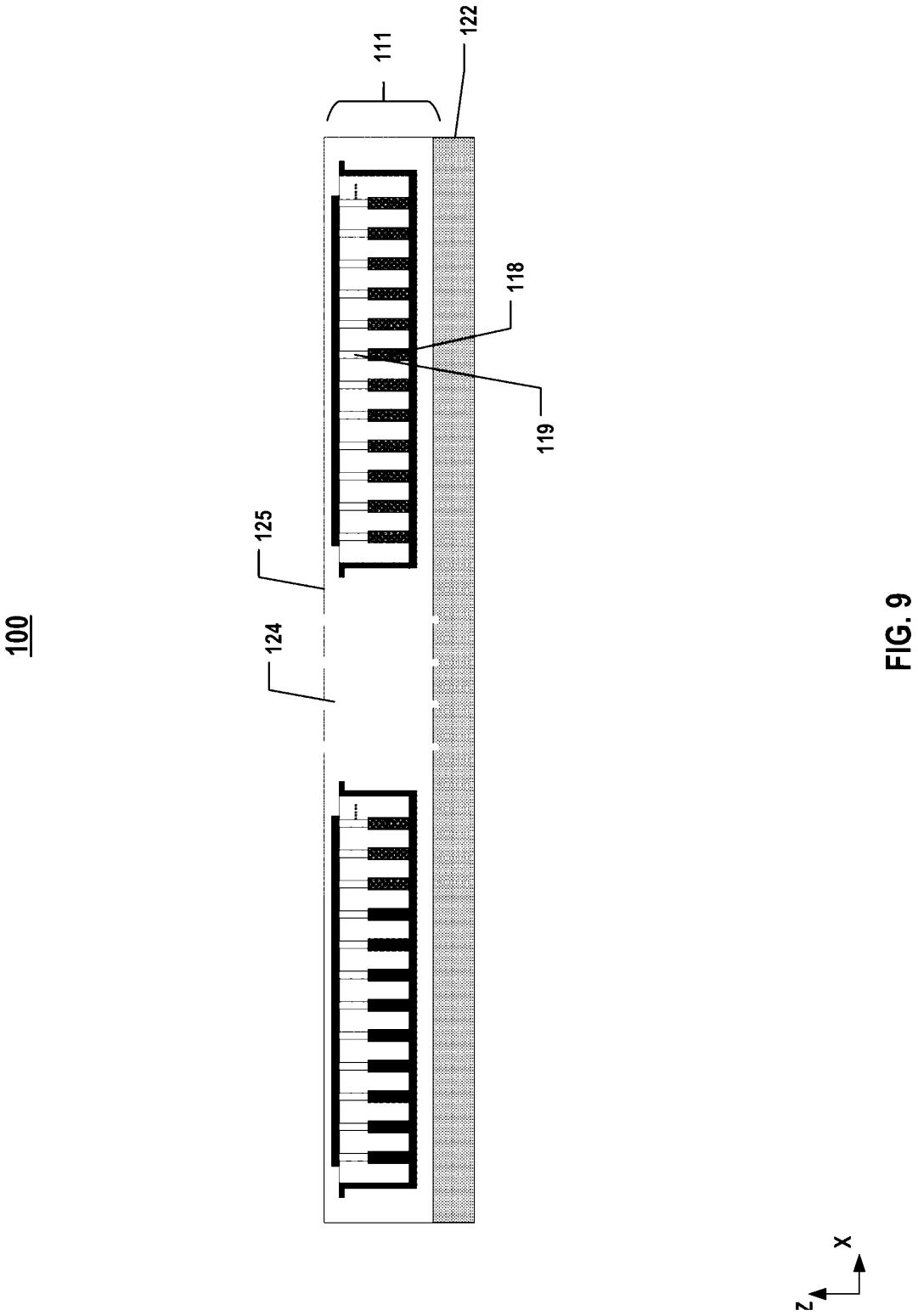


FIG. 9

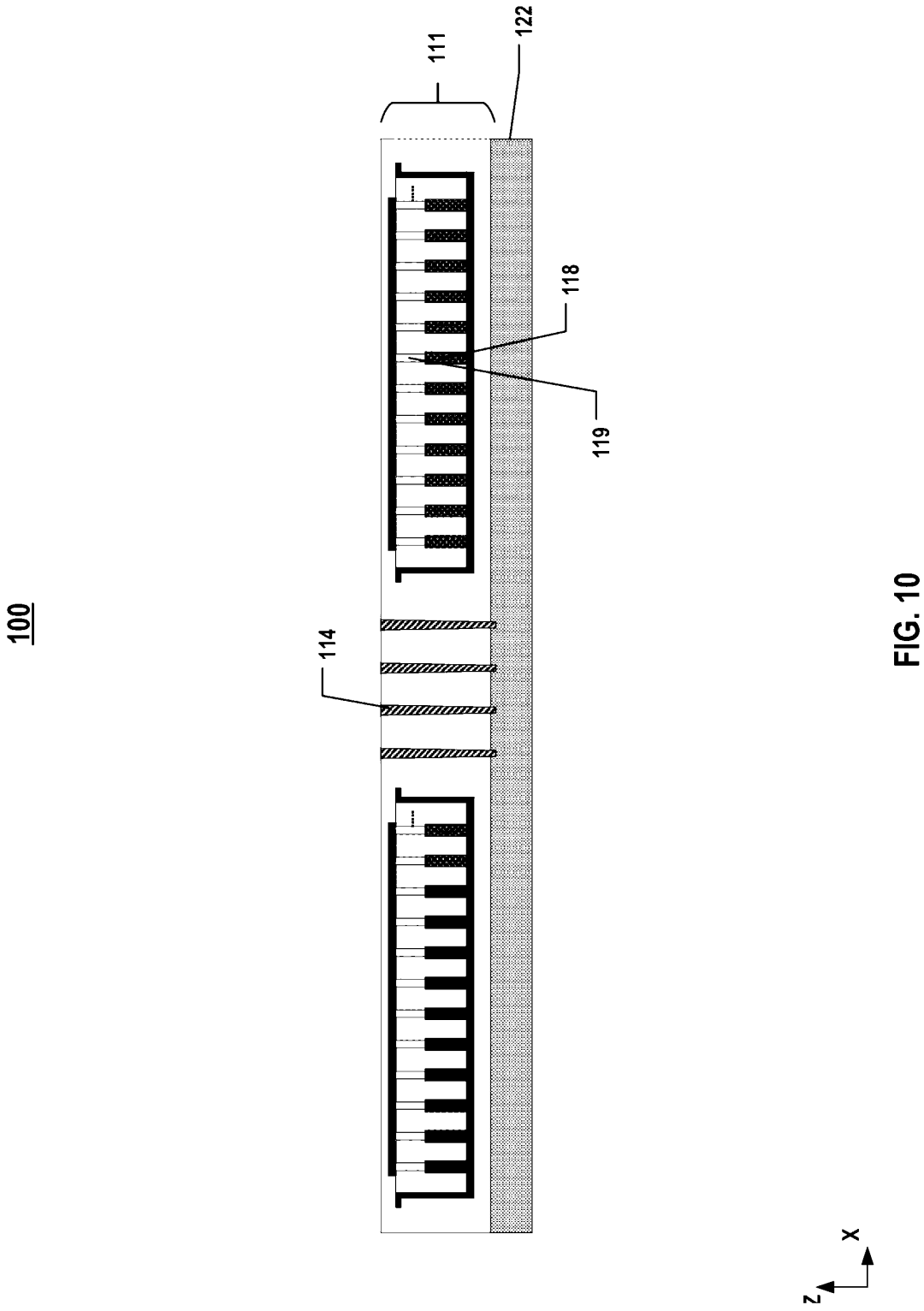


FIG. 10

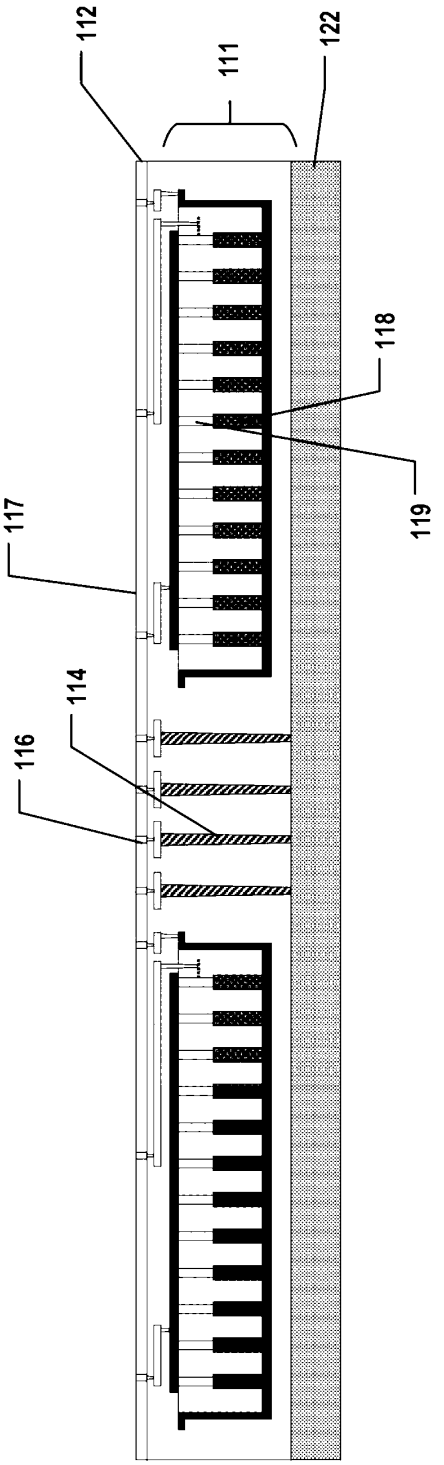


FIG. 11

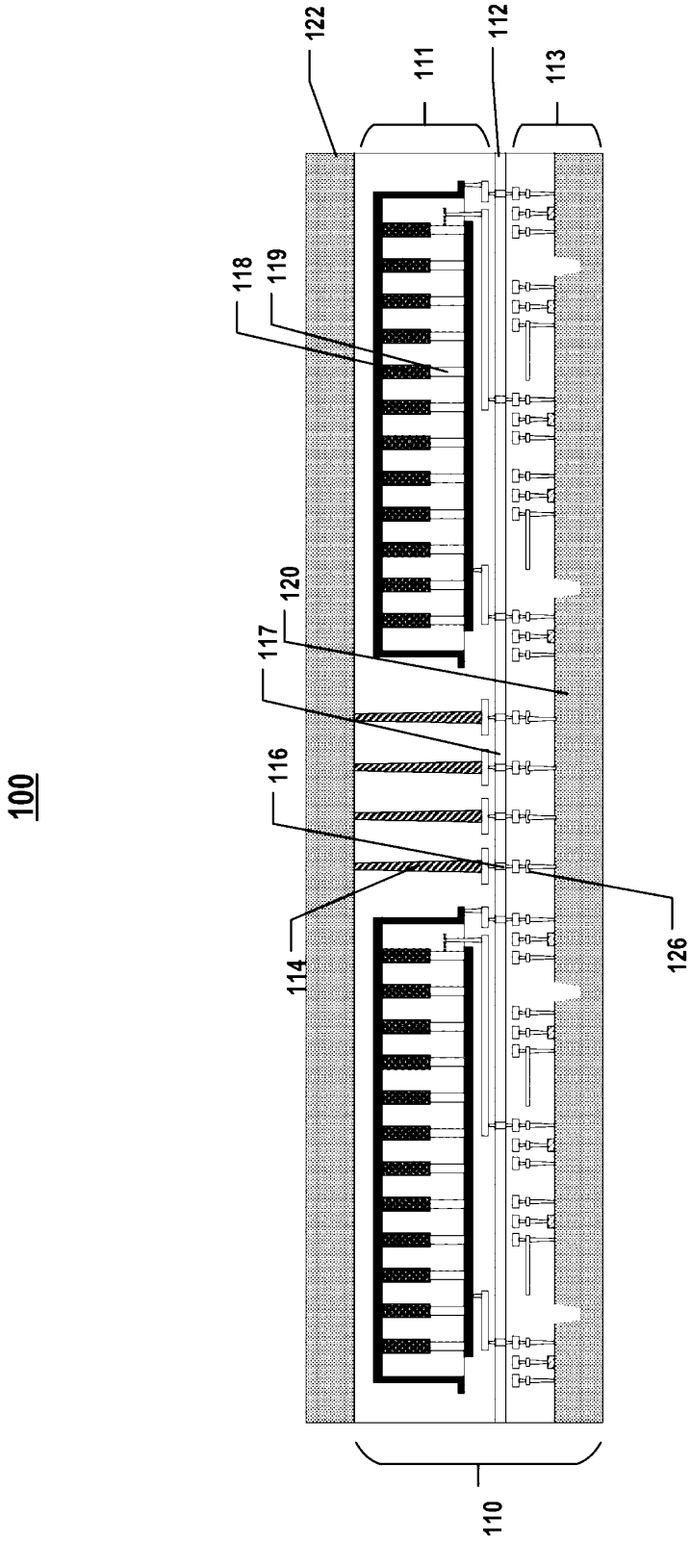


FIG. 12

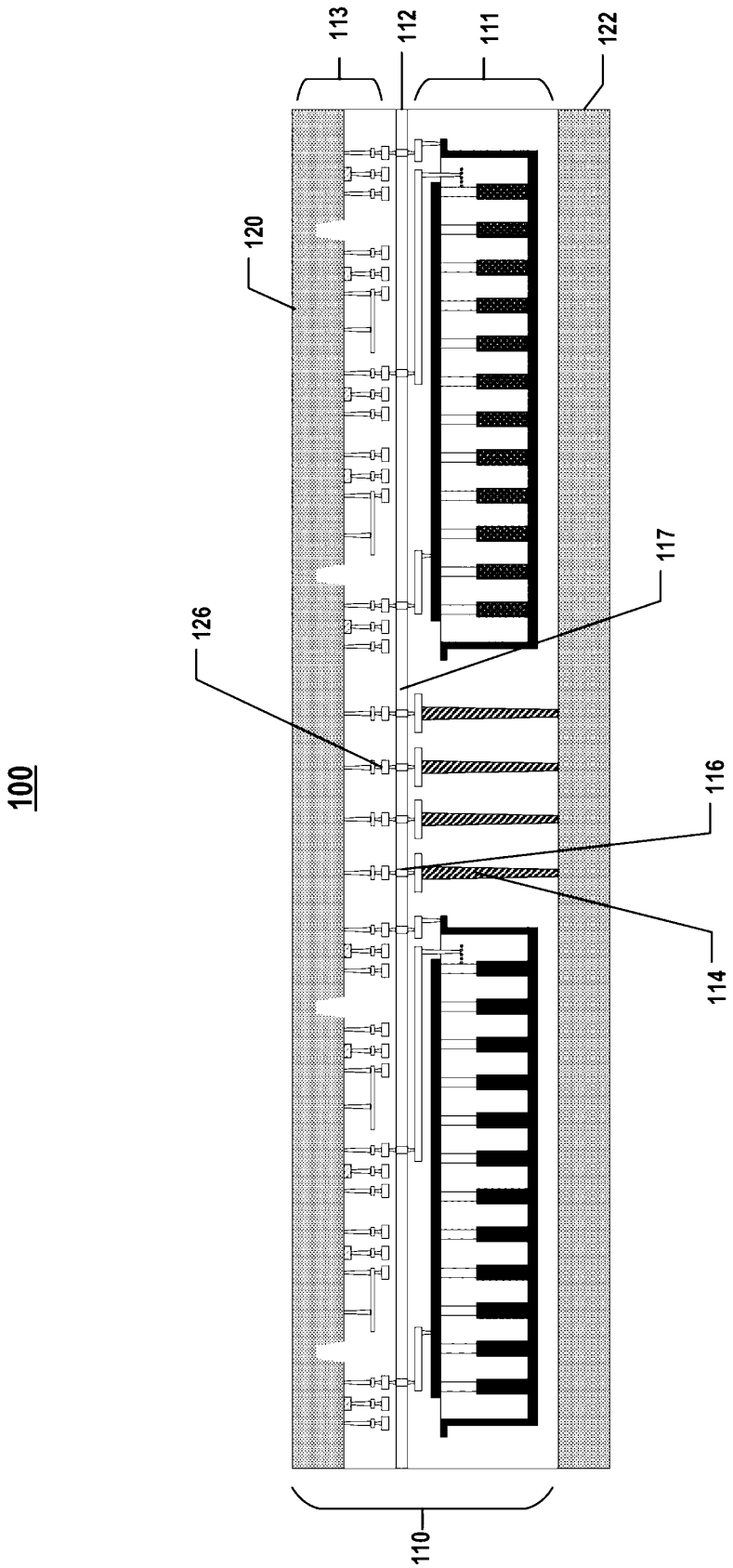


FIG. 13

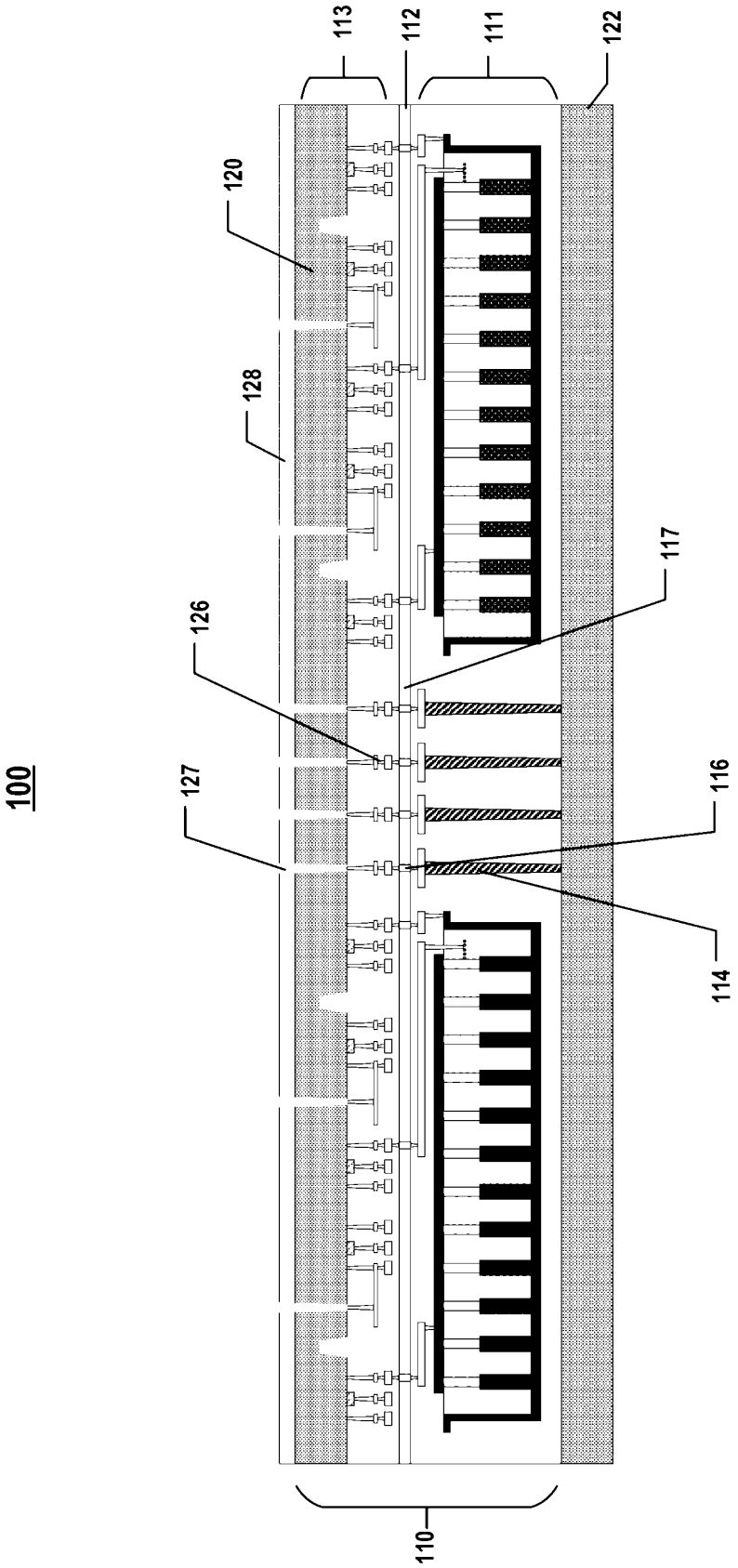


FIG. 14

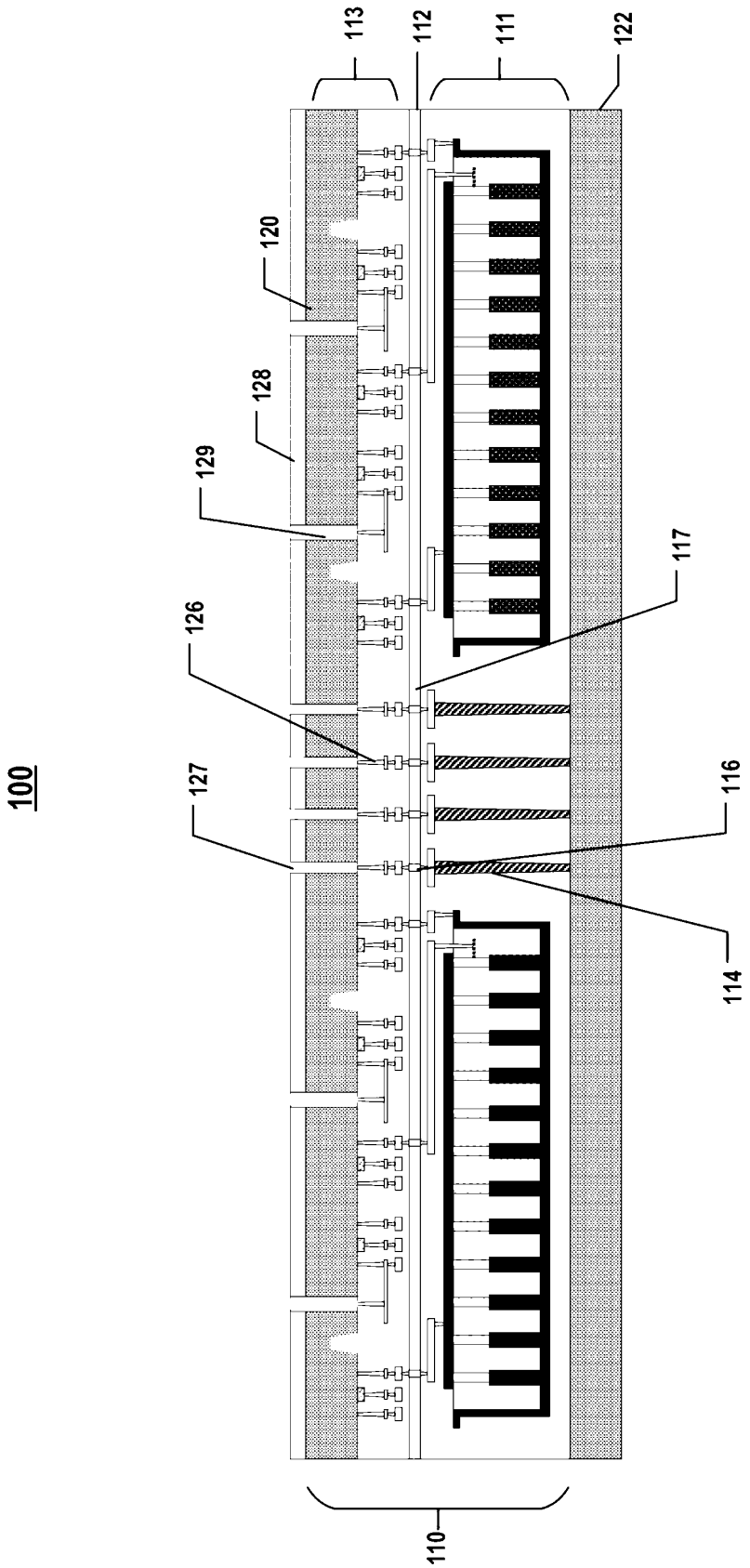


FIG. 15

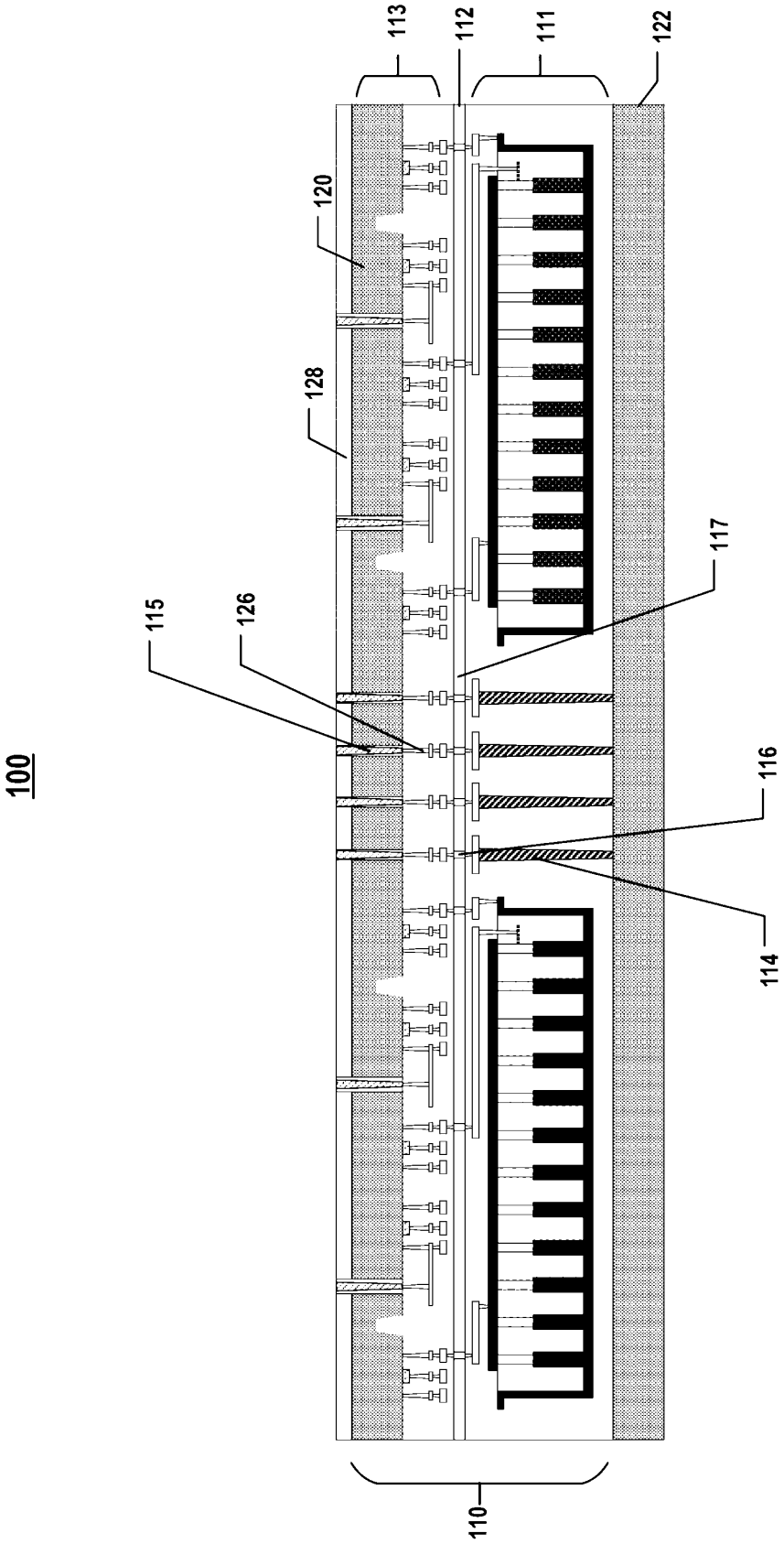


FIG. 16

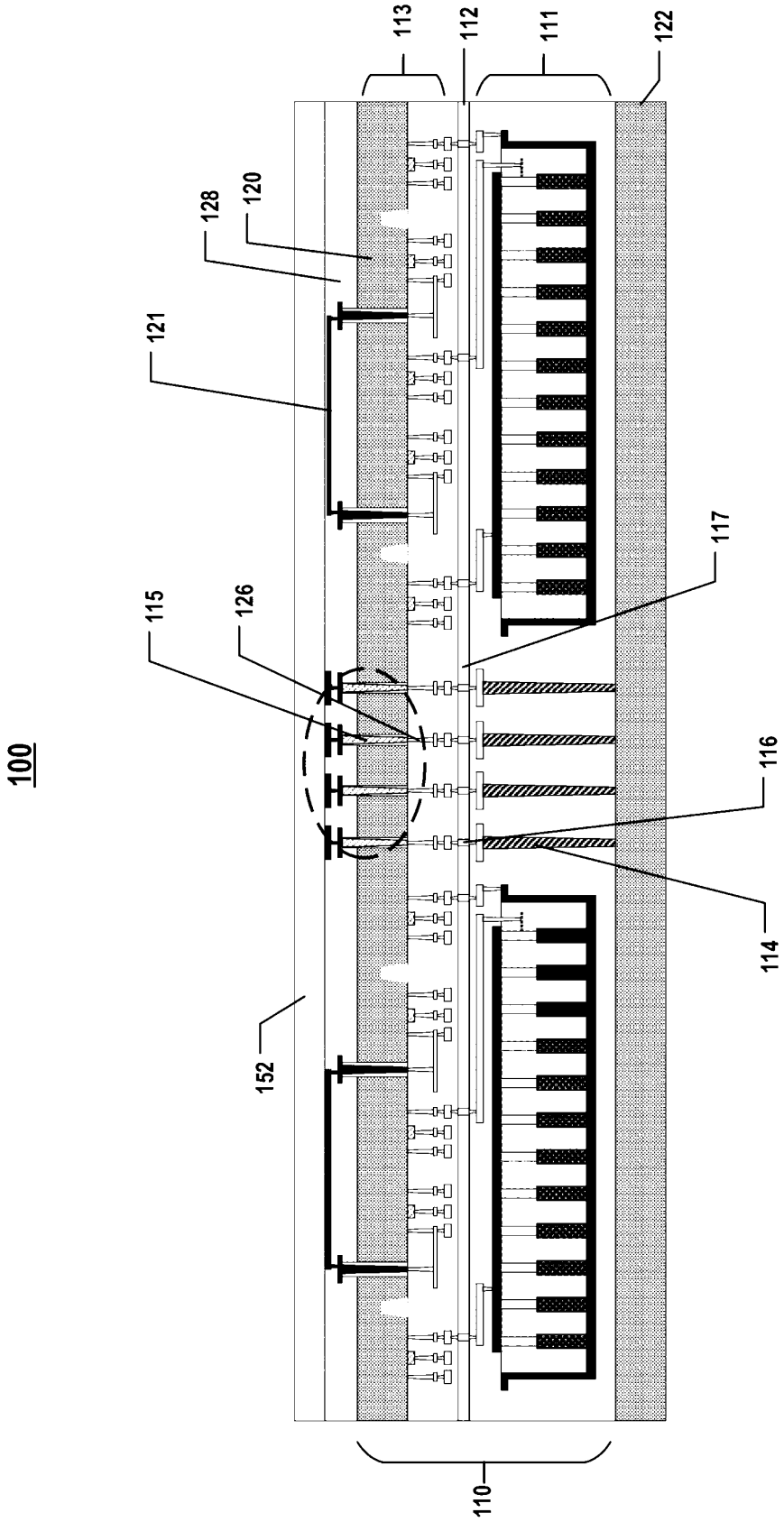


FIG. 17

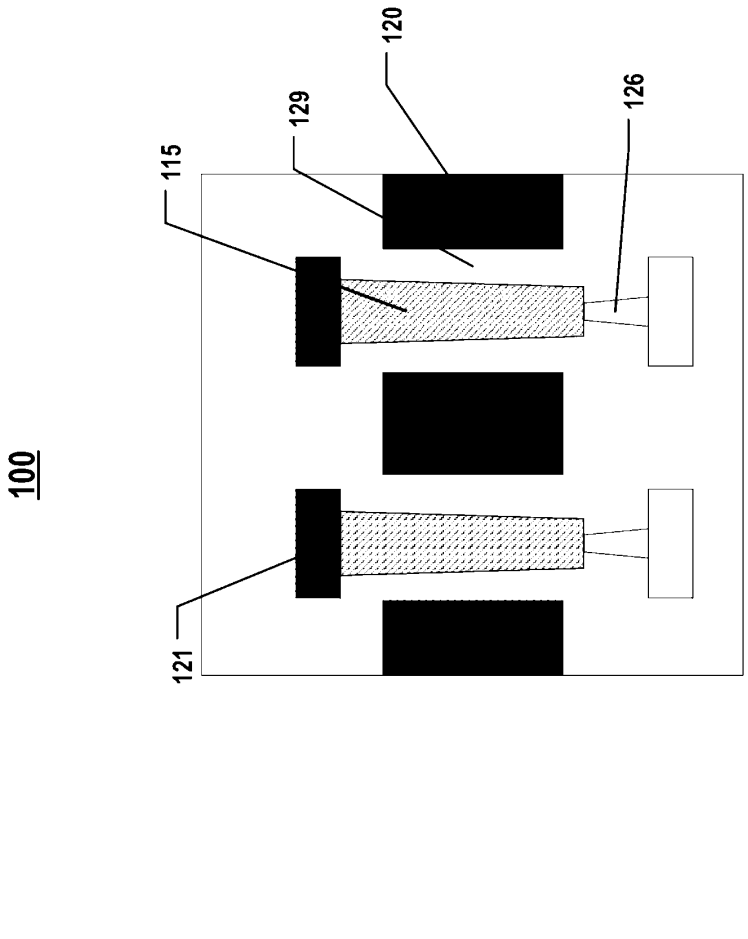


FIG. 18

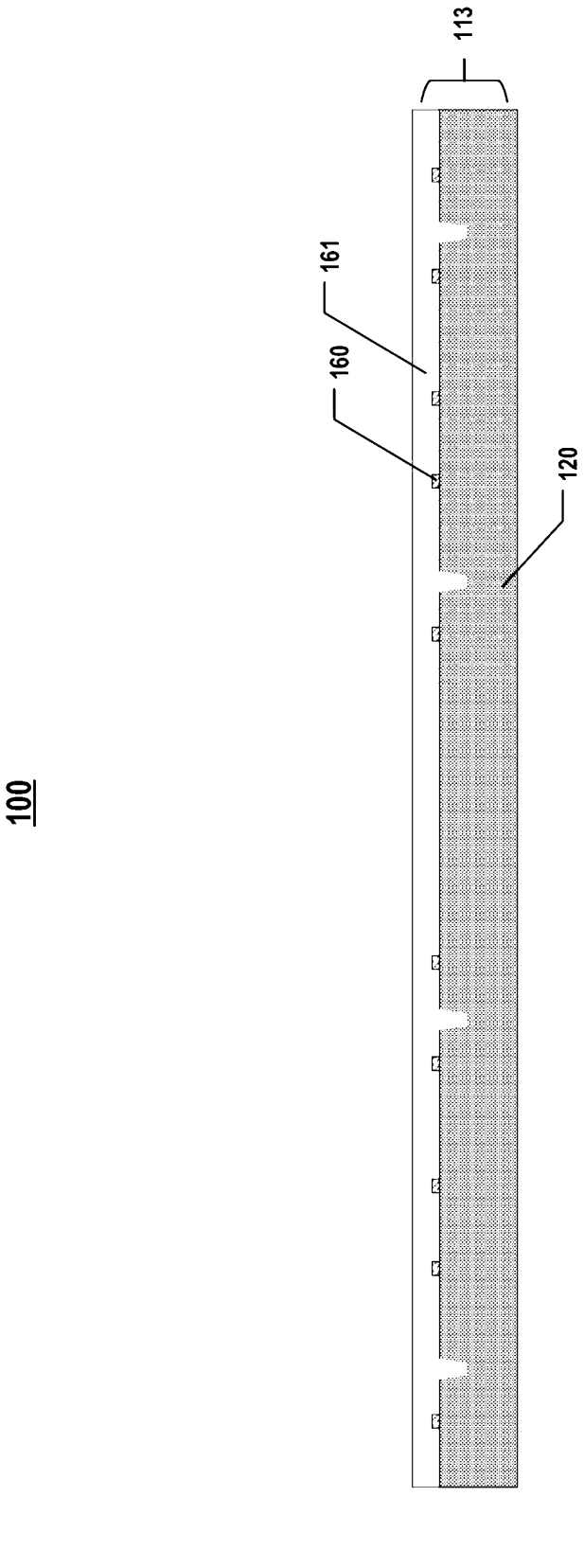


FIG. 19

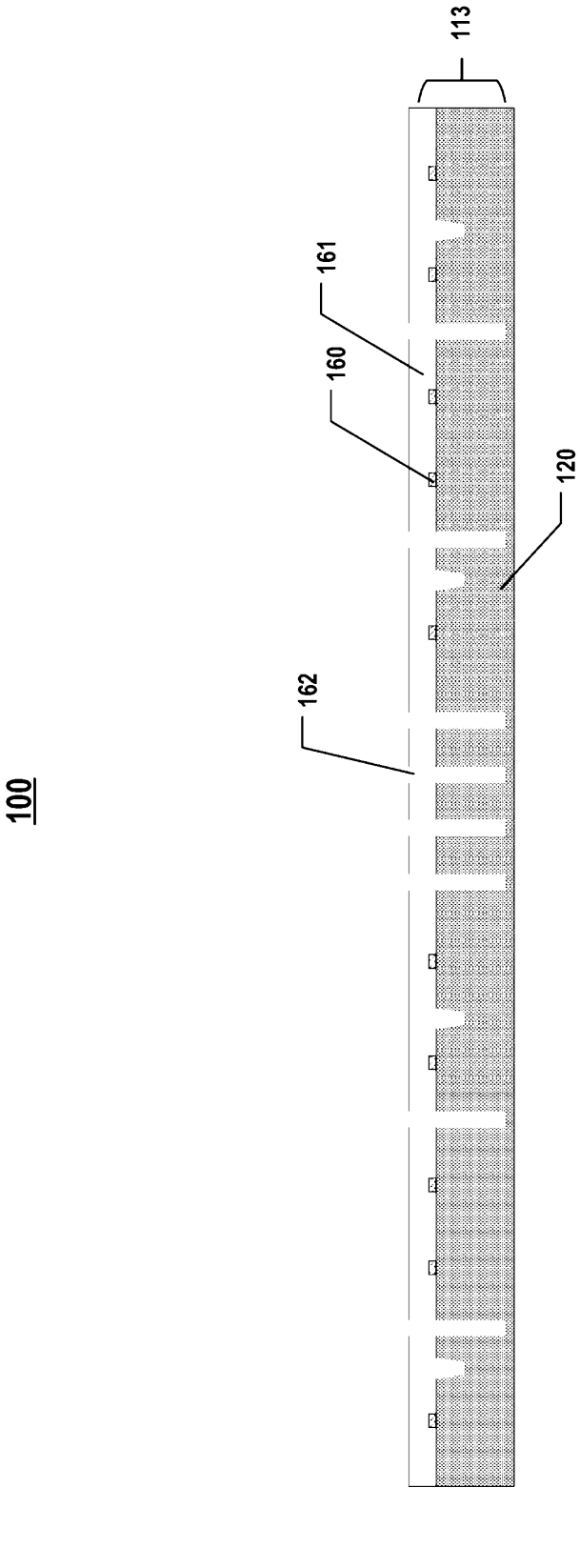


FIG. 20

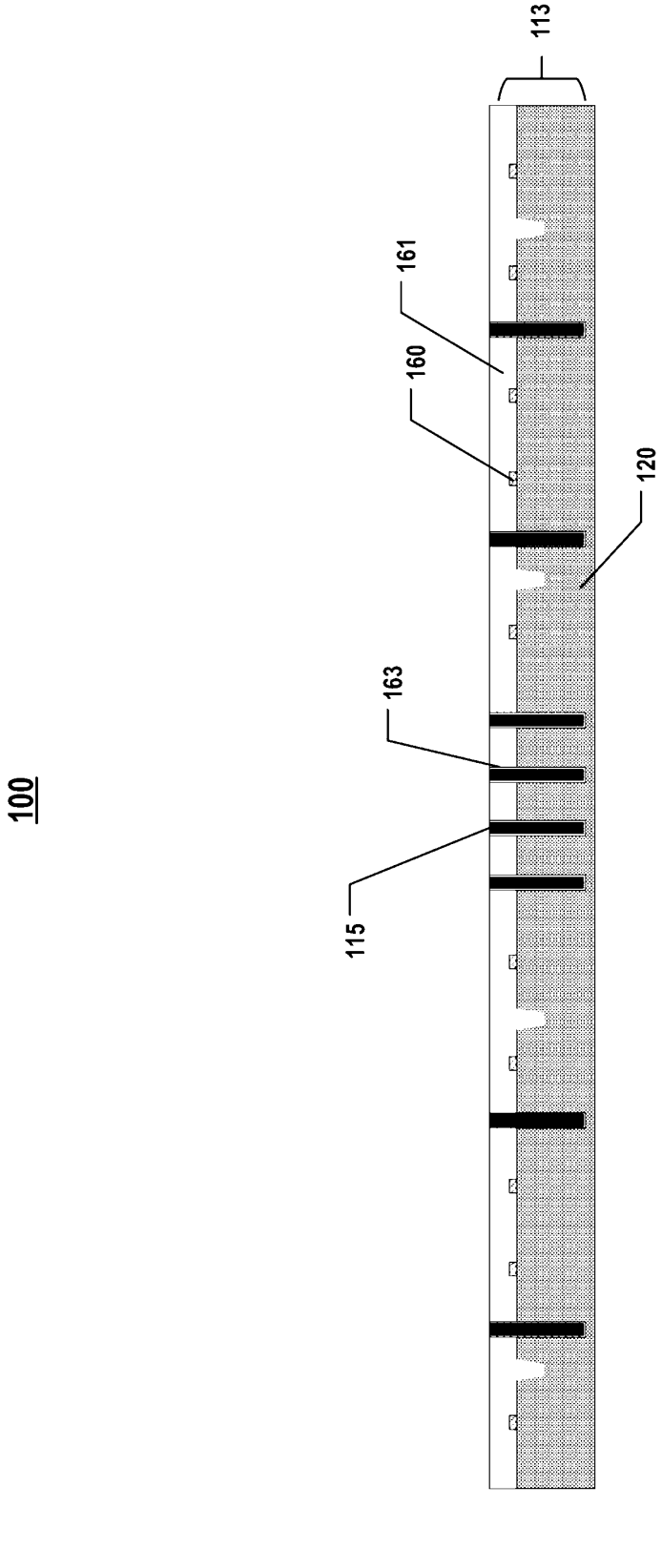


FIG. 21

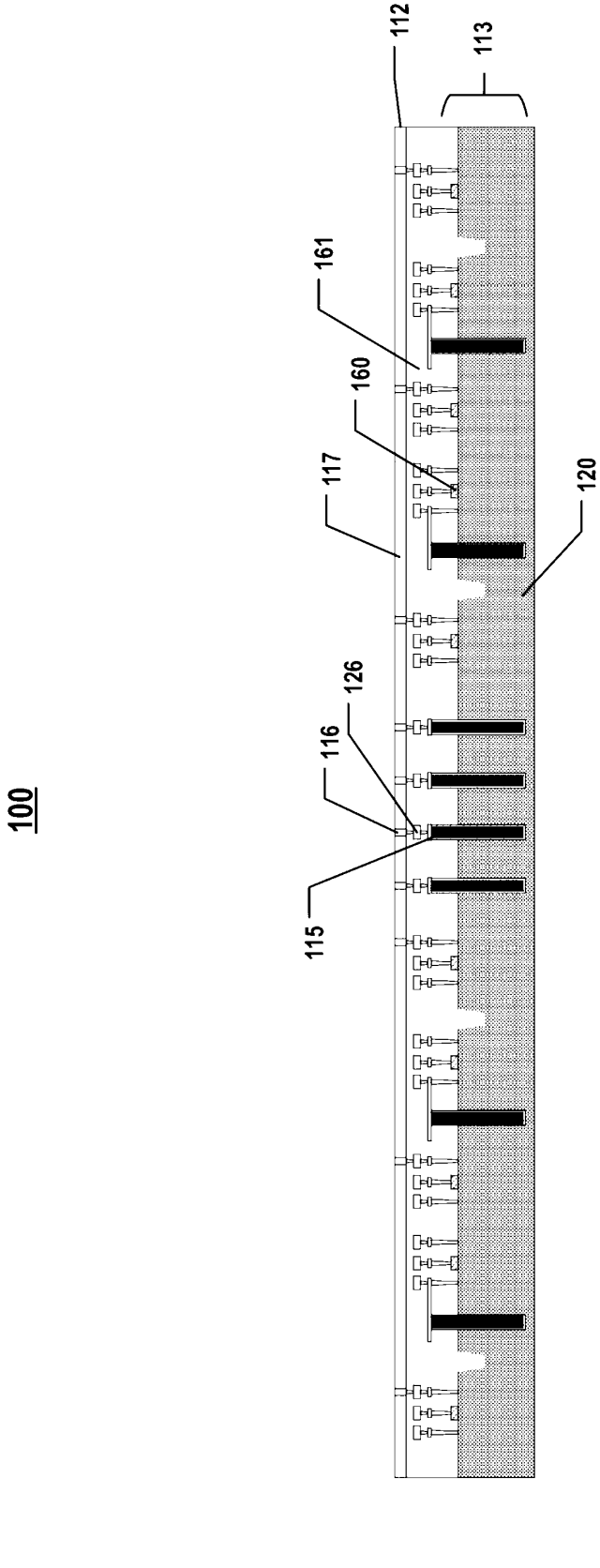


FIG. 22

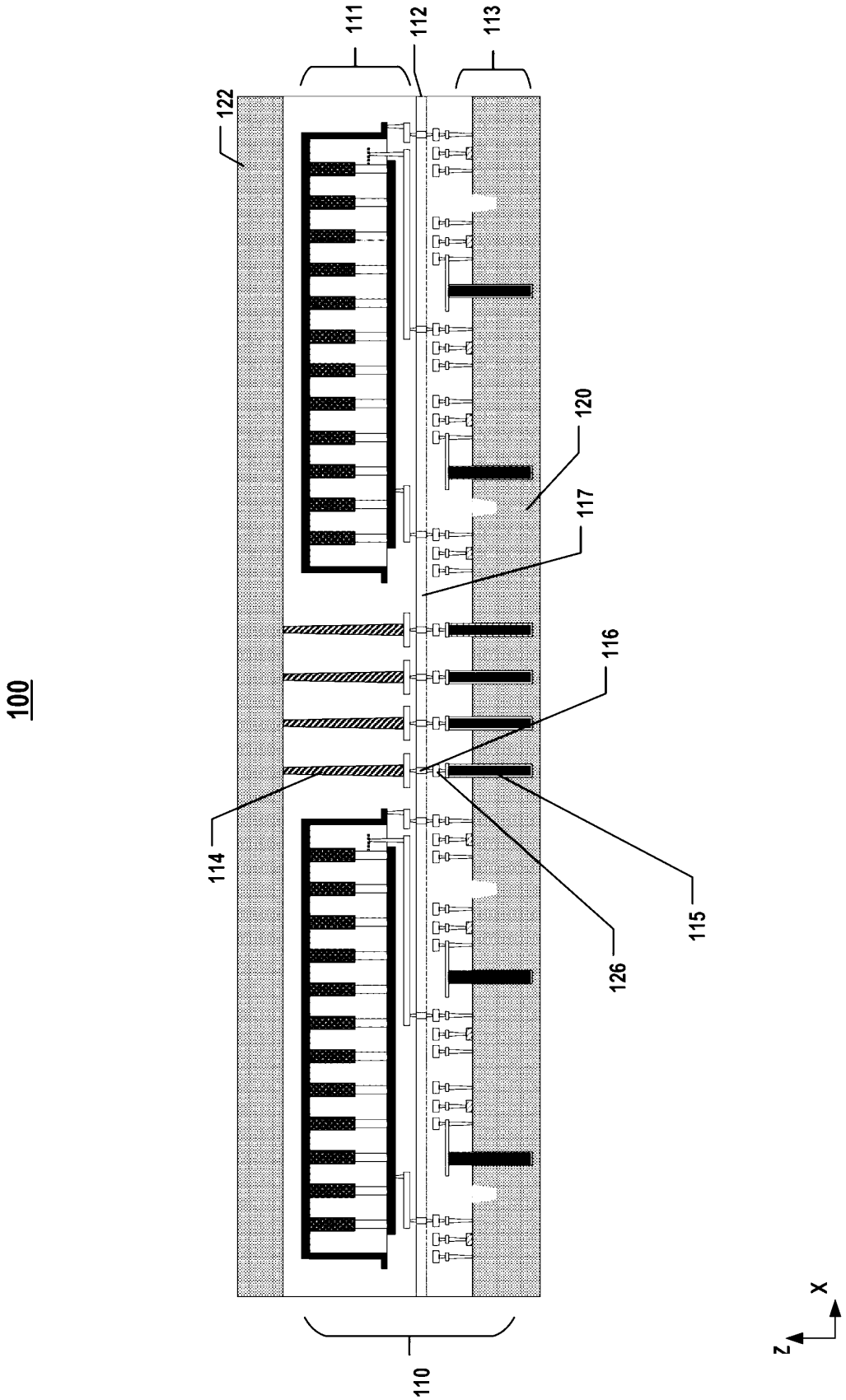


FIG. 23

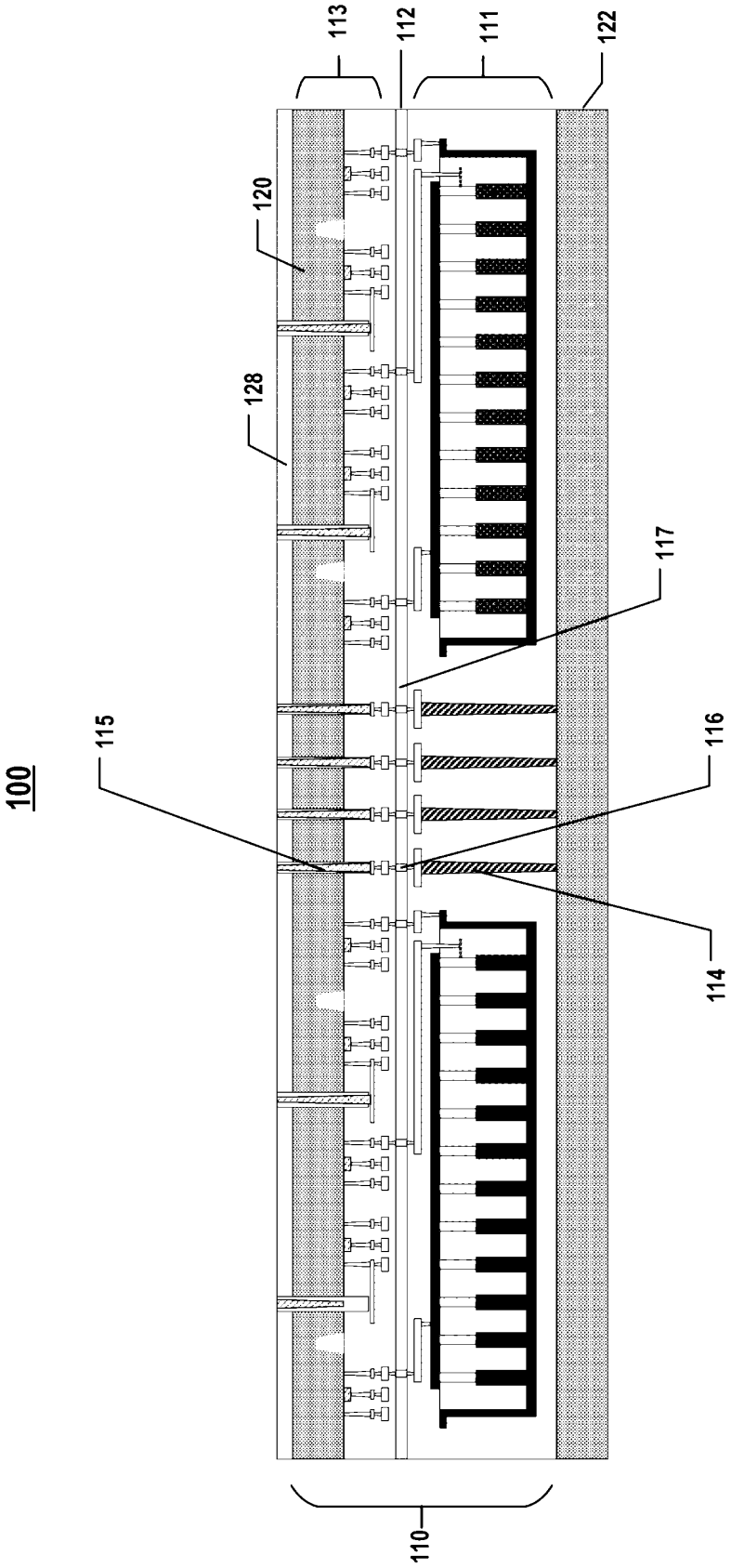


FIG. 24

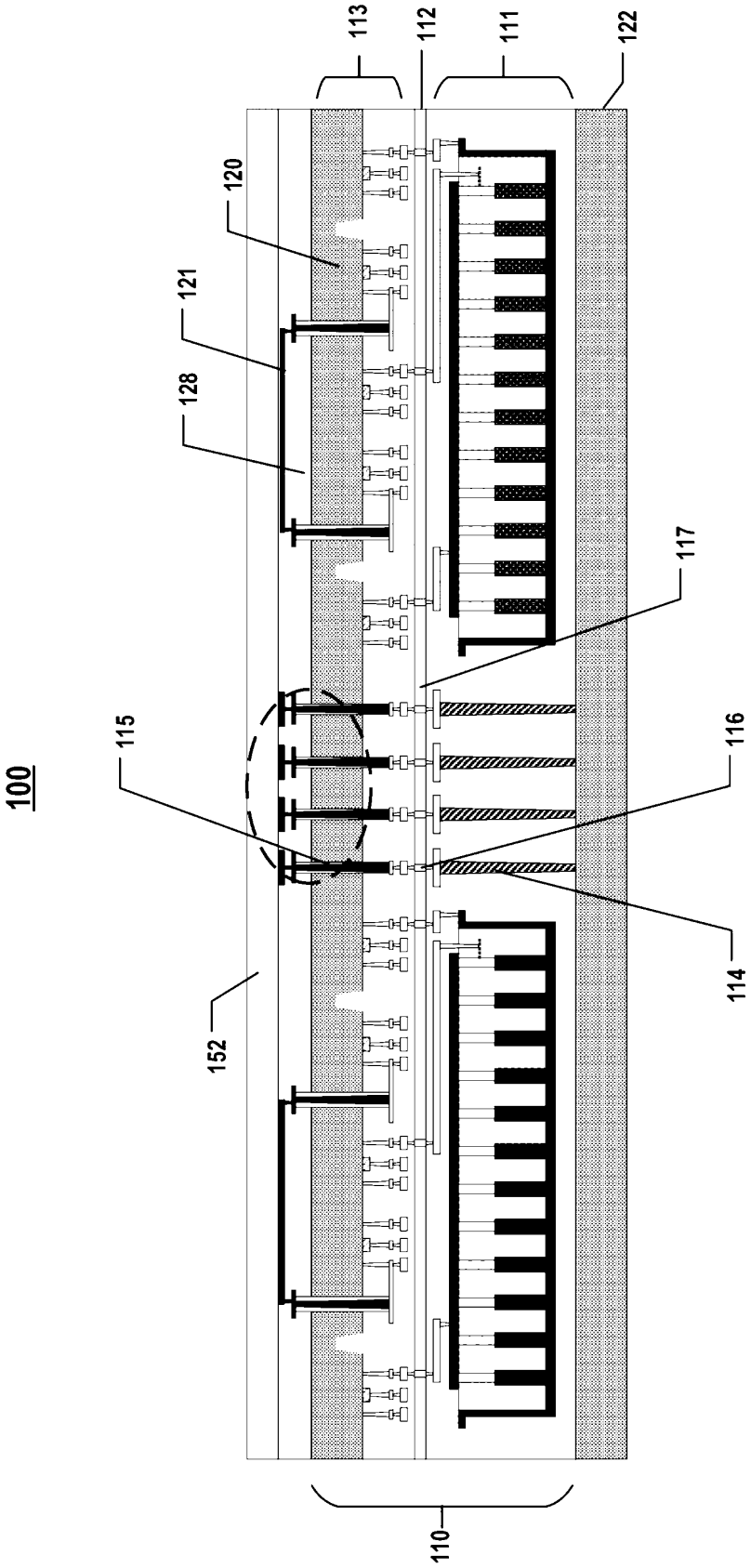


FIG. 25

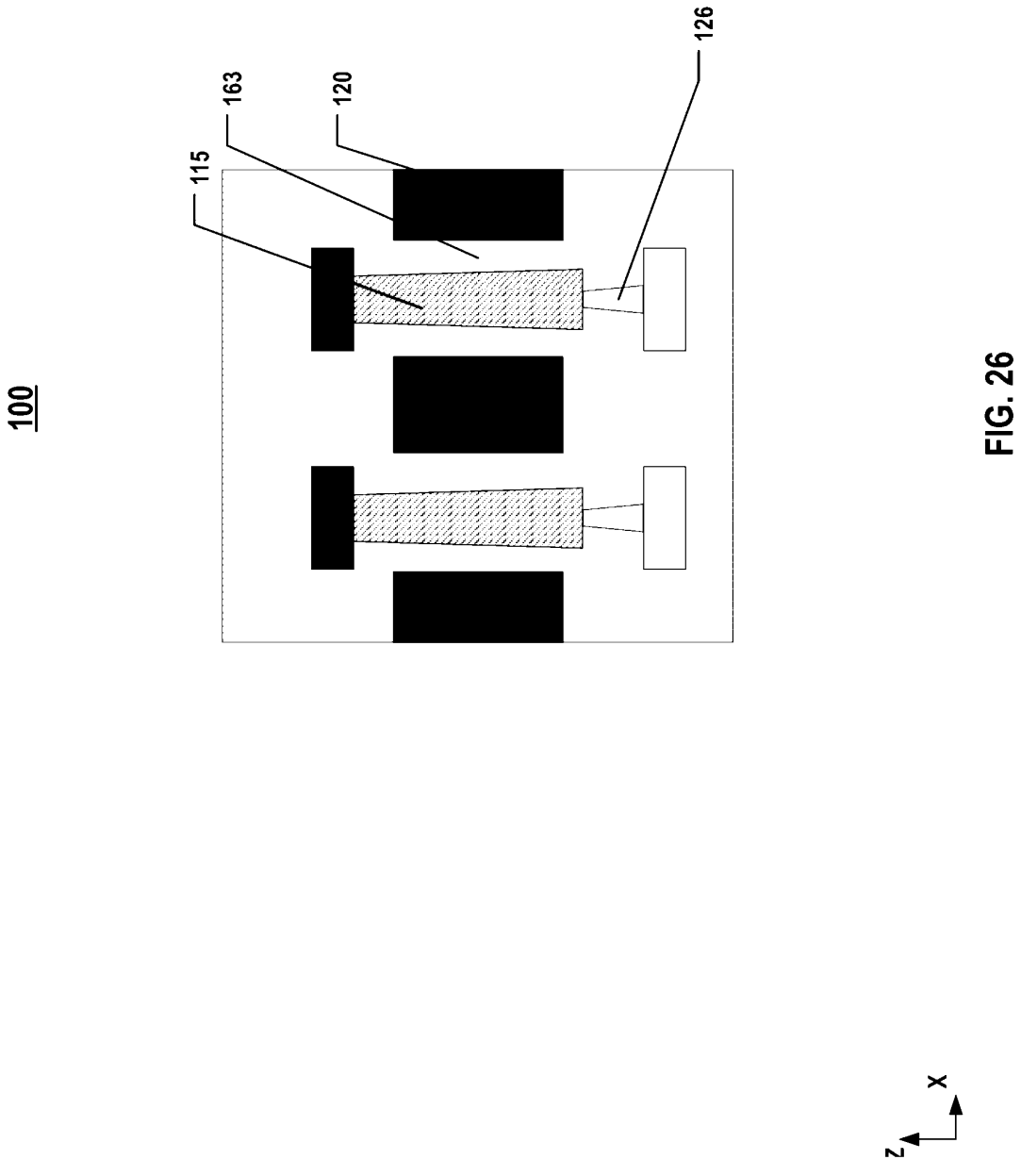


FIG. 26

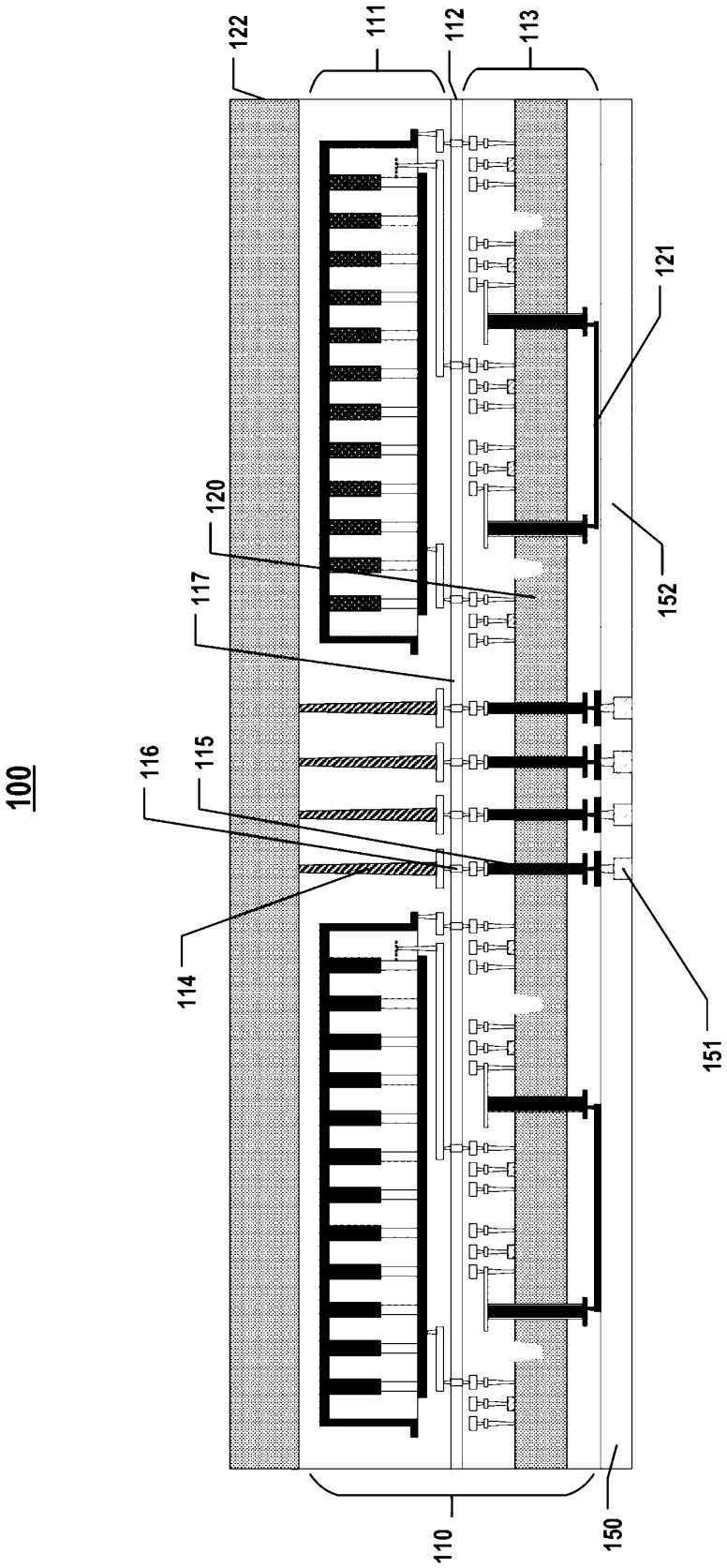


FIG. 27

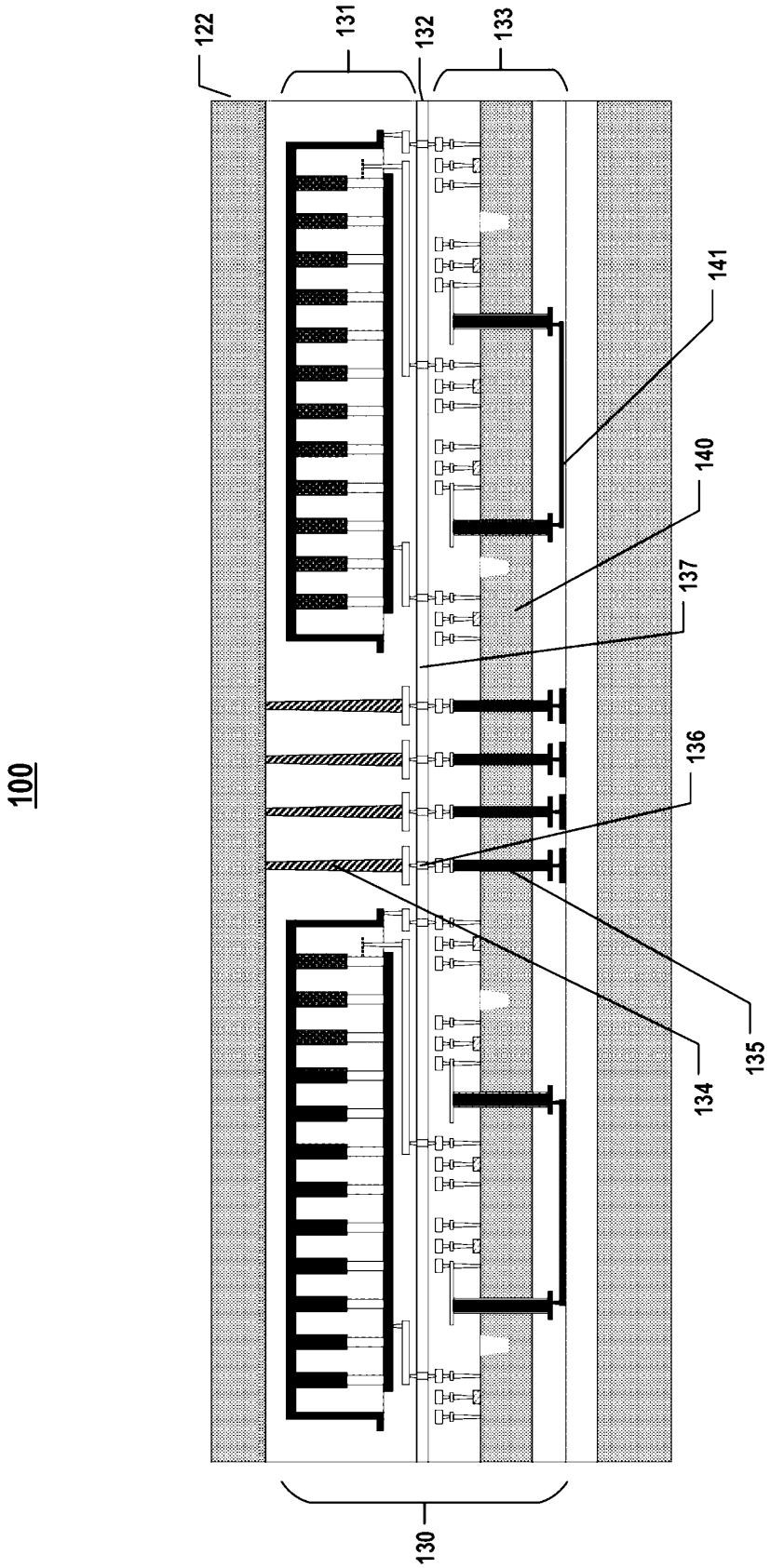


FIG. 28

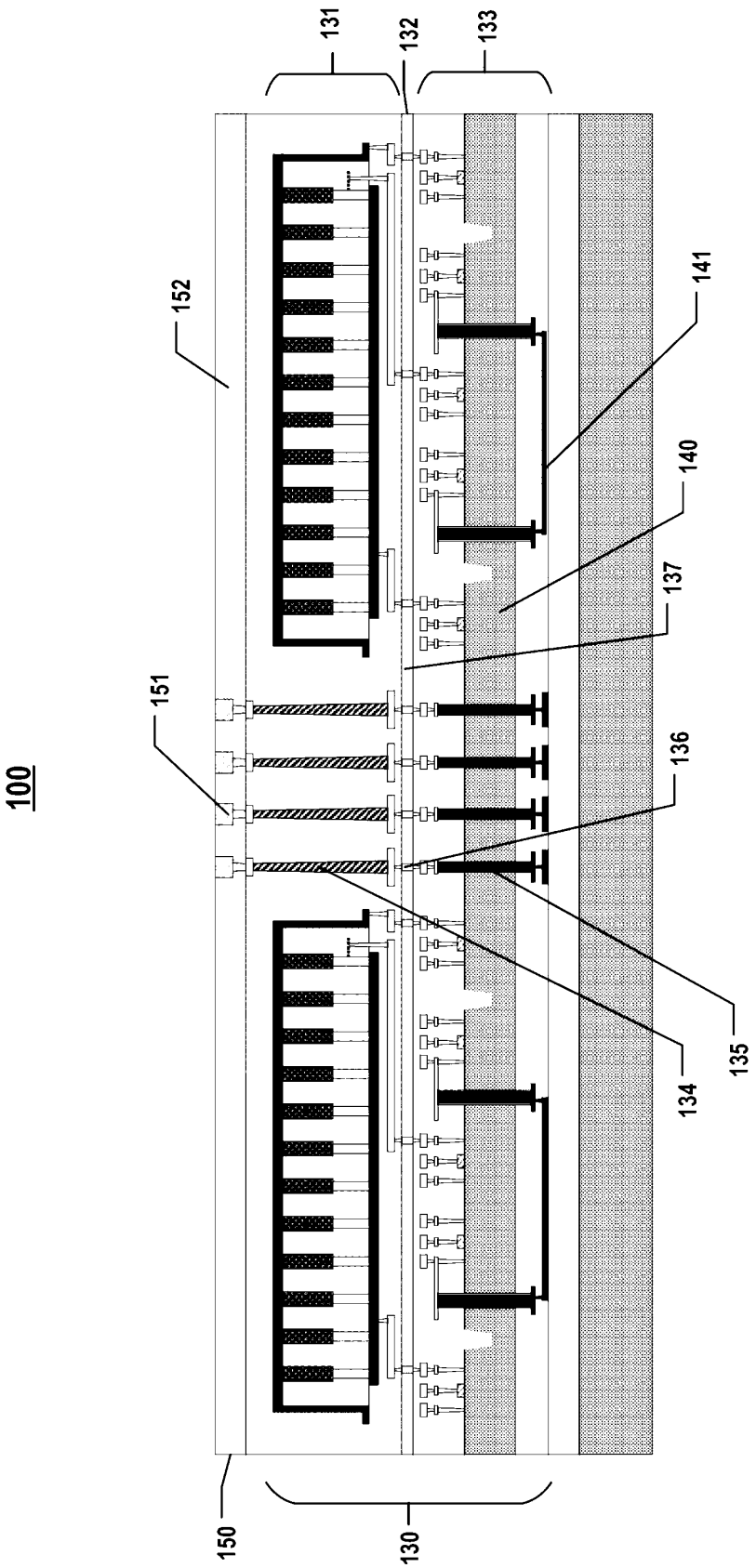


FIG. 29

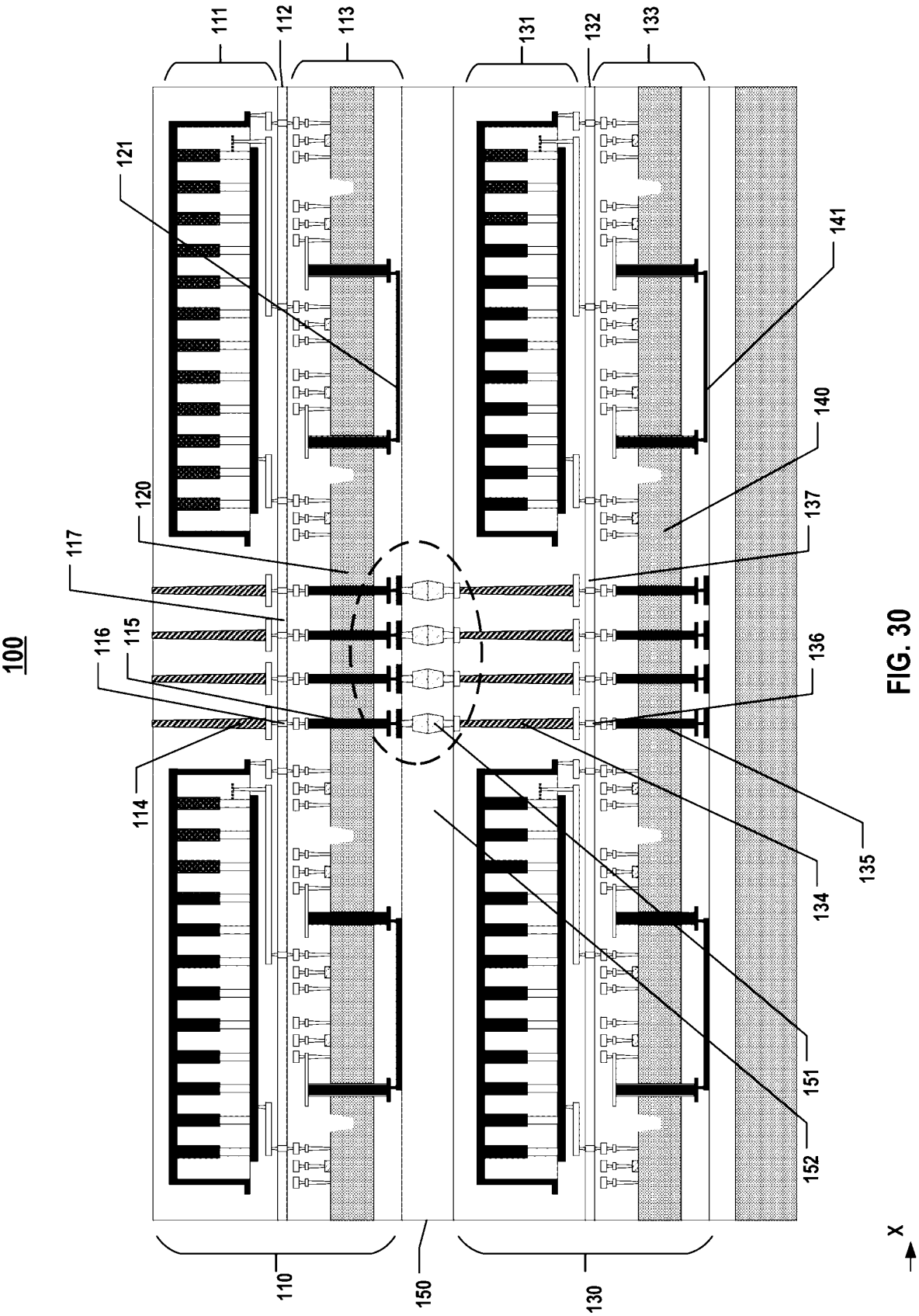

100
111
112
113
131
132
133
121
141
140
120
137
117
116
115
136
114
135
134
151
152
110
150
130
X

FIG. 30

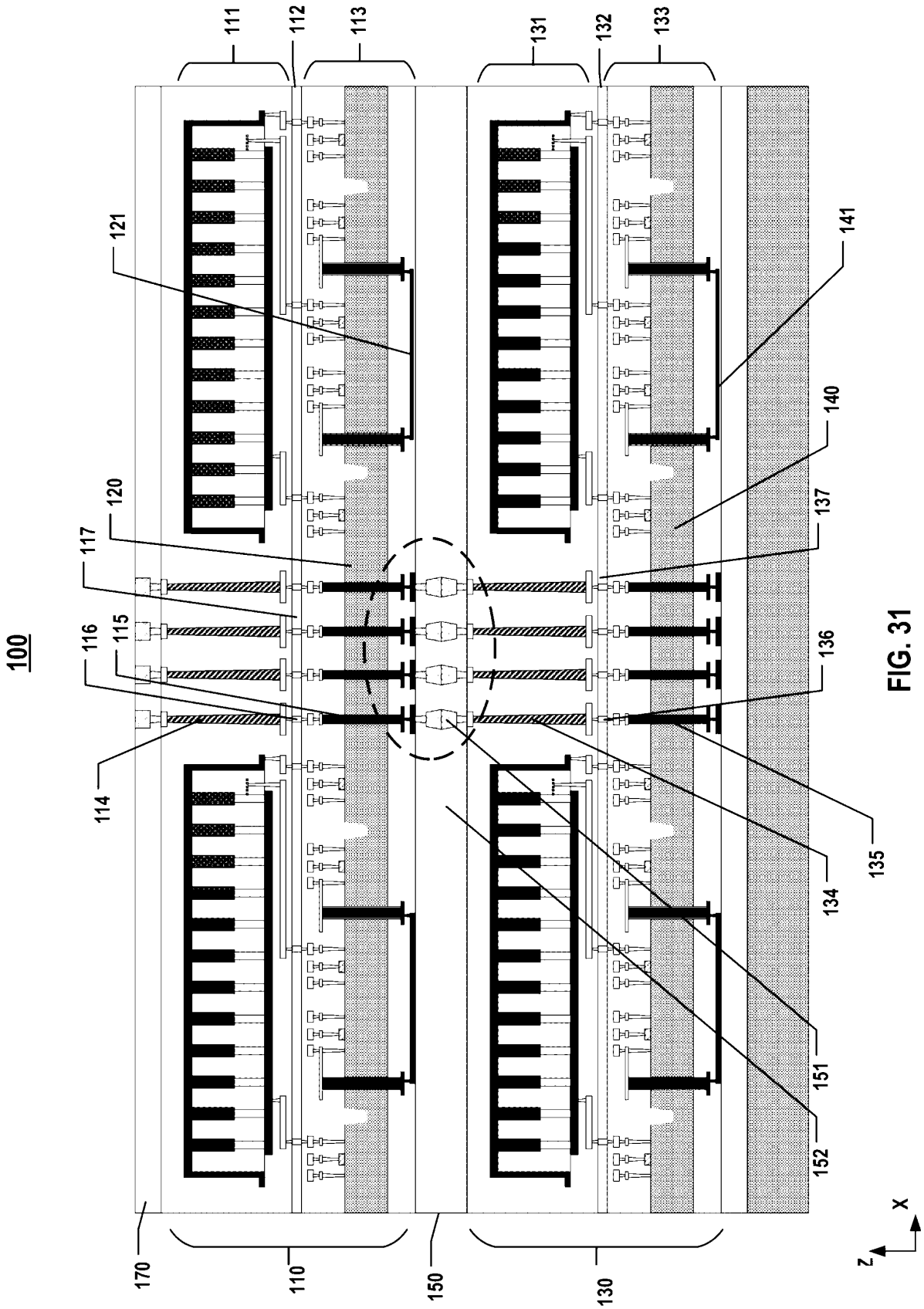

100
111
112
113
131
132
133
121
141
140
120
137
117
116
115
136
114
135
134
151
152
170
110
150
130
X
Z

FIG. 31

100

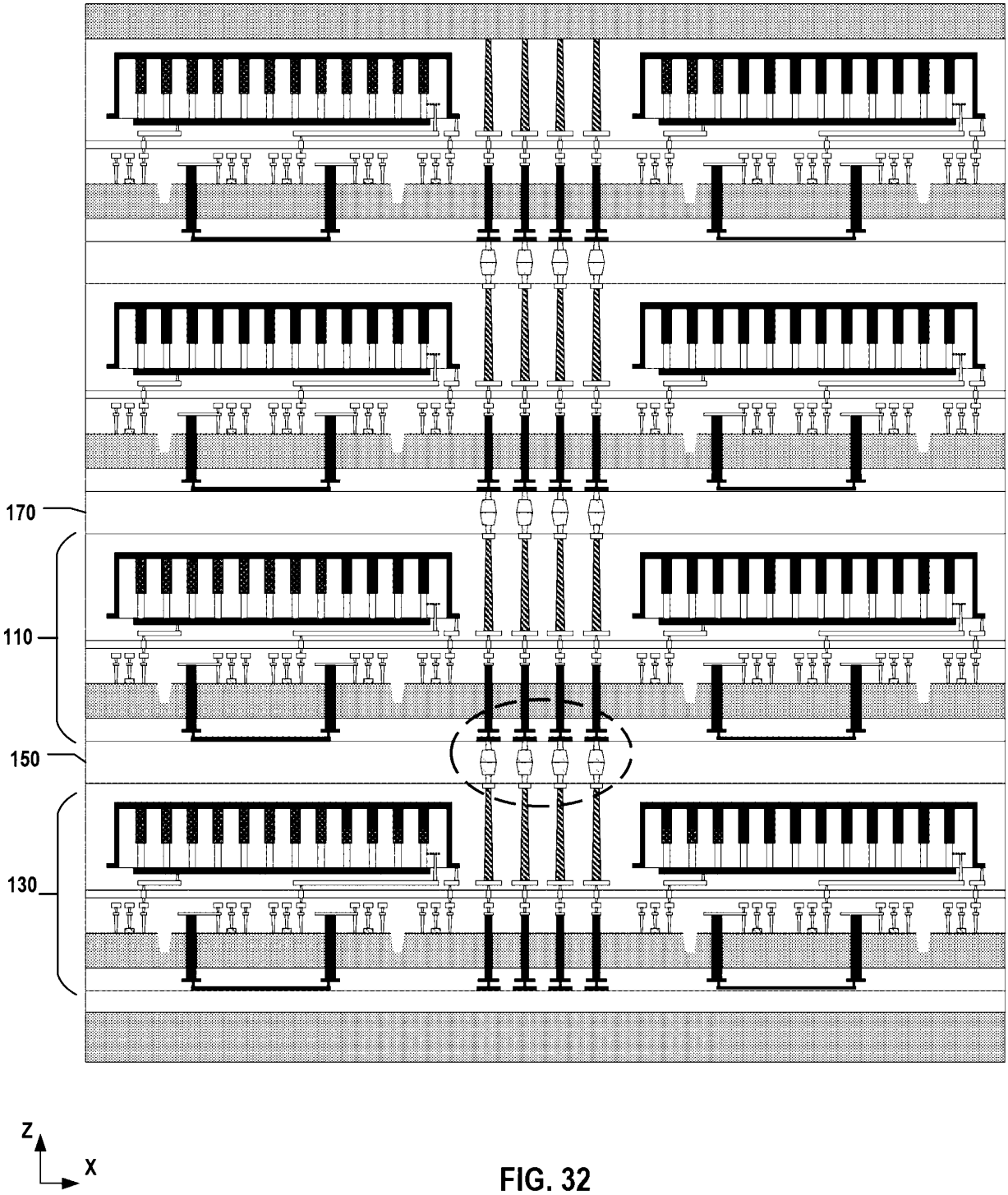


FIG. 32

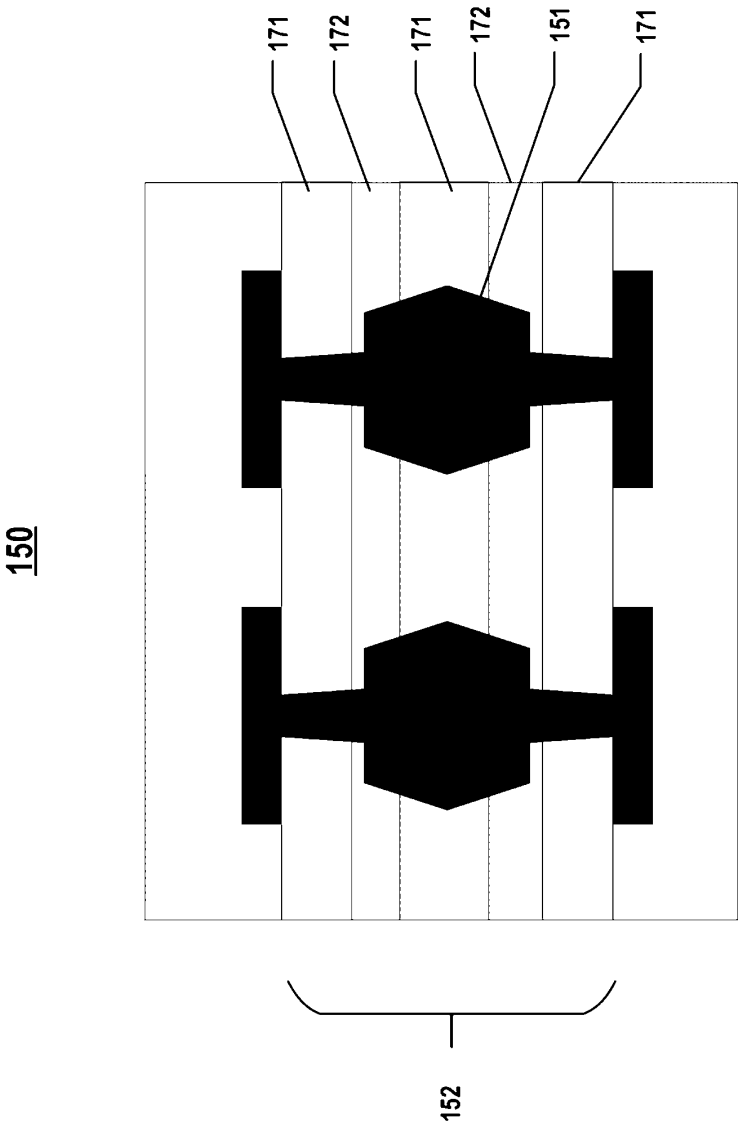


FIG. 33

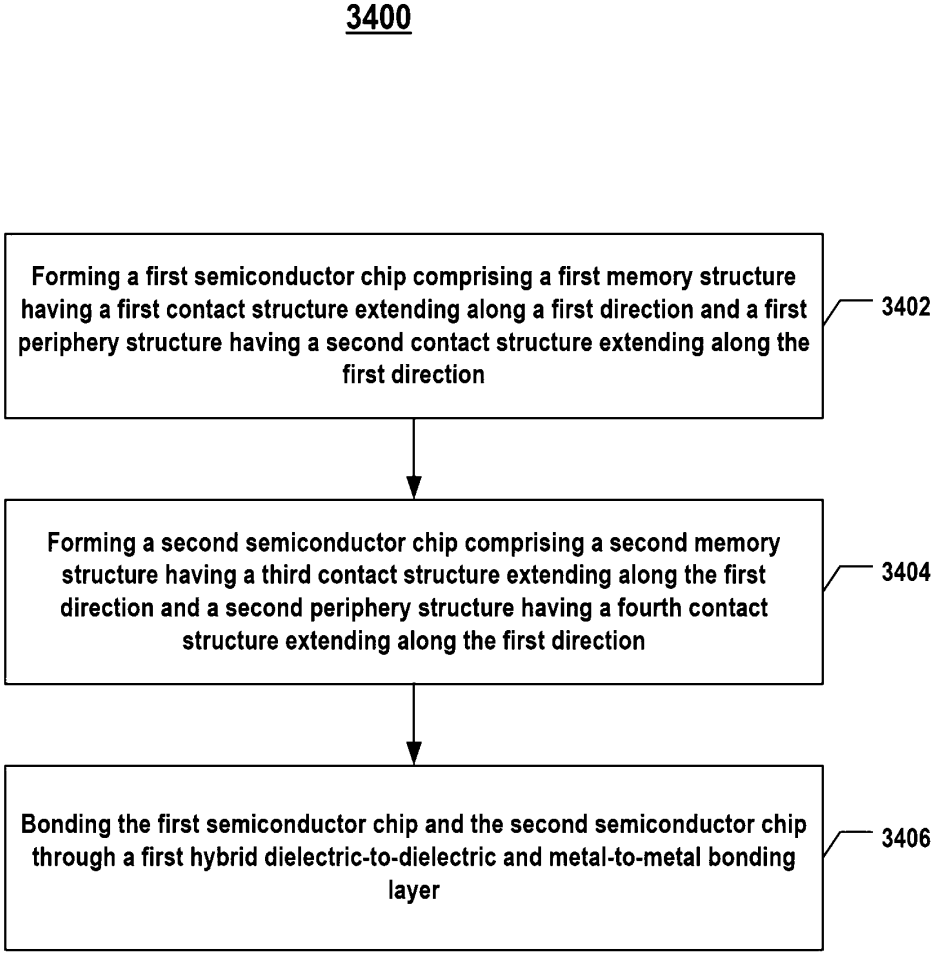

3400
Forming a first semiconductor chip comprising a first memory structure having a first contact structure extending along a first direction and a first periphery structure having a second contact structure extending along the first direction
3402
Forming a second semiconductor chip comprising a second memory structure having a third contact structure extending along the first direction and a second periphery structure having a fourth contact structure extending along the first direction
3404
Bonding the first semiconductor chip and the second semiconductor chip through a first hybrid dielectric-to-dielectric and metal-to-metal bonding layer
3406

FIG. 34

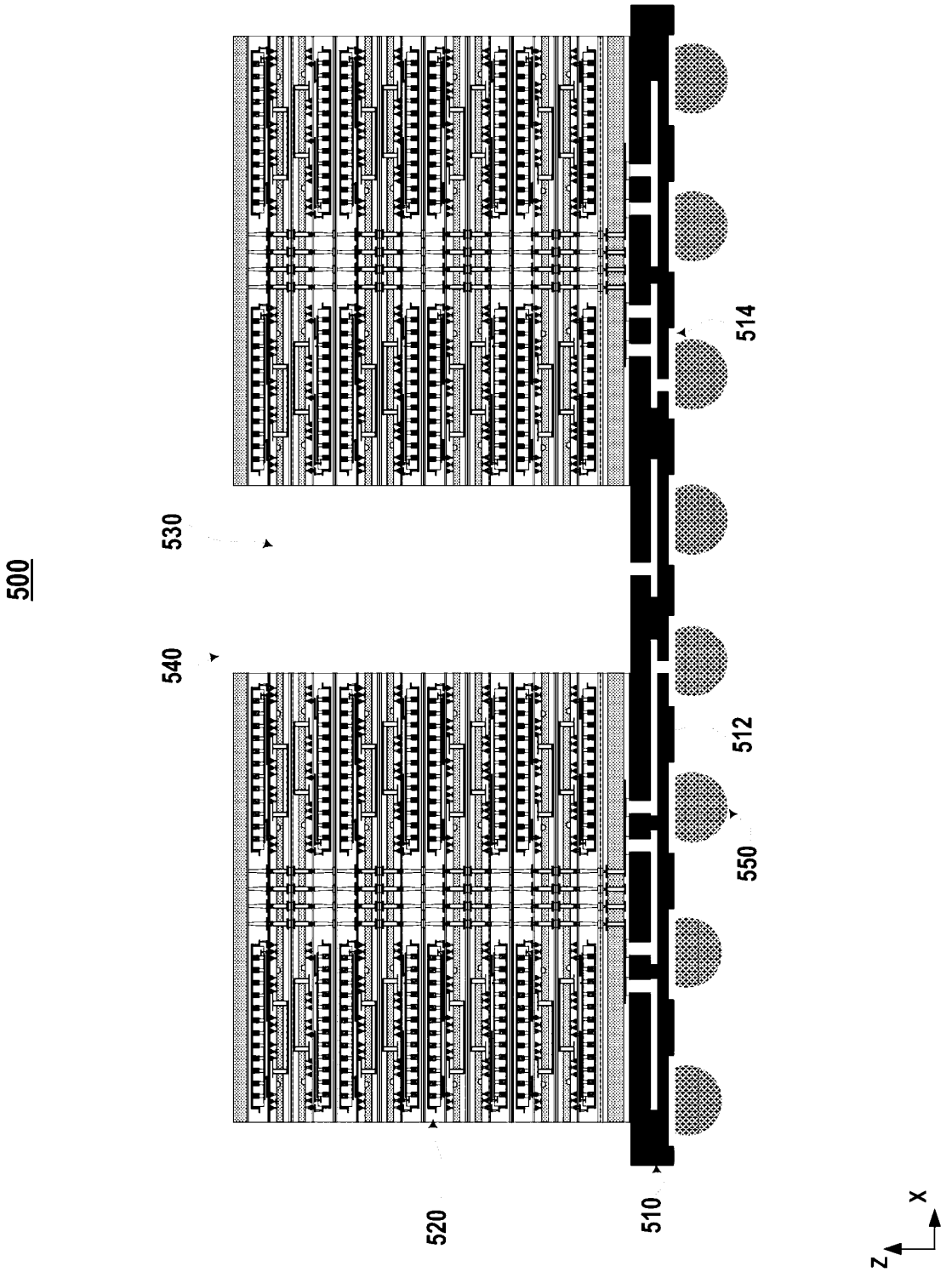


FIG. 35

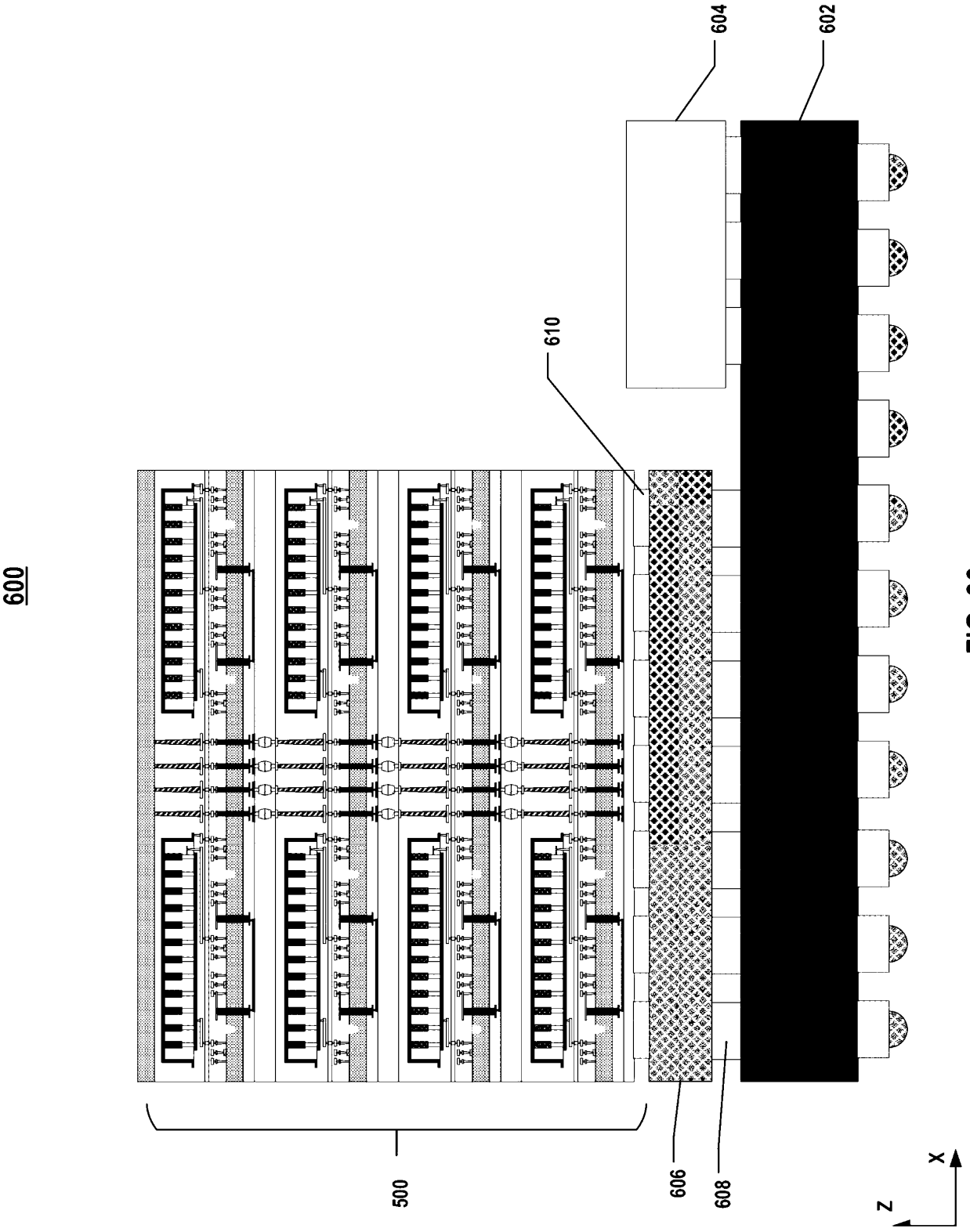


FIG. 36