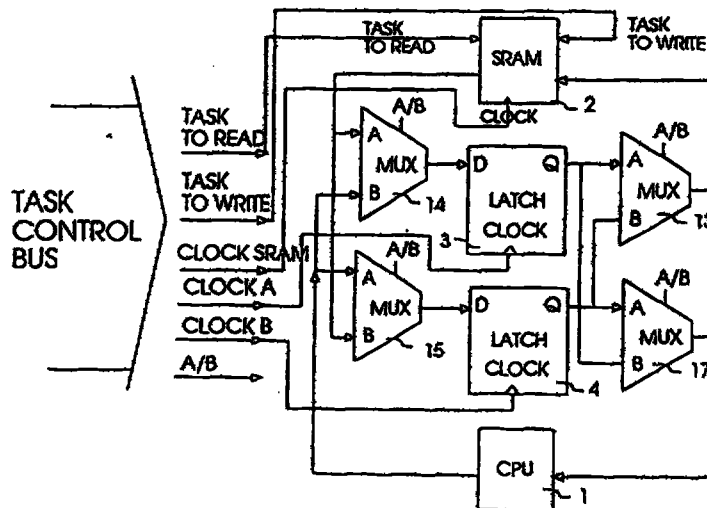




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(54) Title: ZERO OVERHEAD COMPUTER INTERRUPTS WITH TASK SWITCHING



(57) Abstract

The invention constitutes a unique hardware zero overhead interrupt and task change system for the reduction or elimination of interrupt latency as task change processing overhead delays in computer architectures. Without loss of time, the system performs complete task state saving and restoration between one cycle and the next without software intervention. For each Central Processing Unit (1) the invention uses one or more auxiliary latches (3, 4) wherein one latch (4) is used as the "running" latch and one of the auxiliary latches is attached to task storage memory. The invention swaps connections between alternate "running" registers and auxiliary registers while transferring other tasks to and from task storage memory (2). The invention provides a task linking system to allow the linking of tasks for mandatory sequential execution of the linked tasks. Further, the invention includes a priority "impatience" counter system to increase the relative priorities of various tasks as they approach their task deadlines.