

REPLACED SHEETS SG

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METHOD AND CIRCUIT TO SENSE THE T_j OF
MOS-GATED POWER SEMICONDUCTOR DEVICES

FIELD OF THE INVENTION

5 The present invention relates to the sensing of
the junction temperature of a MOS-gated power
semiconductor device, such as a power MOSFET or an IGBT
die. More specifically, the invention relates to the
integration of a simple temperature sensor in the MOS-
gated device die and relates to an integrated circuit for
10 trimming and reading the sensor.

BACKGROUND OF THE INVENTION

The accurate determination of the junction
temperature (T_j) of a power semiconductor device is
important for attaining high levels of operation
15 reliability. This problem is particularly critical for
extra low $R_{ds(on)}$ power MOSFETs, such as those having a
value of 6 milliohm, because these devices are very
difficult to protect against overloads.

It is known that an integrated circuit can be
20 employed to determine the junction temperature of the
power semiconductor device. However, prior FET devices,
such as the TEMPFET made by Siemens, require that the IC
be mounted on top or close to the power device. It is
more desirable to have the capability of either
25 separately packaging the integrated circuit in a standard
package or co-packaging it with the power device.

There are various ways to integrate a
temperature sensor into a power semiconductor device. As
an example, polysilicon diodes, P+/epi substrate diodes

or lateral MOSFETs are incorporated for temperature sensing. However, these known sensors have limitations and require fabrication using a non-standard process with extra masks. It is therefore desirable to incorporate a
5 temperature sensor that is compatible with current processes for manufacturing existing semiconductor devices.

It has been proposed to include a resistor in the power semiconductor device, such as an N+ polysilicon
10 resistor, to sense the junction temperature. The standard processes for making a polysilicon resistor have a very wide variation, typically $\pm 20\%$, which when compared to their very low temperature coefficient, typically $0.1\%/^{\circ}\text{C}$, can cause a $\pm 200^{\circ}\text{C}$ variation in the
15 measured temperature. Though this problem can be solved by trimming the IC that reads the sensor, the mass production process of the IC would be greatly complicated if each individual IC were to be trimmed for a respective MOSFET or IGBT. Thus, it is further desirably to
20 simplify the adaptation of the IC to the power device.

SUMMARY OF THE INVENTION

The present invention incorporates an N+ polysilicon resistor to sense the junction temperature of a MOS-gated semiconductor device and employs an
25 integrated circuit that is self-adapting to the power device.

The use of an N+ polysilicon resistor to sense the junction temperature has several advantages. The sensor is compatible with current MOS-gated semiconductor
30 devices, such as the HEXFET power MOSFET made by International Rectifier Corporation and IGBTs also made by International Rectifier Corporation. The sensor can

be easily routed at the center of the power device to sense the peak temperature. The thermal time constant is very low, typically on the order of $1\mu s$ and is an order of magnitude lower than that of the prior devices. The center is completely isolated from the power terminals by the field oxide so that the isolation is at least ± 60 volts for a low voltage HEXFET MOSFETs and higher for IGBTs. Thus, the temperature of a high side power semiconductor device can be easily sensed using a grounded IC control.

The self adapting IC includes a small non-volatile memory, typically around 10 bits, and a trimming sequencer. When the integrated circuit is assembled with the power semiconductor device on a printed circuit board or in a hybrid or power module, and is tested by the end user, a programming signal, typically 5 volts, is applied to a special input of the IC. The signal starts a trimming sequence inside the IC which may be similar to that used by the IR3010 device sold by International Rectifier Corporation. The IC then determines the optimum combination of bits that matches the respective room temperature resistance of the sensor. The trimming sequence is completely transparent to the user. When the programming pin is released, the 10 bit word is permanently stored in the IC memory.

The IC uses the value of the polysilicon resistance as an image of the junction temperature of the power device. The integrated circuit may also be capable of providing a simple overtemperature (OT) signal when the sensed temperature is above a predetermined threshold, a dual OT signal indicating pre alarm/shut down, or a linear measurement of the junction temperature T_j . These functions can be provided using relatively



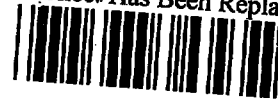
simple analog processing. The integrated circuit can also be capable of monitoring the junction temperature of up to 4 to 6 power semiconductor devices that are bridge connected.

5 In accordance with the invention, a method of self-trimming a temperature measuring circuit adapts to a respective temperature sensing resistor disposed in a power semiconductor device. Plural successive count values are generated, and a variable current is supplied
10 to the temperature sensing resistor that increases as a function of each successive count value. The voltage across the resistor is measured, and the counting is terminated when the voltage across the temperature sensing resistor reaches a predefined value. The last
15 one of these plural values is stored.

A reset signal to initiate the generation of the successive count values may be supplied. A constant current value may be generated as a function of the stored count value, the current supplied to the
20 temperature sensing resistor, and the voltage across the temperature sensing resistor measured. The measured voltage may be compared to a limit value that is proportional to the predefined value, and an overtemperature signal generated when the measured
25 voltage exceeds the limit value.

The predefined value may be proportional to the bandgap voltage. The method may also be carried out by an integrated circuit.

30 According to another aspect of the invention, a self-trimming temperature monitoring circuit adapts to a respective temperature sensing resistor disposed in a power semiconductor device. The sequencer generates plural successive count values, and a current source



supplies a variable current to the temperature sensing resistor having a value that increases as a function of each successive count value. A measuring circuit measures the voltage across the temperature sensing resistor, and a detecting circuit terminates operation of the sequencer when the voltage across the temperature sensing resistor reaches a predefined value. The final one of the count values is stored in a memory.

A reset signal generator may generate a signal that initiates operation of a sequencer. The current source may include a variable ratio current mirror, and the sequencer may include a counter. The predefined value may be proportional to the bandgap voltage.

The current source may include a constant current source which generates a constant current as a function of the value stored in the memory, and the measuring circuit may measure the voltage across the resistor using the constant current. An overvoltage detection circuit compares, when the constant current is delivered across the temperature sensing resistor, the voltage across the resistor to a limit value that is proportional to the predefined value, and an overtemperature signal generator generates an overtemperature signal when the measured voltage exceeds the limit value.

The circuit may be an integrated circuit, and the memory may be an EEPROM.

According to another aspect of the invention, a system measures the junction temperature of a power semiconductor device and includes a temperature sensing resistor disposed in the power semiconductor device, and a self-trimming, temperature sensing circuit that is adaptable to the temperature sensing resistor.

A semiconductor device may be a MOSFET or may be an IGBT. The circuit may be an integrated circuit, and the integrated circuit and power semiconductor device may be co-packaged.

5 Other features and advantages of the present invention will become apparent from the following description of the invention which refers to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

10 The invention will now be described in greater detail in the following detailed description with reference to the drawings in which:

Figure 1 is a top view of an MOS-gated power semiconductor device in which a temperature sensing polysilicon resistor is incorporated according to the invention;

Figure 2 is a block diagram showing the temperature sensing integrated circuit according to the invention; and

20 Figure 3 is a diagram showing an example of the implementation of the integrated circuit of Figure 2 with a power semiconductor device.

DETAILED DESCRIPTION OF THE INVENTION

Figure 1 shows how the temperature sensor polysilicon resistor can be implemented in an MOS-gated power semiconductor device die 9. The die may be a power MOSFET or an IGBT, for example. The polysilicon resistor 10 is narrower in the vicinity of the source pad 11 to sense the peak temperature. The total number of squares of the resistor is 1000 to 2000, corresponding to 25 to 50 KOhm, respectively. The gate pad 12, drain 13, and

source 11 are connected to pins 14, 15 and 16, respectively, of a conventional package. Sense pins 1 and 2 are connected to sense pads 17 and 18, respectively, on the resistor of die 9.

5 Fig. 2 shows a simplified block diagram of the self-adapting IC 20. The self-adapting operation of IC 20 is as follows: When +5V is supplied to the PROG input, a reset signal is delivered to the counter 22. Then, the counter 22 starts to count up, increasing the
10 ratio of the variable current mirror 23 and, in turn, the current supplied to the resistor 10. The current supplied to the sense resistor 10 ramps up until the voltage across it reaches 0.87 times value of a bandgap reference voltage V_{bg} , present in line 29. The bandgap
15 reference voltage is supplied by bandgap reference supply 37 and is divided across divider 38 and then supplied to op-amp 35 which compares the divided voltage, $0.87 V_{bg}$, to the voltage across resistor 10. When the voltage across resistor 10 reaches $0.87 V_{bg}$, op-amp 35 changes state and
20 the output is supplied to AND gate 39 which, in turn, turns off clock enable 33. Then, the enable signal on line 30 goes low, the counter 22 stops counting and the last bit word supplied by the counter is stored in the EEPROM 31.

25 During normal temperature sensing operation, the PROG input 21 is held to ground potential by a pull down resistor 32. A current source 40 generates a zero temperature coefficient current which flows through the current mirror 23 and across sense resistor 10. The
30 value of the current supplied to resistor is controlled using the value stored in EEPROM 18 such that at room temperature, the voltage across the resistor is $0.87 V_{bg}$.

If the power device heats up above 170°C, the sense voltage will reach V_{bz} causing op-amp 36 to change state, and the overtemperature (OT) signal will go high. The current source 40 has a zero temperature coefficient to avoid influencing the IC temperature on the OT threshold.

The EEPROM 31 can be implemented using a CMOS/EEPROM processor or by "zener zapping". The size of the IC is only a few mm².

Fig. 3 shows a practical implementation of the IC 20. The IC 20 can be assembled in a very small surface amount package or may be co-packaged with a power device 50, such as a MOSFET or IGBT, in a power module.

In carrying out the design, care must be taken to control variations in the temperature coefficient (TC) of the polysilicon resistor. These variations translate directly into variations in the OT threshold. Thus, it is preferable that the variations of TC are less than +/- 10%.

Care should also be taken to prevent loss of data on the EEPROM which can be caused by a high ambient temperature, such as the ambient temperature of 150°C that is needed for automotive applications and the ambient temperature of 200°C for power modules application. The "zap" technique may be used in place favor of the EEPROM 31 in such applications.

Although the present invention has been described in relation to particular embodiments thereof, many other variations and modifications and other uses will become apparent to those skilled in the art. It is preferred, therefore, that the present invention be limited not by the specific disclosure herein, but only by the appended claims.



WHAT IS CLAIMED IS:

1. A method of self-trimming a temperature measuring circuit to adapt to a respective temperature sensing resistor disposed in a power semiconductor device, the method comprising the steps of:

5 generating a plurality of successive count values;

supplying a variable current to the temperature sensing resistor, the value of said current increasing as a function of each successive count value;

10 measuring the voltage across the resistor;
terminating the counting when the voltage across the temperature sensing resistor reaches a predefined value; and

15 storing the final one of said plurality of successive count values.

2. The method of claim 1 further comprising the step of supplying a reset signal to initiate said step of generating a plurality of successive count values.

3. The method of claim 1 further comprising the steps of:

5 generating a constant current as a function of the stored count value and supplying the constant current to said temperature sensing resistor; and

measuring the voltage across the temperature sensing resistor.

4. The method of claim 3 further comprising the steps of:





5 comparing the measured voltage with a limit
value that is proportional to said predefined value; and
 generating an overtemperature signal when said
measured voltage exceeds said limit value.

5. The method of claim 1 wherein said
predefined value is proportional to the bandgap voltage.

6. The method of claim 1 wherein said method
is carried out by an integrated circuit.

7. A self-trimming temperature monitoring
circuit for adapting to a respective temperature sensing
resistor disposed in a power semiconductor device; said
circuit comprising:

5 a sequencer for generating a plurality of
successive count values;

 a current source for supplying a variable
current to the temperature sensing resistor, the value of
said current increasing as a function of each successive
10 count value;

 a measuring circuit for measuring the voltage
across the temperature sensing resistor;

 a detecting circuit for terminating operation
of said sequencer when the voltage across the temperature
15 sensing resistor reaches a predefined value; and

 memory for storing the final one of said
plurality of successive count values.

8. The circuit of claim 7 further comprising
a reset signal generator for generating a signal that
initiates operation of said sequencer.





9. The circuit of claim 7 wherein said current source includes a variable ratio current mirror.

10. The circuit of claim 7 wherein said sequencer includes a counter.

11. The circuit of claim 7 wherein said predefined value is proportional to the bandgap voltage.

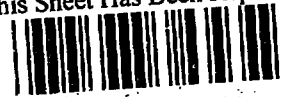
12. The circuit of claim 7 wherein said current source includes a constant current source, said current source generating a constant current as a function of the value stored in said memory, and said measuring circuit measure the voltage across said resistor using said constant current.

13. The circuit of claim 12 further comprising an overvoltage detection circuit for comparing, when said constant current is delivered across the said temperature sensing resistor, the measured voltage across said resistor with a limit value that is proportional to said predefined value, and an overtemperature signal generator for generating an overtemperature signal when said measured voltage exceeds said limit value.

14. The circuit of claim 7 wherein said circuit is an integrated circuit.

15. The circuit of claim 7 wherein said memory is an EEPROM.





16. A system for measuring the junction temperature of a power semiconductor device, said system comprising:

5 a temperature sensing resistor disposed in said power semiconductor device; and

a self-trimming temperature sensing circuit that is adaptable to said temperature sensing resistor and comprising:

10 a sequencer for generating a plurality of successive count values;

a current source for supplying a variable current to the temperature sensing resistor, the value of said current increasing as a function of each successive count value;

15 a measuring circuit for measuring the voltage across the temperature sensing resistor;

a detecting circuit for terminating operation of said sequencer when the voltage across the temperature sensing resistor reaches a predefined value; and

20 memory for storing the final one of said plurality of successive count values.

17. The circuit of claim 16 further comprising a reset signal generator for generating a signal that initiates operation of said sequencer.

18. The system of claim 16 wherein said current source includes a variable ratio current mirror.

19. The system of claim 16 wherein said sequencer includes a counter.





20. The system of claim 16 wherein said predefined value is proportional to the bandgap voltage.

21. The system of claim 16 wherein said current source includes a constant current source, said current source generating a constant current as a function of the value stored in said memory, and said
5 measuring circuit measure the voltage across said resistor using said constant current.

22. The system of claim 21 further comprising an overvoltage detection circuit for comparing, when said constant current is delivered across the voltage across temperature sensing resistor the voltage across said
5 resistor with a limit value that is proportional to said predefined value, and an overtemperature signal generator for generating an overtemperature signal when said measured voltage exceeds said limit value.

23. The system of claim 16 wherein said circuit is an integrated circuit.

24. The system of claim 16 wherein said memory is an EEPROM.

25. The system of claim 16 wherein said power semiconductor device is a MOSFET.

26. The system of claim 16 wherein said power semiconductor device is an IGBT.





27. The system of claim 23 wherein said integrated circuit and said power semiconductor device are co-packaged.

