SPECIFICATION

Electrical delay network comprising a chain of all-pass sections

The invention relates to an electrical delay network comprising a chain of at least three all-pass sections having mutually substantially identical phase responses and substantially flat amplitude responses as a function of frequency at least up to a given frequency value. Such a network may be used for delay purposes or, for example, as an electrical filter network whose frequency response can be adjusted electrically by simple means.

The trend in recent years has been towards digitally controlled and operated filters, for example transversal filters, comprising a chain of clock-pulse controlled storage sections, tappings on the chain being coupled to a summing device *via* weighting factor adjusting means. The summing device adds the input signal to the input signal delayed by various amounts, yielding an output signal whose amplitude and phase (*i.e.* the characteristic) can be adjusted electrically by means of the weighting factor adjusting means. Such filters can be realized in integrated circuit form and are suitable for a wide field of applications owing to their adjustability, a given required adjustment being obtainable by means of a read-only memory (ROM) which may be programmable.

Such filters do, however, exhibit some drawbacks, which prevent their general use in for example radio and television receivers. For example, a source of clock pulses is needed, which source generally has to be capable of supplying a substantial power, in order to shift the signal along the chain of storage sections with the required reliability and accuracy. Moreover the clock frequency, which determines the maximum signal frequency that can be processed, cannot be varied without the risk of signal degradation occurring.

The invention provides an electrical delay network comprising a chain of at least three all-pass sections having mutually substantially identical phase responses and substantially flat amplitude responses as a function of frequency at least up to a given frequency value, said all-pass sections being integrated on a semiconductor body and each comprising a semiconductor current amplifier circuit arrangement having first and second inputs and a common output, and first and second couplings from an input terminal of the section to said first and second inputs respectively, said first coupling including a series resistor, said second coupling including a series capacitor, said amplifier circuit arrangement being inverting from one of its said inputs to its output, being non-inverting from the other of its said inputs to its output, and comprising a current mirror coupling said one of ins inputs to its output.

It should be noted that, if the current amplifier arrangement in such a network were replaced by a voltage amplifier arrangement, and an input signal voltage were applied thereto by applying it to a series combination of a resistor and a capacitor, the resulting voltage component appearing across the resistor being applied to the first input of the amplifier arrangement and the resulting voltage component appearing across the capacitor being applied to the second input of the amplifier arrangement, special attention would have to be paid to parasitic effects, because of the fact that the two voltage components would appear across floating impedances.

Embodiments of the invention will now be described, by way of example, with reference to the accompanying diagrammatic drawings, in which

Figure 1 is a block diagram of a first embodiment of the invention, in the form of a transversal filter;

Figure 2 shows a variant of the filter of Figure 1;

Figures 3 and *4* show first and second examples respectively of an all-pass section which form part of the filters of Figures 1 and 2;

Figure 5 shows a possible modification to part of the all-pass section of Figure 3;

Figure 6 shows a possible modification to the circuit of Figure 5;

Figure 7 shows a possible modification to another part of the all-pass section of Figure 3;

Figure 8 shows a possible modification to the circuit of Figure 7;

Figure 9 shows a possible construction for part of the circuits of Figures 7 and 8;

Figure 10 shows a possible modification to the circuit of Figure 8;

Figure 11 shows a complete all-pass section incorporating the circuit of Figures 6 and 10;

Figure 12 shows examples of characteristics which can be obtained in a transversal filter made up from sections constructed as shown in Figure 10; and

Figure 13 is a block diagram of a further embodiment of the invention in the form of a programmable filter including sections constructed as shown in Figure 10.

Figure 1 shows a transversal filter in schematic form. An input signal S_i is applied to a chain of all-pass sections S_1, S_2...s_n which ideally have constant amplitude response characteristics and identical phase response characteristics. These characteristics may be represented by the transfer function

$$\frac{p-1/2}{p+1/2}$$

where p represents the complex frequency $\mathcal{R} + jw$ ($\mathcal{R}$ = the damping, ω = the angular frequency). The chain is preceded by a section s_0 having a transfer function

$$\frac{1}{p+1/2}$$

so as to obtain an orthogonal pulse response at the tappings; this section may be omitted under some conditions. Weighting factor adjusting means w_0 w_1, $w_2 \ldots w_n$ are fed from respective tappings on the chain, and multiply the signals at the corresponding tappings by factors a_0, a_1, $a_2 \ldots a_n$ respectively. The output signals of the adjusting means $w_0 \ldots w_n$ are added together to produce the output signal s_0. As a variant the input signal S_i may be applied to tappings on the chain of sections $s_0 \ldots s_n$ via the various adjusting means (see Figure 2), the chain then performing the summing function to produce the output signal S_0. In either case the contribution to S_0 by the k^{th} weighting factor adjusting means w_k is given by

$$\frac{(p-1/2)^k}{(p+1/2)^{k+1}} \cdot a_k.$$

As a further variant (not shown) a recursive filter can be obtained by applying the input signal in a manner as shown in Figure 2 to tappings on the chain of sections s_0 - s_n *via* the weighting factor adjusting means and by furthermore feeding the output of the section s_0 back in phase opposition to said tappings *via* an attenuator and further weighting factor adjusting means. In this case the section s_0 should be dispensed with.

In all these cases a filter is obtained whose transfer characteristic can be varied at will by means of the weighting factor adjusting means, whilst owing to the orthogonality of the pulse responses *via* the different paths (see, for example, Y. W. Lee, Statistical Theory of Communication, 1960, Chapter 19) there is no risk of interaction of the weighting factor adjusting means with the transmission of the complete filter. It will be evident that if the chain of sections $s_0 \ldots s_n$ is to be used for delay purposes only, all or some of the weighting factor adjusting means $w_0 \ldots w_n$ may be dispensed with.

When realizing transversal filters attention has been paid so far in the main to versions which comprise clock-pulse controlled delay sections provided with tappings from which the delayed signals are taken, these signals being adjusted to the desired magnitude with the aid of weighting factor adjusting means and being subsequently added together. Such transversal filters are generally realized by means of integrated circuit technology. However, they cannot be realised by those standard integration processes by means of which other circuits are also integrated; special processes have had to be developed for this purpose, and have enabled filters of very small dimensions to be obtained. Therefore the sections s of Figures 1 and 2 are not constructed in this way.

It is known *per se* that in order to realize the transfer function $p-\frac{1}{2}/p+\frac{1}{2}$ of one section in an analogue manner, use can be made of an amplifier having two outputs which carry signal voltages in phase opposition, one output being connected to a common point via a resistor, and the other being connected thereto *via* a capacitor, the desired output signal appearing on said common point. However, such a circuit is not suitable for integration, because the parasitic impedances which then occur affect the transfer function.

Each section s of Figures 1 and 2 therefore in fact comprises a semiconductor amplifier circuit arrangement having first and second inputs and a commmon output, and an arrangement comprising a resistor and a capacitor coupling an input terminal of the section to said first and second inputs in such manner that first and second signal paths having resistive and capacitive characters respectively exist from said input terminal to said common output via said first and second inputs respectively and a signal applied to said input terminal will be split between said paths, the amplifier circuit arrangement being constructed to exhibit negligible consumption of input signal power.

Figure 3 shows a very simple possible construction for such a section. The input signal current i_i is applied to an input terminal 11 of the section and then divides between two parallel branches, the first (resistive) branch comprising a resistor R and a non-inverting current amplifier 1, and the second (capacitive) branch comprising a capacitor C and an inverting current amplifier 2–3, which takes the form of a current mirror. Owing to the low input impedances of the amplifiers 1 and 2–3 respectively, the signal power consumption by these amplifiers is negligible and, moreover, any parasitic impedances present leave the respective resistive and capacitive characters of the two branches substantially unaffected. The amplifier 1 takes the form of a transistor amplifier with its base earthed and its emitter constituting the input. The amplifier 2–3 comprises a transistor 2 which is connected as a diode and which shunts the base-emitter path of a transistor 3 to form a kown type of current mirror arrangement having a low input impedance.

The term "current mirror" is to be understood herein to mean an arrangement which comprises a first transducer which converts a current flowing through it into a voltage which is a non-linear (generally logarithmic) function of this current, which first transducer is coupled to a second transducer which re-converts said voltage into a current which is a non-linear (generally exponential) function of said voltage. The latter function will generally be the inverse of the former function. The input current of the current mirror can pass through the first transducer (e.g. diode 2 in Figure 3) in which case the second transducer (e.g. transistor 3 in Figure 3) may provide the output current of the current mirror. However, as an alternative the output current of the current mirror may pass through the first transducer (diode 2) and the input current through the second transducer (3) (as shown in the variant of Figure 4), if the circuit including the two transducers is included in a negative-feedback loop of an amplifier (4 in Figure 4).

Figure 4 shows an alternative possible construction for a network section. In Figure 4 the input signal current i_i is again applied to two parallel branches. The first branch comprises a resistor R and now terminates in an inverting current amplifier in the form of a current mirror, known *per se*. This current mirror again comprises a transistor 2, which is connected as a diode, connected in parallel with the emitter-base path of a transistor 3. The collector-base path of transistor 3 is shunted by the base-emitter path of a transistor 4. The signal current component i_R through said first branch is consequently duplicated in the collector of the transistor 4. The second branch comprises a capacitor C and terminates at the connection between the base of transistor 3 and the emitter of transistor 4.

Consequently, transistor 4 functions as a non-inverting current amplifier for the signal current component i_c through the second branch and the output current i_o of transistor 4 consequently becomes equal to $i_c \cdot i_R$. A similar effect is obtained if the capacitor C and the resistor R are interchanged.

In the ideal case the output current i_o as a function of the input current i_i is given by

$$\frac{i_o}{i_i} = \frac{1-pRC}{1+pRC} \text{ and } -\frac{1-pRC}{1+pRC} \text{ in Figures 3 and 4 respectively.}$$

However this expression is not satisfied exactly at high frequencies. Since each of the two branches comprises an individual amplifer, it is possible to select the current gains of these branches differently. If these current gains at low frequencies are a_o and b_o respectively, then $\frac{i_o}{i_i}$ may be written as $\frac{i_o}{i_i} = \frac{a}{1+pRC} - \frac{bpRC}{1+pRC}$ where

$a = \frac{a_o}{1+p\tau_a}$ and $b = \frac{b_o}{1+p\tau_b}$. In the last expressions τ_a and τ_b are time constants which are representative of the high-frequency behaviour of the transistors in the first amplifer (1 in Figure 3; 2, 3, 4 in Figure 4) and the second amplifer (2, 3 in Figure 3; 4 in Figure 4) respectively.

If for convenience a_o is assumed to have the value 1, a substantial improvement of the high-frequency behaviour of the section can be obtained by choosing b_o to equal $1 - 3/8c$. The ratio i_o/i_i is then given to a first approximation by:

$$\frac{i_o}{i_i} \approx \frac{1-p\tau_a}{1+pRC} - \frac{pRC}{1+pRC} + \frac{p\tau_a}{1+pRC} + \frac{p^2RC\,\tau_b}{1+pRC} - \frac{p^2\,\tau_a\,\tau_b}{1+pRC}$$

$$\approx \frac{1}{1+pRC} - \frac{pRC}{1+pRC}.$$

If, allowance is made for the internal resistance r of the diode 2 in Figure 3, the transfer function of the section becomes:

$$\frac{i_o}{i_i} = a\frac{1+prC}{1+p(R+r)C} - b\,\frac{pRC}{1+p(R+r)C}.$$

This effect can be corrected by selecting b to equal $1 + 2r/R$ (for $a = 1$). It is furthermore possible to correct for the parasitic capacitance c which the input terminal 11 of the section exhibits relative to the substrate of a semi-conductor body on which the sections are integrated, by selecting b_o to equal $1 + c/C$ (for $a = 1$).

All in all the gain factor b_o can be adjusted by adding together the various above-mentioned differences between b_o and the value 1, so that a common correction for all the above-mentioned undesired effects is obtained. In theory, this could be realized by the example constructing the current mirror 2–3 in Figure 3 so that the ratio of its ouput current to its input current is different from 1, for example by selecting the emitter areas of the transistors 2 and 3 to be different from each other. However, in practice it is found desirable to make the value of b_o freely adjustable, not only because of possible spreads in the transistor parameters, but also because if the quiescent-current settings of the transistors are varied, for example in order to change the drive range or signal handling capacity of the filter, the transistor parameters and thus

the correction needed for b_o may change.

Figure 5 shows a modification to the capacitive branch of Figure 3 by means of which this adjustment of b_o can be obtained. For this purpose a low resistance R_s is included between the diode 2 and the transistor 3 of Figure 3, across which a voltage is produced with the aid of an adjustable current source I_s, which voltage, added to the voltage across the diode 2, acts on the base of the transistor 3 and consequently determines the gain of the current mirror 2–3. If a setting is selected for the current source I_s which is such that when $I_c = 0$, i_o also equals 0, the mirror ratio $\frac{i_o}{i_c}$ will very exponentially with the bias current I_s. A similar resistor may be included in the arrangement of Figure 4.

A drawback of the circuit arrangement of Figure 5, is, *inter alia*, that negative feedback occurs for high frequencies *via* the internal collector-base capacitance of the transistor 3. This can be compensated for in the manner shown in Figure 6 i.e. by providing an additional transistor 5 in series with transistor 3, the base of this additional transistor being connected to a point of constant potential (cascode circuit).

The capacitance C_{be3} between the base of transistor 3 and earth also has an adverse effect on the high frequency behaviour. This capacitance is constituted by the internal base-emitter capacitance of the transistor 3 and by the capacitance of the current source I_s with respect to earth. However, this effect can be compensated for by not connecting transistor 2 as a pure diode, but rather by including a low resistance R_b in its base circuit and connecting its collector to the junction point of R_s and R_b, thereby utilizing the capacitance C_{be2} between the base and emitter of transistor 2. The requirement for full compensation is $R_sC_{be3}=R_bC_{be2}$. Such an extra resistor may be included in the arrangement of Figure 4.

In general it is desirable that the delay (=2RC) produced in each section be adjustable. In theory the capacitors may be made variable, for example by realizing them as reverse-biased pn-diodes, a similar variation of the capacitance values of the capacitors (*i.e.* the diodes) in variable voltage to a line which is common to the diodes. However, it is preferred to make the effective values of R adjustable, so that the capacitive branches can be chosen to give maximum bandwidth.

Figure 7 shows a circuit arrangement by which the effective resistance value may be adjusted. The resistor R of Figure 3 is shunted in Figure 7 by a transistor 6, to shows base a variable voltage is applied with the aid of a variable current source I_c and a resistor R_c of low value. The transistor 1 is the non-inverting amplifier transistor 1 of Figure 3. The input current i_R (of the resistive branch) flows through the parallel combination of the resistor R and the transistor 6 and then through the emitter-collector path of the transistor 1 to the output 12, so that i_o is substantially equal to i_R.

The parallel combination of R and transistor 6 constituents an impedance the value of which increases exponentially with the current setting of the source I_c. This is because the base of transistor 6 is virtually connected to earth for signal voltages, resulting in negative signal feedback *via* its emitter. The value of this impedance is the effective resistance value.

In order to correct for the base currents of the transistors 1 and 6 of Figure 7, further transistors 7 and 8 may be included as shown in Figure 8, which transistors can be biased in such a way (with the aid of a current source I_h) that no standing current flows through the resistor R. For this purpose a bridge of current sources I_{s1} and I_b has been included. The source I_b is preferably adjusted to produce a current which is twice as high as that produced by the source I_h.

The current sources required for eachof the sections are preferably coupled to each other in such manner that all currents will vary to the same degree in response to a common control signal and the delay times of the sections will always substantially correspond to each other. Figure 9 shows an example of how the various sources I_c and I_o (Figures 7 and 8) can be controlled simultaneously by sources I_{in} and I_h, *viz.* in such a way that the otherwise exponential variations of the effective resistance per section with control current is replaced by a variation given by $R_{eff} = R/(1-I_{in}/I_h)$.

The tappings and weighting factor adjusting means (w_o ... w_n in Figure 1) required for transversal filter operation can be incorporated in the amplifer included in the branch having a resistive character. Figure 10 shows how this may be done by adding further transistors 16, 17 and 18 and a current source I_t to the circuit of Figure 8. In Figure 10 the input signal current i_i of the section applied to the input terminal 11 again divides over the (first) branch containing the resistor R and the (second) branch containing the capacitor C (the latter branch being assumed to be constructed as described with reference to Figure 5 or 6). The output current i_o of the first branch (to which that of the second branch is to be added) is taken from the output electrode 12 of the section. The tapping current i_t of the section appears in a balanced manner on terminals is given by $i_t = \frac{I_t}{I_b} i_R$ where i_R is again the signal current component in the first branch. This formula reveals that the magnitude of the tapped current can be adjusted by suitably choosing the output current of the source I_t. This adjustment may be fixed, but for versatility (flexibility) of the transversal filter it may be desirable to provide an electrical adjusting facility. This may, for example, be obtained in known manner with the aid of a programmable read only memory (ROM). Because $i_R = i_i/(1+pRC)$, so that $i_t = I_t/I_b$ $i_i/1+pRC$ in the arrangement of Figure 10, it is not necessary to provide the low-pass section S_o described with reference to Figure 1 when each section is constructed as shown in Figure 10, its function then being automatically incorporated in the resistive branches. A transversal filter consisting entirely of identical sections may therefore be constructed.

Figure 11 shows the complete circuit of a filter section constructed in accordance with the principle discussed above. The input current i_i of the section divides over a first branch (current component i_R) having a resistive character and constructed as shown in Figure 10, and a second branch (current component i_C) having a capacitive character and constructed as shown in Figure 6. The output current i_o of the

section, which is also the input current of the next section, is obtained by summation of the currents in the two branches. The necessary corrections can be obtained with the aid of the current sources I_a, I_c and I_h, whilst the magnitude of the current i_t on the tapping electrodes 21, 22 can be adjusted with the aid of the current source I_t. In a practical emobidment the resistors R_a, R_b and R_c and values of 100, 200 and 200 Ohms respectively, the capacitor C was constituted by a nitride dielectric and had a value of 30 pF, and the parasitic capacitance in parallel with the transistor 2 was 10 pF.

Figure 12 shows some transfer characteristics which were obtained for a single section constructed as shown in Figure 11 and which was terminated in the correct manner. The amplitude response a_o from the input 11 to the output 12 was substantially flat up to approximately 50 MHz, whilst the corresponding phase characteritic ψ_o passed through the value 90° at approximately 2 MHz. The amplitude response a_t and the phase response ψ_t at the tapping points 21 and 22 was such that the amplitude had dropped by 3 dB and the phase shift was 45° at this frequency.

Figure 13 is a block diagram of part of a programmable filter each section 26, 27, ... of which is constructed as shown in Figure 11. A coefficient memory 23 controls digital-analog converters 24 and 25, which produce respective currents I_t which determine the magnitudes of the weighting factors a_t (c.f. Figure 1) for the tappings on the cascaded delay sections 26, 27, ... The tapping currents i_t are applied to bushbars 30 and 31 with the desired polarity by means of switches 28, 29, ... these polarity switches being controlled by the sign bit of the corresponding coefficent in the coefficient memory. The anlog section of the circuit may for example be realized by means of a standard linear bipolar integration process and the digital section may for example be realized in I^2L (integrated injection logic), together on one semiconductor body.

CLAIMS

1. An electrical delay network comprising a chain of at least three all-pass sections having mutually substantially identical phase responses and substantially flat amplitude responses as a function of frequency at least up to a given frequency value, said all-pass sections being integrated on a semiconductor body and each comprising a semiconductor current amplifier circuit arrangement having first and second inputs and a common output, and first and second couplings from an input terminal of the section to said first and second inputs respectively, said first coupling including a series resistor, said coupling including a series capacitor, and amplifier circuit arrangement being inverting from one of its said inputs to its output, being non-inverting from the other of its said inputs to its output, and comprising a current mirror coupling said one of its inputs to its output.

2. A network as claimed in Claim 1, wherein the current mirror comprises a first transistor, a diode or diode-equivalent connected in parallel with the base-emitter path of said first transistor, and a second transistor the base-emitter path of which shunts the collector-base path of the first transistor, said one input of the amplifier circuit arrangement being connected to the base of the second transistor, said other input of the amplifier circuit arrangement being connected to the base of the first transistor, and the collector of the second transistor being connected to the common output of the amplifier circuit arrangement.

3. A network as claimed in Claim 1, wherein the current mirror comprises a first transistor, a diode or diode-equivalent connected in parallel with the base-emitter path of said first transistor and a second resistor included in a connection from the diode or diode-equivalent to the first transistor, said one input of the amplifier circuit arrangement being connected to the diode or diode-equivalent, and the collector of the first transistor being connected to the output of the amplifier circuit arrangement.

4. A network as claimed in Claim 2, including a second resistor in a connection from the diode or diode-equivalent to the first transistor.

5. A network as claimed in Claim 3 or Claim 4, wherein the diode-equivalent is constituted by a further transistor the collector and the emitter of which constitute respective terminals of the diode-equivalent, the collector of said further transistor being connected to its base via a third resistor and said second resistor being included between the collector of the further transistor and the base of the first transistor.

6. A network as claimed in any preceding Claim, wherein each section includes an additional transistor the collector-emitter path of which is connected in parallel with the resistor of Claim 1 and a controllable current source connected to the base of said additional transistor for controlling conduction in said additional transistor.

7. A network as claimed in Claim 6, characterized in that direct current through the resistor of Claim 1 is compensated for by a bridge of current sources.

8. A network as claimed in Claim 6 or Claim 7, wherein the controllable current sources included in the various sections are intercoupled so that they are controllable simultaneously and to the same degree by means of a single control signal.

9. A network as claimed in any of the preceding Claims, wherein each said amplifier circuit arrangement includes an additional amplifier having controllable gain and having its input coupled to the first input of the corresponding amplifier circuit arrangement.

10. A transversal filter comprising a network as claimed in Claim 9, the outputs of said additional amplifiers being collectively coupled to a single output.

section, which is also the input current of the next section, is obtained by summation of the currents in the two branches. The necessary corrections can be obtained with the aid of the current sources I_a, I_c and I_h, whilst the magnitude of the current i_t on the tapping electrodes 21, 22 can be adjusted with the aid of the current source I_k. In a practical emobidment the resistors R_a, R_b and R_c and values of 100, 200 and 200 Ohms respectively, the capacitor C was constituted by a nitride dielectric and had a value of 30 pF, and the parasitic capacitance in parallel with the transistor 2 was 10 pF.

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CLAIMS

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2. A network as claimed in Claim 1, wherein the current mirror comprises a first transistor, a diode or diode-equivalent connected in parallel with the base-emitter path of said first transistor, and a second transistor the base-emitter path of which shunts the collector-base path of the first transistor, said one input of the amplifier circuit arrangement being connected to the base of the second transistor, said other input of the amplifier circuit arrangement being connected to the base of the first transistor, and the collector of the second transistor being connected to the common output of the amplifier circuit arrangement.

3. A network as claimed in Claim 1, wherein the current mirror comprises a first transistor, a diode or diode-equivalent connected in parallel with the base-emitter path of said first transistor and a second resistor included in a connection from the diode or diode-equivalent to the first transistor, said one input of the amplifier circuit arrangement being connected to the diode or diode-equivalent, and the collector of the first transistor being connected to the output of the amplifier circuit arrangement.

4. A network as claimed in Claim 2, including a second resistor in a connection from the diode or diode-equivalent to the first transistor.

5. A network as claimed in Claim 3 or Claim 4, wherein the diode-equivalent is constituted by a further transistor the collector and the emitter of which constitute respective terminals of the diode-equivalent, the collector of said further transistor being connected to its base via a third resistor and said second resistor being included between the collector of the further transistor and the base of the first transistor.

6. A network as claimed in any preceding Claim, wherein each section includes an additional transistor the collector-emitter path of which is connected in parallel with the resistor of Claim 1 and a controllable current source connected to the base of said additional transistor for controlling conduction in said additional transistor.

7. A network as claimed in Claim 6, characterized in that direct current through the resistor of Claim 1 is compensated for by a bridge of current sources.

8. A network as claimed in Claim 6 or Claim 7, wherein the controllable current sources included in the various sections are intercoupled so that they are controllable simultaneously and to the same degree by means of a single control signal.

9. A network as claimed in any of the preceding Claims, wherein each said amplifier circuit arrangement includes an additional amplifier having controllable gain and having its input coupled to the first input of the corresponding amplifier circuit arrangement.

10. A transversal filter comprising a network as claimed in Claim 9, the outputs of said additional amplifiers being collectively coupled to a single output.

11. An electrical delay network substantially as described herein with reference to any of Figures 1, 2 and 13 of the drawings in conjunction with Figure 3, Figure 4 or Figure 11 of the drawings or in conjunction with Figure 3 or Figure 4 of the drawings when modified in accordance with any of Figures 5 to 10 of the drawings.

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