A METHOD AND APPARATUS FOR A SINGLE-WORD ALIGNMENT IN A PAGE-READ OPERATION

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to the field of memory devices; more particularly, the present invention relates to a method and apparatus for providing single-word alignment in a page-read operation.

2. Description of Related Art

Central processing unit (CPU) based systems, such as computers and embedded systems, process data and instructions stored in a memory. The memory is often organized in blocks of data corresponding to cache lines. Each cache line contains multiple pages and each page contains multiple words. For example, a common organization is 16-word cache lines, each cache line containing four 4-word pages, each word containing 8 bits.

The CPU generates read requests to the memory. When the memory receives a burst read request in which the first word is aligned with a 4-word page boundary, the memory loads the page corresponding to the first word into a page buffer and generates a burst cycle to provide the 4 words to the CPU. While the memory generates the burst cycle corresponding to the first page, the memory loads an adjacent page to continue the burst cycle using the four words of the adjacent page. Thus, long sequences of pages may be provided in a continuous burst cycle containing a series of 4-word burst cycles.

If the time to load the adjacent page into one page buffer is greater than the time to generate a burst cycle for the words in other page buffer, wait states are inserted between the words from each page buffer at 4-word page boundaries. Wait states are inactive states that are inserted when the memory cannot provide the requested information during a particular bus cycle. Generally, wait states reduce the performance of the bus. Reduced bus performance often reduces the performance of the CPU-based device.

Memories are often designed to store the adjacent page into a page buffer before a 4-word burst cycle for the prior page is completed so that the memory can generate a continuous burst cycle of multiple 4-word-aligned pages. However, if the first word is not aligned with a page boundary, the burst cycle provides less than all 4 words in the page buffer before an adjacent page is needed to provide the next word in the sequence. Since non-aligned read requests provide fewer words before using the adjacent page than an aligned read request, there is less time for the memory to fetch the adjacent page before the requested words of the prior page are provided. Thus, the memory often inserts wait states at 4-word page boundaries of non-aligned read requests. Such wait states often reduce performance of CPU-based systems.

What is needed is a method and apparatus to avoid wait states between page boundaries of non-aligned burst read requests.

SUMMARY OF THE INVENTION

A method and apparatus for performing non-N-word-aligned burst cycles, the method comprising the steps of: receiving a first non-N-word-aligned burst cycle request; loading a first portion of a first N-word aligned page and a first portion of a second N-word-aligned page into a first buffer; and accessing the first buffer to generate a first N-word burst cycle.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates one embodiment of a method of performing a non-4-wordaligned burst cycle.

FIG. 2 illustrates one embodiment of a method of perform a 4-word aligned read starting at word 0 (WO).

FIG. 3 illustrates one embodiment of a method of perform a non-4-word aligned read starting at word 1 (W 1).

FIG. 4 illustrates one embodiment of a method of perform a non-4-word aligned read starting at word 2 (W2).

FIG. 5 illustrates one embodiment of a method of perform a non-4-word aligned read starting at word 3 (W3).

FIG. 6 illustrates one embodiment of an apparatus for performing non-4-wordaligned burst cycles.

FIGS. 7a and 7b illustrates one embodiment of a method of for performing non4-word-aligned burst cycles using the apparatus of FIG: 6.

DETAILED DESCRIPTION

The present invention is a method and apparatus to avoid wait states between page boundaries of non-N-word-aligned burst read requests.

In one embodiment, a cache line includes 16 words: a word 0 (WO), a word 1 (WI), a word 2 (W2) and a word 3 (W3), a word 4 (W4), a word 5 (W5), a word 6 (W6), a word 7 (W7), a word 8 (W8), a word 9 (W9), a word 10 (W 10) and a word 11 (W 11), a word 12 (W 12), a word 13 (W 13), a word 14 (W 14) and a word 15 (W 15). The cache line includes four 4-word-aligned pages. The first 4-word-aligned page includes W0, W 1, W2 and W3, the second 4-word-aligned page includes W4, W5, W6 and W7, the third 4-word-aligned page includes W8, W9, W 10 and W 11, and the fourth 4-word-aligned page includes W 12, W 13, W 14 and W 15.

FIG. 1 illustrates one embodiment of a method of performing a non-4-wordaligned burst cycle.

In step 700, a non-4-word-aligned burst read request is received. For example, a burst read request starting at W 1 is received.

In step 710, a portion of a first 4-word-aligned page and a portion of a second 4word-aligned page are loaded into a first page buffer. For example, W 1, W2 and W3 are loaded from the first 4-word-aligned page and W4 is loaded from the second 4word-aligned page and these four words are stored as W4, W 1, W2 and W3 in the first page buffer.

In step 720, the first page buffer is accessed to generate a first 4-word burst cycle. For example, the first 4-word burst cycle generates W 1, W2, W3 and W4.

In step 730, a portion of the second 4-word-aligned page and a portion of a third 4-word-aligned page are loaded into a second page buffer. For example, W5, W6 and W7 are loaded from the second 4-word-aligned page and W8 is loaded from the third 4 word-aligned page and these four words are stored as W8, W5, W6 and W7 in the second page buffer.

In step 740, the second page buffer is accessed to generate a 4-word burst cycle. For example, the second 4-word burst cycle generates W5, W6, W7 and W8.

FIGS. 2 through 5 illustrate memories having pairs of page buffers storing different portions of the cache line described above. It will be apparent to one skilled in the art that the memory array, address decoding and bit-routing circuitry and other necessary portions of a functional memory are not shown. Details of one embodiment of the address decoding and bit-routing circuitry are shown with reference to FIG. 6.

4-Word-Aligned Burst Read Starting t WO

FIG. 2 illustrates a memory 650 having a pair of page buffers, a page buffer 600 and a page buffer 601, each storing a 4-word-aligned page.

The memory 650 first loads the page buffer 600 with W0, W 1, W2 and W3 in response to a read request starting at W0. While the memory 650 generates a first burst cycle providing W0, Wl, W2, and W3, the memory 650 also loads the page buffer 601 with W4, W5, W6 and W7. The memory 650 generates a second burst cycle providing W4, W5, W6 and W7 without any wait states between the first and second burst cycles.

The memory 650 loads the next 4-word aligned page, W8, W9, W 10 and W 11, in the page buffer 600 while the memory 650 generates the second burst cycle providing W4, W5, W6 and W7. The memory 650 generates a third burst cycle without any wait states between the second and third burst cycles. Similarly, subsequent burst cycles can be generated to provide a continuous burst sequence of multiple pages.

Burst reads starting at W4, W8, and W12 are handled in a similar manner.

Non-4-Word-Aligned Burst Read Starting t W1

A prior art memory typically loads a first page buffer with W0, W 1, W2 and W3, in response to a burst read request starting at W 1. While the prior art memory provides the first three words of the first burst cycle, W 1, W2, and W3, the prior art memory loads the second page buffer with W4, W5, W6 and W7. Since only 3 words are output in the first burst cycle before a word from the second page buffer is required, the prior art memory has less time to load the second page buffer and generate the last word of the first burst cycle than the memory does during an aligned burst read.

Similarly, while the prior art memory provides the first three words of the second burst cycle, W5, W6, and W7, the prior art memory loads the first page buffer with W8, W9, W 10 and W 11. Since only 3 words are output in the second burst cycle before a word from the first page buffer is required, the prior art memory has less time to load the first page buffer and generate the last word of the second burst cycle than the memory does during an aligned burst read described with reference to FIG. 1. Thus, prior art memories insert wait states between the first 3-words and the last word of each burst cycle in response to a burst read request starting at W 1.

FIG. 3 illustrates a memory 651 having a pair of page buffers, a page buffer 610 and a page buffer 611, each storing a non-4-word-aligned page. A non-4-word-aligned page includes words from two 4-word aligned pages.

In contrast to the prior art memory described above, the memory 651 first loads the page buffer 610 with W4, W l, W2 and W3 in response to a burst read request starting at Wl. While the memory generates a first burst cycle providing Wl, W2, W3, and W4, the memory 651 loads the page buffer 611 with W8, W5, W6 and W7. Since all four words of the first burst cycle are in the page buffer 610, no words are required from page 611 during the first burst cycle. Thus, the memory 651 generates the first burst cycle without any wait states.

Similarly, the memory 651 provides W5, W6, W7 and W8, during the second burst cycle without any wait states. Next, W 12, W9, W 10 and W 11, can

be loaded in the page buffer 610 while the memory 651 generates the second burst cycle providing W5, W6, W7 and W8. Thus, the memory 651 can generate a third burst cycle without any wait states. Subsequent burst cycles can be generated to provide a continuous burst sequence of multiple pages without any wait states.

Burst reads starting at W5, W9, and W 13 are handled in a similar manner.

In one embodiment, a 16-word burst read at W 13 wraps around to WO of the current line. Thus, the memory loads the page buffer with W0, W 13, W 14, and W 15. Thus, WO of the current cache line is produced to complete a cache line fill, for example. Four burst cycles for a cache line fill starting at W 1 include a first burst cycle of W l, W2, W3 and W4, a second burst cycle of W5, W6, W7 and W8, a third burst cycle of W9, W 10, W 11 and W 12, and a fourth burst cycle of W 13, W 14, W 15 and W0.

Alternatively, a continuous burst read at W13 continues to WO of the adjacent cache line. In one embodiment, the cache buffer loads the page buffer with WO (of the current cache line), W 13, W 14 and W 15, but discards the WO of the current cache line. After generating W 13, W 14, and W 15 of the current cache line, the memory inserts one or more wait cycles while it loads the adjacent cache line.

The memory then generates subsequent cache line accesses starting at WO of that cache line such that subsequent accesses are 4-word-aligned. At the next cache line boundary, the 4-word-aligned read produce a complete 4-word burst cycle to allow the memory time to load the adjacent page from the adjacent cache line. Subsequent reads in the continuous burst cycle are 4-word-aligned. Thus, wait states are only generated at e first cache line boundary in a continuous burst that crosses multiple cache line boundaries.

Non-4-Word-Aligned Burst Read Starting t W2

A prior art memory typically loads a first page buffer with W0, W l, W2 and W3, in response to a burst read request starting at W2. While the prior art

memory provides the first two words of the first burst cycle, W2, and W3, the prior art memory loads the second page buffer with W4, W5, W6 and W7. Since only 2 words are output in the first burst cycle before a word from the second page buffer is required, the prior art memory has less time to load the second page buffer and generate the last two words of the first burst cycle than the memory does during an aligned burst read. Prior art memories often insert wait states between the first two words and the last two words of each burst cycle in response to a burst read request starting at W2.

FIG. 4 illustrates a memory 652 having a pair of page buffers, a page buffer 620 and a page buffer 621, each storing a non-4-word-aligned page.

In contrast to the prior art memory described above, the memory 652 first loads the page buffer 620 with W4, W5, W2 and W3 in response to a burst read request starting at W2. While the memory generates a first burst cycle providing W2, W3, W4, and W5, the memory 652 loads the page buffer 621 with W8, W9, W6 and W7. Since all four words of the first burst cycle are in the page buffer 620, no words are required from page 621 during the first burst cycle. Thus, the memory 652 generates the first burst cycle without any wait states.

Similarly, the memory 652 provides W6, W7, W8 and W9, during the second burst cycle without any wait states. Next, W 12, W 13, W10 and W 11, can be loaded in the page buffer 620 while the memory 652 generates the second burst cycle providing W6, W7, W8 and W9. Thus, the memory 652 can generate a third burst cycle without any wait states. Subsequent burst cycles can be generated to provide a continuous burst sequence of multiple pages without any wait states.

Burst reads starting at W6, W 10, and W14 are handled in a similar manner.

In one embodiment, a 16-word burst read at W 14 wraps around to WO and W 1 of the current line. The memory loads the page buffer with W0, W 1, W 14, and W 15. Thus, WO and W 1 of the current cache line are produced to complete a cache line fill, for example.

Alternatively, a continuous burst read at W 14 continues to WO and W 1 of the adjacent cache line. In one embodiment, the cache buffer loads the page buffer with WO and W 1 (of the current cache line), W 14 and W 15, but discards the WO and W 1 of the current cache line. After generating W14 and W 15, the memory inserts one or more wait cycles while it loads the adjacent cache line. The memory then generates subsequent cache line accesses starting at WO of that cache line such that subsequent accesses are 4-word-aligned. Thus, wait states are only generated at the first cache line boundary in a continuous burst that crosses multiple cache line boundaries.

Non-4-Word-Aligned Burst Read Starting at W3

A prior art memory typically loads a first page buffer with W0, W 1, W2 and W3, in response to a burst read request starting at W3. While the prior art memory provides the first word of the first burst cycle, W3, the prior art memory loads the second page buffer with W4, W5, W6 and W7. Since only 1 word is output in the first burst cycle before a word from the second page buffer is required, the prior art memory has less time to load the second page buffer and generate the last three words of the first burst cycle than the memory does during an aligned burst read. Prior art memories often insert wait states between the first word and the last three words of each burst cycle in response to a burst read request starting at W3.

FIG. 5 illustrates a memory 653 having a pair of page buffers, a page buffer 630 and a page buffer 631, each storing a non-4-word-aligned page.

In contrast to the prior art memory described above, the memory 653 first loads the page buffer 630 with W4, W5, W6 and W3 in response to a burst read request starting at W3. While the memory generates a first burst cycle providing W3, W4, W5, and W6, the memory 653 loads the page buffer 631 with W8, W9, W10 and W7. Since all four words of the first burst cycle are in the page buffer 630, no words are required from page 631 during the first burst cycle. Thus, the memory 653 generates the first burst cycle without any wait states.

Similarly, the memory 653 provides W7, W8, W9 and W 10, during the second burst cycle without any wait states. Next, W 12, W 13, W14 and W 11, can be loaded in the page buffer 630 while the memory 653 generates the second burst cycle providing W7, W8, W9 and W 10. Thus, the memory 653 can generate a third burst cycle without any wait states. Subsequent burst cycles can be generated to provide a continuous burst sequence of multiple pages without any wait states.

Burst reads starting at W7, W11, and W15 are handled in a similar manner.

In one embodiment, a 16-word burst read at W15 wraps around to W0, W1, W2 of the current line. The memory loads the page buffer with W0, W1, W2, and W15. Thus, W0, W1, and W2 of the current cache line fill for example.

Alternately, a continuous burst read at W15 continues to W0, W1, and W2 of the adjacent cache line. In one embodiment, the cache buffer loads the page buffer with W0, W1, and W2 (of the current cache line), and W15, but discards the W0, W1, and W2 of the current cache line. After generating W15, the memory inserts one or more wait cycles while it loads the adjacent cache line. The memory then generates subsequent cache line accesses starting at W0 of that cache line such that subsequent accesses are 4 word-aligned. Thus, wait states are only generated at the first cache line boundary in a continuous burst that crosses multiple cache line boundaries.

Memory Device Including A Burst Control and A Bit-routing Circuit

FIG. 6 illustrates one embodiment of an apparatus for performing non-4-wordaligned burst cycles.

The memory device includes a memory array 100, a bit-routing circuit 190, and burst control circuit 195. The memory array 100 is configured to provide a line of data corresponding to line selector in response to a read request indicated by the read signal. The bit-routing circuit 190 is coupled to receive line bits that correspond to an output signal Wo. The burst control circuit 195 generates the control signals that route selected line bits to be the burst bits. The

burst control circuit 195 also generates the burst pointer that sequences through the burst bits to produce the burst sequence on the output signal Wo.

Although one bit-routing circuit is shown, multiple bit-routing circuits may be used to receive the other bits associated with each page of the line. For example, if the memory device generated byte-wide output data, 8 bit-routing circuits may be used to produce the byte output. Each of the 8 bit-routing circuits receives the same control signals from the burst control circuit 195.

The memory array 100 is coupled to receive a line selector signal and a read signal. When the read signal is asserted, the memory reads the line bits corresponding to the selected line of the memory array 100. The bit-routing circuit 190 receives the line bits including b0 (bit corresponding to WO), b1 (bit corresponding to W 1), b2 (bit corresponding to W2) and b3 to b 15. b3 to b 15 correspond to W3 to W15, respectively.

The bit-routing circuit 190 receives a word selector 170 (including A0, A1, A2, and A3), a word selector 171 (including B0, B1, B2, and B3), a word selector 172 (including C0, C1, C2, and C3), and a word selector 173 (including D0, D1, D2, and D3). Transistor T0 is coupled to pass b0 to WA if A0 is asserted. Transistor T1 is coupled to pass b4 to WA if A1 is asserted. Transistor T2 is coupled to pass b8 to WA if A2 is asserted. Transistor T3 is coupled to pass b12 to WA if A3 is asserted. A sense amp/latch 135 is coupled to receive WA and generate a latched signal LWA.

Transistor T5 is coupled to pass b1 to WB if B0 is asserted. Transistor T6 is coupled to pass b5 to WB if B1 is asserted. Transistor T6 is coupled to pass b9 to WB if B2 is asserted. Transistor T7 is coupled to pass b13 to WB if B3 is asserted. A sense amp/latch 140 is coupled to receive WB and generate a latched signal LWB.

Similarly, Transistors T8, T9, T10, and T11 are coupled to pass b2, b6, b10, or b14 to WC depending on whether C0, C1, C2, or C3, respectively, is asserted. A sense amp/latch 145 is configured to receive WC and generate a latched signal LWC.

Transistors T12, T13, T14, and T15 are coupled to pass b3, b7, b11, or b15 to WD depending on whether D0, D1, D2, or D3, respectively, is asserted. A sense amp/latch 150 is configured to receive WD and generate a latched signal LWD.

A 4:1 Multiplexor (MUX) 160 is coupled to receive the burst bits (LWA, LWB, LWC, and LWD) and the burst pointer and generate the burst sequence on the output signal Wo.

The burst control circuit 195 is coupled to receive a start page which selects a page that contains the first requested word, a start word which selects the first requested word in selected page, and a burst type signal that identifies the type of burst cycle requested.

The shifter control 130 is configured to receive the start word and the burst type and generate a cntla signal, a cntlb signal, a sntlc signal, and a cntld signal (control signals). The control signals specify the direction and umber of bits of a particular shifter in a particular shifter. For exapmle, the cntla signal may specify a 2-bit right shift to the shifter 110. It will be apparaent that the shifter control logic can be configured to generate control signals for numerous combinations of start word values and burst-type values.

A 2 to 4 Decoder 105 is coupled to receive the start page and generate a decoded start page signal. A shifter 110 is coupled to receive the decoded start page signal and shift the bits in response to a ctrla signal to produce the line selector 170 signal. Similarly, a shifter 115, a shifter 120, a shifter 125 are coupled to receive the decoded start page selector and produce the word selector 171, the word selector 172, and the word selector 173 in response to a ctrlb signal, a ctrlc signal, and a ctrld signal, respectively.

A counter 155 is coupled to receive the start word signal and the burst-type signal and generate a burst pointer signal. In one embodiment, the counter 155 generates a sequence of values on the burst pointer signal that start with the value of start word and increment by one, wrapping around to zero at four. Alternatively, the counter 155 generates a sequence of values on the burst pointer signal that start with the value of start word and decrements by one,

wrapping around to four at zero. The burst bits may provide to the output bit Wo in other orders dependent on the burst-type signal.

FIGS. 7a and 7b illustrates one embodiment of a method for performing non-4word-aligned burst cycles using the apparatus of FIG. 6

In order to illustrate the method, the method is applied to the apparatus of FIG. 6 using a non-4 word-aligned burst read starting at W 10 of line 200 in a 256-line memory. The line contains a single bit corresponding to each word in the line. In this example, the 12-bit address signal is 110010001010_2. In one embodiment, the start word is the least significant two bits of the address signal, IO_2, and the line selector is the 10 most-significant bits of the address signal, 11001000_2.

In step 800, a line of data is received. A read signal is asserted to the particular line selected using line selector signal. In the example, the line selector signal is 11001000_2 to select line 200 of the memory array 100 to be driven onto bits b0 to b15.

In step 805, a start page is received. In the example, the start page signal is 10, to select page 2 since page 2 includes W 10.

In step 810, the start page is decoded to provide a decoded start page. In the example, the start page of 102 is decoded to produce a decoded start page of 01002. In step 815, the burst type is received. In one embodiment, the burst type specifies whether the burst counter should increment from the start word or decrement from the start word. Alternatively, the burst type may specify one of multiple burst sequences within each page.

In step 820, the start word is received. In the example, the start word is 102. A start word of 102 and a start page of 102 indicates that the second word within the second page is the first requested word. W10 is word 2 of page 2.

In step 825, the decoded start page is shifted to generate a word selector 170 according to the start word and burst-type signal. The word selector 170 select one of the first set of page bits, b0, b4, b8 and b 12, corresponding to the selected word.

In one embodiment, the shifter 110 produces the word selector 170 by shifting the decoded page selector left (towards most significant bit) by 1 when the start word is not zero (for non-4-word aligned burst cycles) and not shifting the line selector at all when the start word is zero (for 4-word-aligned burst cycles). Alternatively, other shifting algorithms may be used. In one embodiment, the shifting algorithm depends on the burst type signal.

In the example, the shifter 110 receives the decoded start page, 01002, and the word selector, 102, and left shifts the decoded start page of ol00z by one to generate a word selector 170 of 1000_2.

In one embodiment, the shifter is a barrel shifter such that in a left shift, the most significant bit shifts through to the least significant bit. Thus, when the decoded start page is 1000_2, a left shift of 1 generates a word selector 170 of 0001_2. This corresponds to the burst read starting at W 15 causing the page buffer to load W0, W 1, W2 and W 15 as described herein.

In step 830, the word selector 170 is used to select one of the first set of line bits. A3, the most significant bit of the word selector 170 is coupled to the gate of transistor T3 to select b12. A2, the second most significant bit of the word selector 170 is coupled to the gate of transistor T2 to select b8. Al, the second least significant bit of the word selector 170 is coupled to the gate of transistor Tl to select b4. A0, the least significant bit of the word selector 170 is coupled to the gate of transistor TO to select b0. In the example, A3 is asserted and b12 is selected.

In step 835, the decoded start page is shifted to generate a select one of the second set of line bits, b 1, b5, b9 and b 13, according to the start word selector.

In one embodiment, the shifter 115 produces the line selector 171 by shifting the decoded start page left (towards most significant bit) when the start word is neither zero nor one and not shifting the line selector at all when the word selector is zero or one. Other shifting algorithms may be used. In one embodiment, the shifting algorithm depends on the burst-type signal.

In the example, the shifter 115 receives the decoded start page, O 100_2, and the word selector, 10_2, and left shifts the decoded start page by one to generate the word selector 171 of 1000_2.

In step 840, the word selector 171 is used to select one of the second set of bits. B3, the most significant bit of the word selector 171 is coupled to the gate of transistor T7 to select b13. B2, the second most significant bit of the word selector 171 is coupled to the gate of transistor T6 to select b9. B 1, the second least significant bit of the line selector 171 is coupled to the gate of transistor T5 to select b5. B0, the least significant bit of the word selector 171 is coupled to the gate of transistor T4 to select b1.

In the example, B3 is asserted and b13 is selected.

In step 845, the decoded start page is shifted to select one of the second set of burst bits, b2, b6, b 10 and b 14, according to the page and word selector.

In one embodiment, the shifter 120 produces the word selector 172 by shifting the decoded page selector left (towards most significant bit) when the word selector 172 is three and not shifting the line selector at all when the word selector is not three. Other shifting algorithms may be used. In one embodiment, the shifting algorithm depends on the burst-type signal.

In the example, the shifter 120 receives the decoded start page, 0100_2, and the word selector, 10_2, and does not shift the decoded start page to produce the word selector 172 of 0100_2.

In step 850, the word selector 172 is used to select one of the third set of bits. C3, the most significant bit of the word selector 172 is coupled to the gate of transistor T1 I to select b14. C2, the second most significant bit of the word selector 172 is coupled to the gate of transistor T10 to select b10. C1, the second least significant bit of the word selector 172 is coupled to the gate of transistor T9 to select b6. C0, the least significant bit of the word selector 172 is coupled to the gate of transistor T8 to select b2.

In the example, C2 is asserted and b10 is selected.

In step 855, the decoded start page is shifted to generate a select one of the fourth set of burst bits, b3, b7, b 11 and b 15 according to the start word.

In one embodiment, the shifter 125 does not shift the decoded start page independent of the start word. Other shifting algorithms may be used. In one embodiment, the shifting algorithm depends on the burst-type signal.

In the example, the shifter 125 receives the decoded start page, 0100_2, and the word selector, 10, and does not shift the decoded start page to produce the line selector 173 of 0100_2.

In step 860, the word selector 173 is used to select one of the fourth set of bits. D3, the most significant bit of the word selector 173 is coupled to the gate of transistor T15 to select b15. D2, the second most significant bit of the word selector 173 is coupled to the gate of transistor T14 to select bl 1. Dl, the second least significant bit of the word selector 173 is coupled to the gate of transistor T13 to select b7. D0, the least significant bit of the word selector 173 is coupled to the gate of transistor T 12 to select b3.

In the example, D2 is asserted and b11 is selected.

Thus, the burst bits are stored in the page buffer. In the example, the page buffer holds burst bits, b12, b13, bl0 and bl1, at the output of the sense amp/latch 135, the sense amp/latch 140, the sense amp/latch 145, and the sense amp/latch 150, respectively.

In step 865, each of the four burst bits is selected sequentially according to the burst order specified by the burst-type signal. In the example, the burst pointer is generated by incrementing from the start word wrapping around to 0 at 4.

In the example, the burst pointer sequences through the values 2, 3, 0 and 1 to select the burst bits in the page buffer to generate a burst sequence in the following order: bl0, b11, b12 and b13.

As described herein, two page buffers are used to sequence through a multiple page burst sequence. The second page buffer is a second set of latches in sense amp/latch 135 to sense amp/latch 150 that can receive the signal WA through WD, respectively, when the second page is selected to be loaded. The mux 160 is configured to receive the burst bits from the second page when the second page is selected to be read.

The present invention may be applied to numerous devices. The memory is not limited to a particular storage technology. For example, the memory may be a dynamic random access memory (DRAM), a static random access memory (SRAM), or an electrically eraseable programmable read only memory (EEPROM). Any memory capable of storing and retreiving data according to an embodiment of the method of the invention may be used.

The present invention is disclosed herein with respect to a cache line having four 4-word pages. However, the present invention may be practiced using other memory organizations. For example, the cache line may include more or less than 16 words, there may be more or less than 4 pages, and each page may include more or less than 4 words. In one embodiment, each word contains 8 bits. However, the present invention may be practiced using other size words.

The present invention is disclosed herein with respect to burst cycles that increment sequentially or decrement sequentially through the words. However, it will be apparent to one skilled in the art that more complex burst cycles may be implemented within the spirit and scope of the present invention. The words from each 4-word burst may be output non-sequentially. For example, one such order is W0, W2, W1, W3. Furthermore, the access to a subsequent cache line in a continuous burst cycle may access a non-adjacent cache line.

CLAIMS



What is claimed is:

1. A method comprising the steps of:

receiving a first non-N-word-aligned burst cycle request;

loading a first portion of a first N-word aligned page and a first portion of a second N-word aligned page into a first buffer; and

accessing the first buffer to generate a first N-word burst cycle.

2. The method of Claim 1 wherein the first N-word burst cycle has no wait states.

3. The method of Claim 1 further comprising the steps of:

loading a second portion of the second N-word aligned page and a first portion of a third N-word aligned page into a second buffer; and

accessing the second buffer to generate a second N-word burst cycle.

4. An apparatus comprising a first page buffer comprising a first portion of a first N-word aligned page and a first portion of a second word aligned page.

5. The apparatus of Claim 4 wherein the apparatus is configured to generate a non-N-word aligned burst cycle comprising the first portion of the N-word aligned page and a first portion of the second N-word aligned page, the non-N-word-aligned burst cycle not having any wait states.

6. An apparatus comprising:

a first circuit configured generate a first control signal in response to a first portion of a pointer;

a first shifter configured to shift a second portion of the pointer in response to the first control signal to produce a first selector signal; and

a second circuit coupled to receive a first plurality of bits and generate a first bit, the first bit being selected from the first plurality of bits by the first selector signal.

7. The apparatus of Claim 6 further comprising a memory configured to produce the first plurality of bits, the first portion of the pointer indicating a

page within the line, and the second portion of the pointer indicating a word within the page.

8. The apparatus of Claim 6 wherein the first circuit is coupled to receive a burst type signal and generate the first control signal in response to the burst type signal.

9. The apparatus of Claim 6 further comprising:

a third circuit configured to receive the first portion of the pointer and generate a burst pointer; and

a multiplexor coupled to receive the first bit and a second bit and generate a third bit corresponding to the one of the first bit or second bit indicated by the burst pointer.

10. The apparatus of Claim 9 wherein the third circuit is coupled to receive a burst type signal and generate a plurality of burst pointers, the plurality of burst pointers being determined by performing a sequence of operations on the first portion of the pointer, the multiplexor generating a third plurality of bits, each of the third plurality of bits corresponding to one of the plurality of burst pointers.

11. The apparatus of Claim 9 further comprising:

a fourth circuit configured to generate a second control signal in response to a first portion of the pointer;

a second shifter configured to shift the first portion of the pointer in response to the second control signal to produce a second selector signal;

a fifth circuit coupled to receive a fourth plurality of bits and generate the second bit, the fifth bit being selected from the fourth plurality of bits by the second selector signal.

12. An apparatus comprising:

a first circuit configures generate a plurality of control signals in response to a first portion of a pointer;

a plurality of shifters, each of the plurality of shifters configured to shift a second portion of the pointer in response to a corresponding one of the plurality of control signals to produce a corresponding selector signal; and

a second circuit coupled to receive a first plurality of bits and generate a second plurality of bits, each of the second plurality of bits being selected from the first plurality of bits by the corresponding selector signal.

13. The apparatus of Claim 12 further comprising a memory configured to produce the first plurality of bits, the first portion of the pointer indicating a line within a page, and the second portion of the pointer indicating a word within the line.

14. The apparatus of Claim 12 wherein the first circuit is coupled to receive a burst type signal and generate the plurality of control signals in response to the burst type signal.

15. The apparatus of Claim 12 further comprising:

a third circuit configured to receive the first portion of the pointer and generate a burst pointer; and

a plurality of multiplexors coupled to receive the first plurality of bits and generate a third plurality of bits corresponding to the burst pointer.

16. The apparatus of Claim 12 wherein the third circuit is coupled to receive a burst type signal and generate a plurality of burst pointers, the plurality of burst pointers being determined by performing a sequence of operations on the first portion of the pointer.

17. A method comprising the steps of:

generating a first control signal based on a first portion of a pointer;

shifting a second portion of a pointer to produce a first selector signal in response to the first control signal; and

selecting a first bit of a first plurality of bits in response to the first selector signal.

18. The method of Claim 17 comprising the steps of:

generating a second control signal based on the first portion of the pointer;

shifting the second portion of a pointer to produce a second selector signal in response to the second control signal; and

selecting a second bit of a second plurality of bits in response to the second selector signal.

19. The method of Claim 17 comprising the steps of:

generating a burst pointer in response to a first portion of the pointer; and

selecting one of the first and second bits in response to the burst pointer.

20. The method of Claim 17 comprising the steps of reading a memory to produce the first plurality of bits.