**WHAT IS CLAIMED IS:**

1. A CMOS semiconductor fabrication process, comprising:

providing a first semiconductor layer;

forming NMOS and PMOS gate structures overlying the first semiconductor layer, each of the NMOS and PMOS gate structures having exposed gate sidewalls;

depositing a first contact etch stop layer over the NMOS and PMOS gate structures;

etching the first contact etch stop layer to form sidewall spacers adjacent to the NMOS and PMOS gate structures;

depositing a second contact etch stop layer over the NMOS and PMOS gate structures and the sidewall spacers;

where one of the first or second contact etch stop layers is a tensile material and the other of the first or second contact etch stop layers is a compressive or neutral material that acts as a hydrogen source.

2. The process of claim 1, where forming a first semiconductor layer comprises forming a layer of silicon containing semiconductor with <100> channel orientation.

3. The process of claim 1, where forming NMOS and PMOS gate structures comprises selectively etching implant spacers from the sidewalls of the NMOS and PMOS gate structures, where the implant spacers were used to form source/drain regions below the NMOS and PMOS gate structures.

4. The process of claim 1, where depositing the first contact etch stop layer comprises depositing a tensile contact etch stop layer over the NMOS and PMOS gate structures.

5. The process of claim 4, where depositing the second contact etch stop layer comprises depositing a neutral or compressive contact etch stop layer over the NMOS and PMOS gate structures and the sidewall spacers.

6. The process of claim 1, where depositing the first contact etch stop layer comprises depositing a neutral or compressive contact etch stop layer over the NMOS and PMOS gate structures.

7. The process of claim 7, where depositing the second contact etch stop layer comprises depositing a tensile contact etch stop layer over the NMOS and PMOS gate structures and the sidewall spacers.

8. The process of claim 1, where the NMOS and PMOS gate structures each comprise a high-k dielectric and a metal gate electrode.

9. The process of claim 1, where etching the first contact etch stop layer to form sidewall spacers comprises:

anisotropically etching the first contact etch stop layer to form tensile sidewall spacers that stress a channel region formed below the NMOS gate structure, where the tensile sidewall spacers have a width that is controlled to eliminate the formation of voids when the second contact etch stop layer is deposited.

10. The process of claim 1, where etching the first contact etch stop layer to form sidewall spacers comprises:

anisotropically etching the first contact etch stop layer to form neutral or compressive sidewall spacers that introduce hydrogen to passivate surface dangling bonds in a channel semiconductor below the PMOS gate structure, where the neutral or compressive sidewall spacers have a width that is controlled to eliminate the formation of voids when the second contact etch stop layer is deposited.

11. A CMOS fabrication process for forming a semiconductor integrated circuit, comprising:

providing a first semiconductor layer having a <100> channel orientation;

forming PMOS and NMOS gate structures over the first semiconductor layer, where the PMOS and NMOS gate structures comprise implant spacers formed on sidewalls of the PMOS and NMOS gate structures;

removing the implant spacers from the sidewalls of the PMOS and NMOS gate structures;

forming sidewall spacers adjacent to the PMOS and NMOS gate structures; and

forming an etch stop layer over the sidewall spacers and the PMOS and NMOS gate structures;

where one of the sidewall spacers or the etch stop layer is formed with a tensile material and the other of the sidewall spacers or the etch stop layer is formed with a hydrogen-rich material.

12. The CMOS fabrication process of claim 11, where forming PMOS and NMOS gate structures comprises:

forming a plurality of metal gate electrodes over a high-k containing dielectric layer that is formed on the first semiconductor layer; and

forming implant spacers on the sidewalls of each metal gate electrode that are used to implant source/drain regions in the first semiconductor layer.

13. The CMOS fabrication process of claim 11, where forming sidewall spacers comprises:

depositing a first tensile silicon nitride layer over the NMOS and PMOS gate structures; and

anisotropically etching the first tensile silicon nitride layer to form tensile sidewall spacers that stress a channel region formed below each NMOS gate structure, where the tensile sidewall spacers have a width that is controlled to eliminate the formation of voids when the etch stop layer is formed.

14. The CMOS fabrication process of claim 13, where forming an etch stop layer comprises depositing a layer of silicon nitride having an atomic percentage of at least six percent hydrogen.

15. The CMOS fabrication process of claim 11, where forming sidewall spacers comprises forming tensile sidewall spacers having a controlled width with a thickness in the range of approximately 150-400 Angstroms.

16. The CMOS fabrication process of claim 11, where forming sidewall spacers comprises:

depositing a hydrogen-rich silicon nitride layer over the NMOS and PMOS gate structures; and

anisotropically etching the hydrogen-rich silicon nitride layer to form sidewall spacers that act as a hydrogen source, where the sidewall spacers have a width that is controlled to eliminate the formation of voids when the etch stop layer is formed.

17. The CMOS fabrication process of claim 16, where forming an etch stop layer comprises depositing a tensile silicon nitride layer over the sidewall spacers and the PMOS and NMOS gate structures.

18. The CMOS fabrication process of claim 11, where forming sidewall spacers comprises forming hydrogen-rich sidewall spacers having a controlled width with a thickness in the range of approximately 50-200 Angstroms.

19. A semiconductor device comprising:

a semiconductor substrate having a <100> channel orientation;

PMOS and NMOS gate structures overlying the silicon substrate;

first spacer structures formed adjacent to the PMOS and NMOS gate structures after source/drain implantation; and

a contact etch stop layer formed over the PMOS and NMOS gate structures and the first spacer structures,

where either the first spacer structures or the contact etch stop layer is formed with a tensile material that stresses channel regions formed below the NMOS gate structures, and the other of the first spacer structures or the contact etch stop layer is formed with a hydrogen-rich material that introduces hydrogen to passivate dangling bonds in channel semiconductor regions below the PMOS gate structures.

20. The semiconductor device of claim 19, where the first spacer structures have a width that is controlled to eliminate the formation of voids when the contact etch stop layer is formed.

What is claimed is:

1. A CMOS semiconductor fabrication process, comprising:

providing a first semiconductor layer;

forming NMOS and PMOS gate structures overlying the first semiconductor layer, each of the NMOS and PMOS gate structures having exposed gate sidewalls;

depositing a first contact etch stop layer over the NMOS and PMOS gate structures;

anisotropically etching the first contact etch stop layer over the NMOS and PMOS gate structures to form sidewall spacers adjacent to the NMOS and PMOS gate structures;

depositing a second contact etch stop layer over the NMOS and PMOS gate structures and the sidewall spacers;

where one of the first or second contact etch stop layers is a tensile material and the other of the first or second contact etch stop layers is a compressive or neutral material that acts as a hydrogen source.

2. The process of claim 1, where forming a first semiconductor layer comprises forming a layer of silicon containing semiconductor with <100> channel orientation.

3. The process of claim 1, where forming NMOS and PMOS gate structures comprises selectively etching implant spacers from the sidewalls of the NMOS and PMOS gate structures, where the implant spacers were used to form source/drain regions below the NMOS and PMOS gate structures.

4. The process of claim 1, where depositing the first contact etch stop layer comprises depositing a tensile contact etch stop layer over the NMOS and PMOS gate structures.

5. The process of claim 4, where depositing the second contact etch stop layer comprises depositing a neutral or compressive contact etch stop layer over the NMOS and PMOS gate structures and the sidewall spacers.

6. The process of claim 1, where depositing the first contact etch stop layer comprises depositing a neutral or compressive contact etch stop layer over the NMOS and PMOS gate structures.

7. The process of claim 6, where depositing the second contact etch stop layer comprises depositing a tensile contact etch stop layer over the NMOS and PMOS gate structures and the sidewall spacers.

8. The process of claim 1, where the NMOS and PMOS gate structures each comprise a high-k dielectric and a metal gate electrode.

9. The process of claim 1, where anisotropically etching the first contact etch stop layer to form sidewall spacers comprises:

anisotropically etching the first contact etch stop layer to form tensile sidewall spacers that stress a channel region formed below the NMOS gate structure, where the tensile sidewall spacers have a width that is controlled to eliminate the formation of voids

when the second contact etch stop layer is deposited.

10. The process of claim 1, where anisotropically etching the first contact etch stop layer to form sidewall spacers comprises:

anisotropically etching the first contact etch stop layer to form neutral or compressive sidewall spacers that introduce hydrogen to passivate surface dangling bonds in a channel semiconductor below the PMOS gate structure, where the neutral or compressive sidewall spacers have a width that is controlled to eliminate the formation of voids when the second contact etch stop layer is deposited.

11. A CMOS fabrication process for forming a semiconductor integrated circuit, comprising:

providing a first semiconductor layer having a <100>channel orientation;

forming PMOS and NMOS gate structures over the first semiconductor layer, where the PMOS and NMOS gate structures comprise implant spacers formed on sidewalls of the PMOS and NMOS gate structures;

removing the implant spacers from the sidewalls of the PMOS and NMOS gate structures;

forming sidewall spacers adjacent to the PMOS and NMOS gate structures by depositing a silicon nitride layer over the PMOS and NMOS gate structures and anisotropically etching the silicon nitride layer over the PMOS and NMOS gate structures to form sidewall spacers adjacent to the PMOS and NMOS gate structures; and

forming an etch stop layer over the sidewall spacers and the PMOS and NMOS gate structures; where one of the sidewall spacers or the etch stop layer is formed with a

tensile material and the other of the sidewall spacers or the etch stop layer is formed with a hydrogen-rich material.

12. The CMOS fabrication process of claim 11, where forming PMOS and NMOS gate structures comprises:

forming a plurality of metal gate electrodes over a high-k containing dielectric layer that is formed on the first semiconductor layer; and

forming implant spacers on the sidewalls of each metal gate electrode that are used to implant source/drain regions in the first semiconductor layer.

13. The CMOS fabrication process of claim 11, where forming sidewall spacers comprises:

depositing a first tensile silicon nitride layer over the NMOS and PMOS gate structures; and

anisotropically etching the first tensile silicon nitride layer to form tensile sidewall spacers that stress a channel region formed below each NMOS gate structure, where the tensile sidewall spacers have a width that is controlled to eliminate the formation of voids when the etch stop layer is formed.

14. The CMOS fabrication process of claim 13, where forming an etch stop layer comprises depositing a layer of silicon nitride having an atomic percentage of at least six percent hydrogen.

15. The CMOS fabrication process of claim 11, where forming sidewall spacers

comprises forming tensile sidewall spacers having a controlled width with a thickness in the range of approximately 150-400 Angstroms.

16. The CMOS fabrication process of claim 11, where forming sidewall spacers comprises:

depositing a hydrogen-rich silicon nitride layer over the NMOS and PMOS gate structures; and

anisotropically etching the hydrogen-rich silicon nitride layer to form sidewall spacers that act as a hydrogen source, where the sidewall spacers have a width that is controlled to eliminate the formation of voids when the etch stop layer is formed.

17. The CMOS fabrication process of claim 16, where forming an etch stop layer comprises depositing a tensile silicon nitride layer over the sidewall spacers and the PMOS and NMOS gate structures.

18. The CMOS fabrication process of claim 11, where forming sidewall spacers comprises forming hydrogen-rich sidewall spacers having a controlled width with a thickness in the range of approximately 50-200 Angstroms.