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(21) International Application Number: PCT/US00/06258 (22) International Filing Date: 11 March 2000 (11.03.00) (30) Priority Data: 60/124,299 12 March 1999 (12.03.99) US (71) Applicant (for all designated States except US): INTERNATIONAL BUSINESS MACHINES CORPORATION [US/US]; New Orchard Road, Armonk, NY 10504 (US). (72) Inventor; and (75) Inventor/Applicant (for US only): CHU, Jack, O. [US/US]; 44 Shelbourne Lane, Manhasset Hills, NY 11040 (US). (74) Agent: TREPP, Robert, M.; IBM Corporation, Intellectual Property Law Dept., P.O. Box 218, Yorktown Heights, NY 10598 (US).		(81) Designated States: CN, JP, KR, SG, US, European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE). Published <i>With international search report.</i> <i>Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.</i>
(54) Title: HIGH SPEED GE CHANNEL HETEROSTRUCTURES FOR FIELD EFFECT DEVICES		
(57) Abstract A method and a layered heterostructure for forming high mobility Ge channel field effect transistors is described incorporating a plurality of semiconductor layers on a semiconductor substrate, and a channel structure of a compressively strained epitaxial Ge layer having a higher barrier or a deeper confining quantum well and having extremely high hole mobility for complementary MODFETs and MOSFETs. The invention overcomes the problem of a limited hole mobility due to alloy scattering for a p-channel device with only a single compressively strained SiGe channel layer. This invention further provides improvements in mobility and transconductance over deep submicron state-of-the art Si pMOSFETs in addition to having a broad temperature operation regime from above room temperature (425 K) down to cryogenic low temperatures (0.4 K) where at low temperatures even high device performances are achievable. 10 → 12 → 12C → 12B → 12A → 18 17, 39 16 15 14 13 19 29'-31' 28' 21'-27' 11		