SEMICONDUCTOR DEVICE HAVING FIELD ISOLATION AND A PROCESS FOR FORMING THE DEVICE

Abstract of the Disclosure

Narrow and wide, planar field isolation region (72, 74, 152, 172, 182) is formed by forming trenches (52, 54) within a substrate (10). For wide, planar field isolation regions (72, 152, 172, 182), the trenches (52) define at least one mesa (76, 150, 170, 180) within the field isolation region (72, 152, 172, 182). The trenches (52, 54) are filled with a material (62) that is polished or etched to form the planar field isolation region (72, 74, 152, 172, 182) where the wide, planar field isolation regions (72, 152, 172, 182) include the mesa(s) (76, 150, 170, 180). Etching can be used or by polishing with minimal, if any, dishing occurs because the widths of the trenches (52, 54) are kept relatively narrow (usually no more than five microns wide). Mesas (180) within a wide, planar field isolation region (182) can form linguistic characters to better identify the part number or mask set of the device. The planar field isolation region (72, 74, 152, 172, 182) can be formed near LOCOS-type field isolation regions when required for certain types of input protection circuits or high potential components.

Fig. 10 accompanies this abstract.