

ABSTRACT

A semiconductor device may include an insulating pattern on a first lower interlayer insulating layer, nanosheets vertically stacked on the insulating pattern, a gate electrode on the insulating pattern and surrounding the nanosheets, a source/drain region on one side of the gate electrode on the insulating pattern, and a source/drain contact electrically connected to the source/drain region. The source/drain region, the first lower interlayer insulating layer, and the insulating pattern may define a contact trench and the source/drain contact may fill the contact trench. The source/drain contact may include a barrier layer, a first filling layer between parts of the barrier layer in the contact trench, and a second filling layer in the contact trench under the first filling layer. The first filling layer may be multi grain and may have a first average grain size. The second filling layer may be single grain.

FIG. 2