

A METHOD FOR MAKING LOW-LEAKAGE DRAM STRUCTURES USING
SELECTIVE SILICON EPITAXIAL GROWTH (SEG) ON AN
INSULATING LAYER

ABSTRACT

Low leakage DRAMs are achieved using a silicon epitaxial layer over an insulator on memory cell areas. A $\text{SiO}_2/\text{Si}_3\text{N}_4$ hard mask is patterned leaving portions over the memory cell areas. Shallow trenches are etched in the substrate, and filled with an oxide which is polished back to the hard mask to form shallow trench isolation around the memory cell areas. The hard mask is removed to form recesses over the memory cell areas exposing the underlying insulating layer. Openings are etched in the insulating layer to provide a silicon-seed surface from which is grown a selective epitaxial layer extending over the insulating layer. After growing a gate oxide on the epitaxial layer, FETs and DRAM capacitors are formed on the epitaxial layer. The insulating layer under the epitaxy drastically reduces the capacitor leakage current and improves DRAM device performance. This self-aligning method increases cell density, and reduces processing cost.

FIG. 10