

SELF-ALIGNED TRENCH FORMATION

Field of Invention

[0001] Embodiments relate to methods for forming semiconductor structures, more specifically to methods for forming self-aligned trenches in semiconductor processing.

Background of Invention

[0002] One way that integrated circuit designers make faster and smaller integrated circuits is by reducing the separation distance between the individual elements that comprise the integrated circuit. This process of increasing the density of circuit elements across a substrate is typically referred to as “scaling” or increasing the level of device integration. In the process of designing integrated circuits with higher levels of integration, improved device constructions and fabrication methods have been developed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] Exemplary embodiments of the invention disclosed herein are illustrated in the accompanying drawings, which are not drawn to scale but are for illustrative purposes only:

[0004] **Figure 1** illustrates a cross-sectional view of a partially formed semiconductor device.

[0005] **Figure 2** illustrates a cross-sectional view of the partially formed semiconductor device of **Figure 1** after a photo mask has been used to pattern a hard mask.

[0006] **Figure 3** illustrates a cross-sectional view of the partially formed semiconductor device of **Figure 2** after the hard mask has been used to pattern a second hard mask.

[0007] **Figure 4** illustrates a cross-sectional view of the partially formed semiconductor device of **Figure 3** after certain layers have been patterned and spacers formed therein.

[0008] **Figure 5** illustrates a cross-sectional view of the partially formed semiconductor device of **Figure 4** after etching a first set of trenches into the substrate.

[0009] **Figure 6** illustrates a cross-sectional view of the partially formed semiconductor device of **Figure 5** after filling the trenches.

[0010] **Figure 7** illustrates a cross-sectional view of the partially formed semiconductor device of **Figure 6** after planarization.

[0011] **Figure 8** illustrates a cross-sectional view of the partially formed semiconductor device of **Figure 7** after selective etching of a placeholder layer from between filled trenches and deposition of a spacer material.

[0012] **Figure 9** illustrates a cross-sectional view of the partially formed semiconductor device of **Figure 8** after performing a spacer etch and subsequently selectively etching a second set of trenches into the substrate in a self-aligned manner.

[0013] **Figure 10** illustrates a cross-sectional view of the partially formed semiconductor device of **Figure 9** after the second set of trenches have been filled.

[0014] **Figure 11** illustrates a cross-sectional view of the partially formed semiconductor device of **Figure 10** after planarization stopping on an etch stop layer.

[0015] **Figure 12** illustrates a detail of a cross-sectional view of the partially formed semiconductor device of **Figure 11** after portions of the surface have been selectively recessed.

[0016] **Figure 13** illustrates a detail of a cross-sectional view of the partially formed semiconductor device of **Figure 12** after the etch stop layer has been removed.

[0017] **Figure 14** shows a top-down view of the semiconductor device of **Figure 13**.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0018] Disclosed herein are fabrication techniques for semiconductor structures including self-aligned trenches. Self-aligned trenches can be used as part of pitch doubling techniques, which promote device integration. The fabrication techniques described herein advantageously enable more precise etching, minimize stress to the substrate and/or promote planarity at the surface of the semiconductor structure.

[0019] **Figure 1** is a cross-sectional view of a partially formed semiconductor device including a substrate 110 over which several additional layers have been formed to

facilitate a masking process. The substrate **110** comprises one or more of a wide variety of suitable workpieces for semiconductor processing. In some embodiments, the substrate **110** includes semiconductor structures that have been fabricated thereon, such as doped silicon platforms. While the illustrated substrate **110** comprises a monocrystalline silicon wafer, in other embodiments the substrate **110** comprises other forms of semiconductor layers, which optionally include other active or operable portions of semiconductor devices. Substrate is also used herein to refer to the workpiece including integrated layers formed thereover.

[0020] As shown in **Figure 1**, in some embodiments an oxide layer **210** is grown or deposited on the substrate **110**. The oxide layer **210** may comprise a thin pad oxide with a thickness between about 30 Å and 150 Å. The oxide layer **210** can be deposited using a suitable deposition process, such as chemical vapor deposition (“CVD”) or physical vapor deposition (“PVD”), or is grown by oxidation of the underlying surface.

[0021] The partially formed semiconductor device of **Figure 1** also shows an etch stop **211** formed over the oxide layer **210** by a suitable deposition process such as CVD or PVD. The etch stop **211** serves as a stop layer for a later planarization step (e.g., a CMP stop layer), as will be described hereinbelow. Relative to conventional CMP stop layers, the etch stop **211** can be very thin, e.g., may have a thickness between about 20 Å and 150 Å, more particularly between about 50 Å and 100 Å. As will be appreciated from the description below, this thin etch stop can improve planarity for subsequent processing. In some embodiments, the etch stop **211** comprises nitride, such as silicon nitride (“Si₃N₄”). In other embodiments, the etch stop **211** comprises aluminum oxide (“Al₂O₃”) or another material against which a neighboring material, particularly silicon oxide, can be selectively etched by a chemical and/or mechanical etching process.

[0022] As shown in **Figure 1**, some embodiments also provide a placeholder material **212** formed above the etch stop **211**. Advantageously, the placeholder material **212** may have a thickness sufficient to provide space for the formation of a spacer material in a later step, as described hereinbelow. Thus, the placeholder material **212** may have a thickness suitable for later definition of a sidewall spacer height, such as between about 500 Å to 3000 Å, more particularly 800 Å to 1000 Å. In the illustrated embodiment, the placeholder material **212** comprises polysilicon, although other materials that are selectively

etchable with respect to surrounding materials, and particularly trench isolation materials, can also be used.

[0023] In accordance with embodiments of the present invention, a hard mask is provided for etching a first set of trenches. In the embodiment shown in **Figure 1**, two hard mask layers **213**, **214** are provided, the first hard mask layer **214** being used to pattern the second hard mask layer **213**, and the second hard mask layer **213** serving as the mask through which the first set of trenches will be etched. This embodiment is described in greater detail below, as this arrangement provides certain performance advantages, such as an improved aspect ratio for etching the first set of trenches. However, other embodiments are also possible wherein a first set of trenches is etched using only a single hard mask, such as by using a photomask to etch a carbon hard mask and then etching the trenches through the carbon hard mask. In still other embodiments, no hard mask is used at all and instead the first set of trenches are simply formed using a photomask.

[0024] Referring again to the embodiment illustrated in **Figure 1**, the second hard mask layer **213** is formed over the placeholder material **212** by any suitable deposition process such as CVD or PVD. The second hard mask layer **213** may comprise a form of silicon oxide, such as tetraethylorthosilicate ("TEOS"), and it may have a thickness between about 500 Å to 1500 Å, more particularly 800 Å to 1200 Å. The first hard mask layer **214** can comprise carbon, such as amorphous carbon. In particular, the amorphous carbon can be a form of transparent carbon that is highly transparent to light, such as is disclosed in A. Helmbold, D. Meissner, Thin Solid Films, 283 (1996), 196-203, the entire disclosure of which is incorporated herein by reference. The first hard mask layer **214** may have a thickness between about 1000 Å to 3000 Å, more particularly 1800 Å to 2200 Å. Accordingly, the fraction of the thickness of the second hard mask **213** as a percentage of the thickness of the first hard mask **214** is less than 100%, more particularly 30-70%, even more particularly 40-60%. This reduced thickness of second hard mask layer **213**, as compared to the first hard mask layer **214**, advantageously provides a lower aspect ratio when the first set of trenches are etched as compared to using the first hard mask **214** directly.

[0025] As shown in **Figure 1**, some embodiments also provide coatings **215**, **216** formed above the first hard mask **214**. A dielectric antireflective coating ("DARC") **215**

advantageously protects the first hard mask 214. The DARC 215 may comprise a silicon rich material, such as silicon oxynitride ("Si_xO_yN_z"). An organic bottom antireflective coating ("BARC") 216 may also be included at the interface with a photoresist 218.

[0026] The photoresist 218 shown in **Figure 1** provides the pattern for removing portions of the first hard mask 214 through photolithography and etching techniques. In some embodiments, as shown in **Figure 1**, the photoresist 218 provides a pattern of parallel lines (shown in cross-section in **Figure 1**; see also **Figure 13**) separated from each other by gaps. In some embodiments, such as when a high degree of device integration is desired, the width of the lines and the gaps between the lines may be approximately equal to "F", where F can be the minimum feature size formable using a particular photolithographic technique. In general, however, "F" is used in the figures to represent relative dimensions. The skilled artisan will appreciate that the methods described herein can be implemented where F is greater than the minimum resolution. Other embodiments can utilize photoresists 218 defining other patterns, which in turn produce different configurations of trenches in later steps. In an exemplary embodiment, the photoresist 218 is formed by spinning on a photosensitive material, exposing the photosensitive material to light through a mask containing the desired pattern, and then developing the material into the photoresist 218. Next, the first hard mask 214 can be etched through the gaps in the photoresist 218. After the photolithography and etching of the first hard mask 214 has been carried out, the photoresist 218 can be stripped, or the photoresist can be removed during the etching of the first hard mask 214, thus producing the partially formed semiconductor device shown in **Figure 2**.

[0027] In **Figure 2**, a first hard mask 214 has been etched with a pattern of alternating lines and gaps. As noted above, in some embodiments, the first set of trenches can be etched into the substrate through the first hard mask 214. However, in the embodiment illustrated in **Figures 2-3**, the relatively thinner second hard mask 213 is etched through the thicker first hard mask 214, and the first hard mask 214 is then removed. This process produces the partially formed semiconductor device shown in **Figure 3**, in which the second hard mask 213 has been patterned.

[0028] With reference to **Figure 4**, the pattern of the second hard mask 213 has been transferred (e.g., via selective wet etch) to the placeholder material 212. An upper

sidewall spacer 217 can be formed along the sidewalls of the placeholder material 212 and the second hard mask 213. The upper sidewall spacer 217 can be formed by conformally depositing a uniformly thick silicon oxide, such as the same material in the second hard mask 213, over upper and sidewall surfaces, and then directionally etching the deposited oxide such that horizontal surfaces are preferentially removed but the upper sidewall spacer 217 remains in the desired locations. In some embodiments, the upper sidewall spacers 217 have a thickness of approximately $\frac{1}{4} F$, which can provide a gap between the upper sidewall spacers 217 of approximately $\frac{1}{2} F$. Such configurations can advantageously provide two uniform sets of trenches with approximately equal widths and separated by approximately equal distances, as will be described hereinbelow.

[0029] With reference to **Figure 5**, a first set of trenches 300 has been etched into the substrate 110 through the second hard mask 213 and the upper sidewall spacers 217. The etching process can be a selective etching process that preferentially etches the material to be removed for the trench, such as silicon, without etching the material of the second hard mask 213 and spacers 217, such as TEOS or other silicon oxide-based material. The skilled artisan will appreciate that other hard mask materials and other selective etch chemistries can be employed, such as when damascene trenches are being formed in an interlevel dielectric (“ILD”). Hence, **Figure 5** shows the second hard mask 213 still in place after the formation of the first set of trenches 300. Nonetheless, the skilled artisan will recognize that the selective etching may be imperfect, thus eliminating all or a portion of the second hard mask 213 in the process of etching the first set of trenches 300.

[0030] In some embodiments, the trenches of the first set 300 are separated by a series of inter-trench regions 301, in which a second set of trenches can later be formed. In some embodiments, the width of the inter-trench regions 301 may be approximately equal to $1.5 F$. Thus, in the embodiment illustrated in **Figure 5**, after the trenches of the first set 300 have been formed, the trenches have a width approximately equal to $\frac{1}{2} F$, the upper sidewall spacers 217 have a width approximately equal to $\frac{1}{4} F$, and the inter-trench regions 301, which include the upper sidewall spacers 217, have a width approximately equal to $1.5 F$.

[0031] The trenches of the first set 300 have a depth “ D_1 ” defined by the distance from the top of the substrate 110 in the inter-trench regions 301 to the bottom silicon of the

trenches 300 immediately after the step of etching the first set of trenches 300. In some embodiments, D_1 is between about 2000 Å and 3000 Å, more particularly 2000 Å to 2500 Å.

[0032] The trenches of the first set 300 also have an aspect ratio defined by the ratio between a depth “ D_2 ” of the trenches (in this case including the masking layers) and a width of the trenches at the top of the trenches. The depth D_2 is defined as the distance from the top surface in the inter-trench regions 301 to the bottom of the trenches 300 immediately after the step of etching the first set of trenches 300. For reasons explained hereinabove, immediately after the step of etching the first set of trenches, the top surface of the inter-trench regions 301 may be at the top of the second hard mask 213 (as shown in Figure 5) or at the top of the placeholder material 212. In some embodiments, the aspect ratio is between about 5:1 and 100:1, more particularly between about 10:1 and 25:1.

[0033] Following the formation of the first set of trenches 300, the trenches can be filled. In some embodiments, the trenches 300 may be lined with one or more liner layers. For example, in the embodiment illustrated in Figure 6, a thin oxide layer 220 is grown in the trenches as well as the surface of the inter-trench regions 301 with a thickness of between about 20 Å to 70 Å. The oxide layer 220 advantageously repairs etch damage to the walls of the trenches 300. Figure 6 also shows a nitride layer 221 with a thickness between about 30 Å to 100 Å that has been deposited above the oxide layer 220 as a barrier layer to facilitate later oxide densification. A TEOS layer 223 of thickness between about 100 Å to 300 Å may optionally be formed above the nitride layer 221, providing a diffusion path for more even distribution of oxidant during SOD densification. The trenches 300 are then filled with a filler material 225, such as an electrically isolating material. In an exemplary embodiment, filler material 225 comprises a spin-on dielectric. As shown in Figure 6, the filling step may include overfilling the trenches 300, such that the filler material 225 extends above the top of the trenches 300.

[0034] Figure 7 illustrates a cross-sectional view of the partially formed semiconductor device of Figure 6 after the surface has been planarized. The planarizing process may comprise a chemical mechanical polishing process. As shown in Figure 7, the planarizing step may stop on the placeholder material 212, such that after the planarizing

step, the surface of the partially formed device comprises the filler material 225 in the trenches 300 and the exposed placeholder material 212 in the inter-trench regions 301.

[0035] Next, the upper sidewall spacers 217 can be removed (if they have not already been removed during the earlier processes), and the placeholder material 212 can be selectively etched from the inter-trench regions 301, thus producing a partially formed device in which the filler material 225 in the trenches 300 protrudes above the surface of the inter-trench regions 301. In some embodiments, TMAH can be used in an isotropic wet etch to selectively remove the placeholder material 212 from the inter-trench regions 301. A second spacer material 230, such as TEOS, may then be blanket deposited to conform to the surface of the device, as shown in Figure 8.

[0036] The spacer material 230 can then be preferentially etched from horizontal surfaces using a directional spacer etch. The directional spacer etch leaves in place second spacer material 230 in the form of sidewall spacers on approximately vertical surfaces, such as the sidewalls of the portions of the filler material above the trenches 300, protruding above the surface of the inter-trench regions 301. These remaining portions of the second spacer material 230 can then be used to align a second set of trenches 302 within the inter-trench regions 301, spaced by the spacers from the first trenches 300. In some embodiments, following the preferential etch of the second spacer material 230, the spacer material can have a thickness approximately equal to $\frac{1}{2} F$. Such embodiments can provide approximately uniform widths of the first and second sets of trenches as well as approximately uniform spacing or gaps between the first and second sets of trenches.

[0037] Figure 9 shows a cross-sectional view of the partially formed semiconductor device after the second set of trenches 302 has been etched into the substrate 110. Figure 8 shows an embodiment in which the first trenches 300 are deeper than the second trenches 302, but other configurations are possible: the second set could be deeper than the first set, or the first set and the second set could be approximately the same depth. As noted above, embodiments can provide a technique for pitch doubling, wherein a trench of the first set 300 is spaced less than a distance F (e.g., approximately $\frac{1}{2} F$) from a trench of the second set 302.

[0038] **Figure 10** shows the partially formed semiconductor device after the second trenches **302** have been filled. The second trenches **302** can be lined with an oxide liner **310**, such as an oxide that is grown to a thickness between about 30 Å and 150 Å. As shown in **Figure 10**, the trenches **302** may then be overfilled with a second filler material **312**, such as with a high density plasma (“HDP”) oxide that extends above the top of the trenches **302**. Note that while the illustrated trenches **300**, **302** have been filled in the illustrated embodiment by different techniques and embodiments, both sets of trenches are filled by forms of silicon oxide that chemically similar from the point of view of selective etching.

[0039] Following the filling of the trenches **302**, the partially formed device may then be planarized. The planarization may be carried out using a chemical mechanical polishing (“CMP”) process, and it may stop on the etch stop **211**. It is typically difficult to control the planarization process with sufficient precision to stop at the top surface of the thin etch stop **211**, such that a majority of the illustrated thin etch stop **211** thickness is consumed at the end of the CMP process. Typically between about 10 Å and 100 Å of the etch stop **211** is consumed in stopping the CMP process, which can represent between about 50% and 80% of the etch stop **211** thickness. A cross-sectional view of a partially formed device after this planarization step has been carried out is illustrated in **Figure 11**.

[0040] In some embodiments, the surface of the device after the planarization step may primarily comprise an etch stop **211** and structural material, such as silicon oxide. The structural material can then be selectively recessed to approximately coplanar with the lower surface of the etch stop, for example by selectively etching the oxide against the nitride of the etch stop.

[0041] **Figure 12** illustrates a detail of a device’s surface after structural materials have been selectively recessed. The amount that structural (illustrated as oxide) materials are recessed is preferably about equal to the thickness of the remaining etch stop **211**. In the illustrated embodiment, the structural materials are recessed by between about 10 Å and 70 Å, more particularly between 30 Å and 50 Å. Thus, the recessed structural materials leave an upper surface approximately (e.g., within ± 20 Å, more particularly within ± 10 Å) coplanar with the lower surface of the etch stop **211**. As shown in **Figure 12**, other portions of the

device, such as nitride liner layer 221, may protrude above the selectively recessed portion along with the etch stop 211.

[0042] Next, the etch stop 211 can be removed, for example by selectively etching nitride. Such an etching step may also remove other portions that protrude above the surface of the structural material, such as the nitride liner layer 221. The inventors have observed that such a process enhances the planarity of the device's surface. **Figure 13** illustrates a detail of a semiconductor device after these steps.

[0043] **Figures 11 and 14** illustrate parallel trenches filled with isolation material, made in accordance with the methods described herein. In one embodiment, the deeper trenches 300 represent shallow trench isolation between transistors in an array (e.g., a memory array such as DRAM). These deeper trenches alternate with parallel shallow trenches 302. As will be understood from the process flow of U.S. patent application No. 2006-0046407, published March 2, 2006, the disclosure of which is incorporated by reference herein, these shallow trenches 302 can represent the gap between source and drain pillars in a U-shaped protruding transistor structure, and can remain filled with insulating material or can be replaced with gate dielectric and gate electrode materials for a "3-sided" channel structure. As described in the incorporated '407 publication, subsequent crossing trenches of an intermediate depth can provide gaps between rows of transistors in which gate electrode material can be formed to surround the U-shaped semiconductor structures at least on two sides. In other embodiments, the trenches can be employed for deep DRAM capacitors; can all be for trench isolation, and may be of approximately equal depth; can be damascene trenches in insulating material for later filling with metal lines; etc.

[0044] Although not illustrated in the figures, a sacrificial oxide layer with a thickness of between about 100 Å and 200 Å may then be grown and subsequently stripped in order to remove and/or repair any damaged silicon at the upper surface.

[0045] Methods have been described that provide several advantages for the formation of semiconductor structures. For example, methods have been taught for using a placeholder material as part of the formation of self-aligned trenches in substrates. Self-aligned trenches can be used as part of pitch doubling techniques, which promote device integration. For example, in the illustrated embodiment, the pitch of the partially formed

device was $2F$ at the stage shown in **Figures 1-7**, whereas the pitch is F at the stage shown in **Figure 13**; the feature size shrinks from F at the stage of **Figure 1** to $\frac{1}{2}F$ at the stage of **Figure 13**. Fabrication techniques described herein advantageously enable more precise etching, such as by using a relatively thin second hard mask to improve the aspect ratio during etching of the trenches. Further, methods disclosed herein promote planarity at the surface of the semiconductor structure, such as by providing a relatively thin etch stop, and a sequence of recessing surrounding materials by an amount about equal the amount of etch stop remaining after consumption during a CMP step.

[0046] In accordance with one embodiment, a method is provided for forming a device. The method comprises forming a layer of polysilicon on a substrate and forming a first set of trenches in the substrate, wherein remaining portions of the polysilicon layer remain above the substrate in inter-trench regions between trenches of the first set. The method further comprises filling the first set of trenches with a filler material, wherein the filler material extends upward to at least a level adjacent the remaining portions of the polysilicon layer. Further, the method comprises selectively etching the remaining portions of the polysilicon layer from the inter-trench regions, forming spacers on sidewalls of the filler material in the inter-trench regions, and etching a second set of trenches into the substrate between the spacers.

[0047] In another embodiment, a method is provided for forming a device on a substrate. The method comprises forming an etch stop layer on the substrate and etching a plurality of first trenches through the etch stop layer and the substrate. The method further comprises filling the first trenches with an isolation material that protrudes above the substrate, forming spacers on sidewalls of the protruding portion of the isolation material, and etching a plurality of second trenches between the spacers. The method further comprises filling the second trenches with a second filler material, planarizing the second filler material and stopping planarizing on the etch stop layer.

[0048] In another embodiment, a method is provided of forming an integrated circuit. The method comprises forming a structure on a substrate, the structure comprising a structural material and an etch stop, the etch stop having an upper surface and a lower surface. The method further comprises planarizing the structure and stopping planarizing on

the etch stop. The method further comprises selectively recessing the structural material to be approximately coplanar with the lower surface of the etch stop, and selectively removing the etch stop.

[0049] It will be appreciated by those skilled in the art that various other omissions, additions and modifications may be made to the methods and structures described above without departing from the scope of the invention. For example, while the illustrated embodiments involve etching alternating “shallow” trench isolation (“STI”) and in a semiconductor material and filling with electrically insulating isolation materials, the skilled artisan will appreciate applications of the principles and advantages taught herein for other contexts. For example, some of the methods taught herein can be applied to defining closely spaced, self-aligned damascene trenches for filling with metal lines. All such changes are intended to fall within the scope of the invention, as defined by the appended claims.

WHAT IS CLAIMED IS:

1. A method of forming a device, the method comprising:
 - forming a layer of polysilicon on a substrate;
 - forming a first set of trenches in the substrate, wherein remaining portions of the polysilicon layer remain above the substrate in inter-trench regions between trenches of the first set;
 - filling the first set of trenches with a filler material, wherein the filler material extends upward to at least a level adjacent the remaining portions of the polysilicon layer;
 - selectively etching the remaining portions of the polysilicon layer from the inter-trench regions;
 - forming spacers on sidewalls of the filler material in the inter-trench regions;
 - and
 - etching a second set of trenches into the substrate between the spacers.
2. The method of Claim 1, further comprising, after filling, planarizing the filler material on the substrate to expose the remaining portions of the polysilicon layer in the inter-trench region prior to selectively etching the remaining portions of the polysilicon layer.
3. The method of Claim 1, wherein forming a layer of polysilicon comprises forming a layer of polysilicon with a thickness between about 500 Å and 3000 Å.
4. The method of Claim 1, wherein etching the second set of trenches comprises etching a second set of trenches that is substantially parallel to the first set of trenches.
5. The method of Claim 4, wherein etching the second set of trenches comprises separating trenches of the first set of trenches from trenches of the second set of trenches by a width less than F, wherein F is a minimum feature size formable using a photolithographic technique.
6. The method of Claim 5, wherein after etching the second set of trenches, the trenches of the first and second sets of trenches are approximately uniformly spaced and have approximately uniform widths.
7. The method of Claim 5, wherein the trenches of the first set have a depth greater than a depth of the second set.

8. The method of Claim 1, wherein forming a first set of trenches comprises etching the first set of trenches through a hard mask layer over the layer of polysilicon.

9. The method of Claim 8, wherein the hard mask layer comprises tetraethylorthosilicate ("TEOS").

10. The method of Claim 8, further comprising, before etching the first set of trenches, forming spacers on at least a portion of sidewalls of the hard mask layer.

11. The method of Claim 8, wherein the first set of trenches has a depth from a top surface of the inter-trench regions to the bottom of the first set of trenches of between about 2000 Å and 2500 Å immediately after the step of forming the first set of trenches.

12. The method of Claim 8, wherein the first set of trenches has an aspect ratio of between about 5:1 and 100:1, wherein the aspect ratio is the ratio between a depth of the first set of trench and a width of trenches of the first set, wherein depth is calculated from the top surface of the inter-trench regions to the bottom of the first set of trenches.

13. The method of Claim 8, further comprising using a carbon hard mask to pattern the hard mask layer and removing the carbon hard mask before etching the first set of trenches.

14. The method of Claim 13, wherein the carbon hard mask has a thickness between about 1800 Å and 2200 Å.

15. The method of Claim 14, wherein the hard mask layer has a thickness between about 500 Å and 1500 Å.

16. The method of Claim 1, further comprising forming an etch stop layer beneath the layer of polysilicon and, after etching the second set of trenches, filling the second set of trenches with a second filler material and planarizing the second filler material, wherein planarizing the second filler material comprises stopping on the etch stop layer.

17. A method of forming a device on a substrate, comprising:

forming an etch stop layer on the substrate;

etching a plurality of first trenches through the etch stop layer and the substrate;

filling the first trenches with an isolation material that protrudes above the substrate;

forming spacers on sidewalls of the protruding portion of the isolation material;

etching a plurality of second trenches between the spacers;

filling the second trenches with a second filler material; and

planarizing the second filler material and stopping planarizing on the etch stop layer.

18. The method of Claim 17, wherein forming an etch stop comprises forming the etch stop with a thickness between about 20 Å and 150 Å.

19. The method of Claim 17, wherein planarizing comprises chemical mechanical planarization.

20. The method of Claim 17, wherein forming an etch stop comprises forming the etch stop of silicon nitride.

21. The method of Claim 17, wherein forming an etch stop comprises forming the etch stop of aluminum oxide..

22. The method of Claim 17, wherein filling the first trenches with an isolation material that protrudes above the substrate comprises:

overfilling the trenches with an isolation material;

planarizing the isolation material to expose placeholder material underlying the isolation material between sidewalls of the first trenches;

selectively etching the placeholder material between sidewalls of the first trenches.

23. The method of Claim 22, wherein overfilling the trenches with an isolation material comprises overfilling the trenches with a spin-on dielectric.

24. The method of Claim 22, wherein filling each of the first trenches further comprises lining the trenches with at least one liner layer.

25. The method of Claim 17, wherein etching a plurality of second trenches comprises spacing the second trenches apart from the first trenches by a width less than F, wherein F is a minimum feature size formable using a photolithographic technique.

26. The method of Claim 17, wherein etching a plurality of second trenches comprises etching the second trenches to a depth less than a depth of the first trenches.