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PATENT SPECIFICATION

DRAWINGS ATTACHED

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COMPLETE SPECIFICATION

Junction Transistors and Method of Fabricating same

We, TEXAS INSTRUMENTS INCORPORATED, of 6000, Lemmon Avenue, Dallas, Texas, United States of America, a corporation organized and existing under the laws of the State of Delaware, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The present invention relates to junction transistors and a method of fabricating same by judiciously combining diffusion and alloying techniques.

In recent years, considerable advances have been made in the fabrication of transistors and particularly in the production of transistors having thin bases whereby improved frequency and current handling characteristics result. The more common techniques developed for the production of thin-base, junction transistors involve forming p-n junctions using alloy, grown, grown diffused or vapor diffused processes. The production of transistors having thin bases, using a diffusion technique, continues to present problems, notable among which are the difficulties of connecting external leads to the thin base and emitter layers. The magnitude of this problem becomes immediately evident when it is realized that the thickness of the base and emitter layers produced by conventional diffusion techniques are in many instances a fraction of a mil thick. For example, the base layer is in the order of .05 mils to .1 mils and the emitter is in the order of .1 to .2 mils thick. In consequence, great care must be exercised in attaching contacts and leads to these thin layers to prevent the lead or contact material from completely penetrating a specific layer and passing into the immediately adjacent layer. In the case of an emitter contact, this would result in shorting of the emitter to the collector.

A broad object of the present invention is to produce a thin-base, junction transistor having all of the advantages of the diffused base transistor but which provides relatively thick emitter and base regions for facilitating attaching external leads. For convenience the invention shall be described with respect to PNP and NPN transistors but it is to be understood that the invention is applicable to NPIN, PNIP, PNPN and NPNP configurations wherein three of the zones are formed in accordance with the present invention and the fourth zone is provided by known techniques, such as alloying an additional body to a wafer.

The present invention is a method of fabricating a junction transistor comprising first diffusing an impurity material of one conductivity producing type into one surface of a wafer of semiconductive material containing an impurity material of an opposite conductivity producing type, the wafer being of said opposite conductivity type, the surface becoming said one conductivity type, and then alloying a body containing an impurity material of said opposite conductivity producing type with a region of the wafer in said surface to form a melt, said melt containing impurity material of said one conductivity producing type having a higher diffusion coefficient than said impurity material of opposite conductivity producing type, maintaining said wafer at a sufficiently high temperature for a sufficient time to diffuse impurity material of said one conductivity producing type into the region of said wafer immediately surrounding the melt, and allowing the melt to cool and solidify whereby an emitter and base zone of said opposite conductivity type and said one conductivity type, respectively, are simultaneously formed.

The semiconductive material may be germanium or silicon, and the body may contain

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only an impurity material of said opposite conductivity producing type.

The present invention is also a method of fabricating a junction transistor comprising placing a dot of semiconductive material of one conductivity upon a wafer of the same conductivity type, heating the combined unit so that the dot forms a melt with a portion of the wafer, the heating being done in an atmosphere of impurity material of the opposite conductivity producing type until the latter material passes through the dot and diffuses into the surface of the wafer to form a layer of opposite conductivity material, solidifying the melt whereby an emitter and base zone of said opposite conductivity type and said one conductivity type, respectively, are simultaneously formed, and attaching leads to the dot, the layer and the wafer.

The present invention is also a transistor comprising a collector constituted by a wafer of semiconductive material of one conductivity type, a diffused layer formed on said wafer adjacent one surface thereof of opposite conductivity type, an emitter constituted by a body containing an impurity of said one conductivity producing type extending through said diffused layer into the region of said wafer of said one conductivity type and alloyed therewith, and a diffused base layer of opposite conductivity type surrounding the portion of the body in said wafer and contacting said first-mentioned diffused layer, and thin with respect to the first-mentioned diffused layer.

In consequence of the arrangement defined in the immediately preceding paragraph, the original diffused layer is in contact with the relatively thin diffused layer and the latter subsists between the body and the original layer. Since the original diffused layer is relatively thick, it is a simple matter to make contact to it and a ring contact is preferably mployed to provide low base resistance. Further, by choosing the quantity of material in the original body such that the body is raised above the surface of the remainder of the transistor, a relatively thick contact may be provided and it is a simple matter to attach leads to the body to form an emitter contact.

The invention and the above noted and other features thereof will be understood more clearly and fully from the following detailed description with reference to the accompanying drawings, in which:—

Fig. 1 is a diagram illustrating a step in the method of the invention wherein an initial thick layer of base material has been formed on a semiconductor wafer and a dot has been placed on top of the base layer;

Fig. 2 is a diagram illustrating a second step in the process of the invention wherein the dot has been alloyed through the base and extends into the wafer;

Fig. 3 is a diagram illustrating a step in the present invention wherein diffusion of the base layer has been completed;

Fig. 4 is an illustration of a complete transistor with electrodes connected to the various regions of the transistor body;

Fig. 5 is a modified counterpart of Fig. 2 in which another embodiment of the method of this invention is disclosed;

Fig. 6 shows another step in the method described in connection with Fig. 5;

Fig. 7 is a cross sectional illustration of the complete transistor formed by the method of Figs. 5 and 6;

Fig. 8 is a modified counterpart of Fig. 1 in which an additional embodiment of the method of this invention is disclosed;

Figs. 9 and 10 illustrates progressive steps in forming a transistor by the method of the embodiment commenced in Fig. 8 and completed in Fig. 11; and

Fig. 11 represents a cross-sectional view of the complete transistor formed by the method of Figs. 8—10.

Referring specifically to Fig. 1 of the drawings, a wafer 1 of a suitable semiconductive material containing a conductivity effecting impurity has on the upper region thereof a relatively thick base contact layer 2 which is formed by diffusion of a suitable impurity material of an opposite conductivity producing type to that possessed by the wafer into the upper surface of the body. A dot of alloying material 3 is placed on the upper surface of the relatively thick base contact layer material 2 preparatory to heat treating the body.

The specific materials employed for the regions 1, 2 and 3 depends primarily upon the material of the wafer 1. If the wafer 1 is of germanium, it is preferable to form a NP transistor and therefore, the wafer is initially doped with a suitable acceptor material such as gallium to convert the semiconductive layer 1 to a P-type material. The base contact layer 2 must then exhibit N-type properties and, therefore, the material diffused into the wafer 1 to produce the layer 2 must be a suitable donor material, for instance, antimony. The dot 3, from which the emitter electrode is to be fabricated, must exhibit acceptor properties, and therefore is primarily constituted of a suitable acceptor material such as indium. However, in order to produce a diffused layer of N-type material about the dot 3, after the fabrication of the semiconductor body is completed, the dot 3 must also contain a suitable donor material unless the concentration of N-type conductivity producing material in the diffused layer 2 is sufficiently high to make this unnecessary. In a specific example, the dot contains 3% antimony by weight as the N-type impurity material and 97% by weight indium as the P-type impurity material.

If a NPN junction transistor is to be fabri-

cated, the wafer 1 is formed preferably from silicon which has been doped with antimony or arsenic, for example, to exhibit N-type conductive properties. The base contact layer 2 is then formed by diffusing a suitable acceptor material into the upper surface of the wafer so that the layer 2 exhibits P-type conductive properties. In a specific example, the layer 2 may be formed by diffusing boron into the wafer 1. The dot 3, in this case, includes only N-type impurity material since in this particular embodiment of the invention, the quantity of boron obtained by alloying the layer 2 with the dot 3 is sufficient to form an effective base junction layer upon a subsequent diffusion step. In a specific example, the dot 3 may comprise 97% tin by weight and 3% by weight arsenic.

Regardless of which semiconductor material is selected, the specific impurity materials chosen for use in the dot 3 and in forming the layer 2 are essentially determined by their various properties and especially by their coefficients of diffusion. The size of the dot 3 is determined primarily by the final desired characeristics of the transistor. For example, if it is desired to produce a high frequency transistor, the diameter of the dot should not exceed about ten mils whereas if the transistor is to be employed primarily for power applications the dot diameter would preferably be about 40 or 50 mils.

Referring to Figure 2 of the accompanying drawing, after the dot 3 has been placed on the layer 2, the body is heated in an evacuated chamber to a suitable alloying temperature of the dot 3 and the wafer 1. The precise alloying temperature required depends almost entirely upon the materials being used. In practically all cases, the alloying temperature for germanium is less than 700° C. and preferably less than 500° C. As a result, the portions of the layer 2 and wafer 1 subsisting substantially immediately under the dot become alloyed therewith. When silicon is used as the semiconductor material, the maximum temperature does not exceed 1200° C. As can be seen from the drawing of Fig. 2, the base contact layer 2, under the dot 3, is destroyed during the alloying process, and the material of the layer 2 and part of the material of the wafer 1 are mixed with the now liquefied dot which, it will be recalled, originally contained both N- and P-type impurity materials. In the case of the production of a PNP transistor, the P-type impurity material in the subsequently solidified mass 6 (Fig. 3) is predominant but the N-type impurity material has a higher diffusion rate. On the other hand, when an NPN transistor is being made, N-type impurity material predominates in the solidified mass 6 and P-type impurity material has a higher diffusion rate.

After the liquefication of the button 3, the temperature of treatment is elevated to a suitable high value and maintained substantially constant for a predetermiend length of time as determined by the materials, the diffusion constants, and the desired depth of penetration of the base layer 5 into the wafer 1. The elevated temperature required for diffusion is less in the case of germanium than in the case of silicon. For the former, temperatures above 600° C. are necessary, whereas temperatures above 900° C. are required for silicon. Thereafter, the temperature is reduced to that required to solidify the molten mass 4 and produce the body as illustrated in Fig. 3 of the accompanying drawings. It will be noted that the base contact layer 2 is in contact with a thin diffused layer 5 containing the same conductivity producing impurity material as the base 2 and that the layer 5 completely surrounds the emitter body 6 to the upper limit of the main body of the transistor. The transistor thus formed has a relatively thick base contact layer 2 which is readily available for connecting leads thereto while there is produced an emitter 6 which is quite thick and to which a lead may also be attached without fear of completely penetrating the emitter region. Collector, base, and emitter leads 7, 8 and 9, respectively, are illustrated in Fig. 4 attached to the respective contacts wafer 1, ring 10, and emitter 6 of the device. Fig. 4 thus shows the completed transistor.

The times and temperatures required for effecting the desired treatment, in accordance with the present invention, are determined by a number of factors. Basically, of course, these factors are determined by the materials involved, each of which has a known diffusion coefficient and surface solubility at a particular temperature. With these factors having been previously determined and their values readily available to all, time of treatment required at a particular temperature is essentially determined by the equation:—

$$C_x = \frac{Q}{\sqrt{\pi Dt}} e^{-x^2/4Dt}$$

where C_x is the concentration of diffusant at depth x per centimenters cubed, Q is the initial surface density of the atoms diffusant, D is the diffusion coefficient at the temperature of operation and t is the time in seconds.

As an example of material and times and temperature of the treatment, it is assumed initially that a PNP transistor is to be fabricated employing a wafer of germanium which is suitably doped with a suitable acceptor material such as gallium. Antimony is diffused into one surface of a germanium base wafer 1 by well-known techniques to form a diffused layer 2 about 0.5 mils thick. Thereafter, a dot 15 mils in diameter and 7 mils thick of 97% by weight indium and 3% by weight antimony is placed on the layer 2

of the wafer and the whole is heated in a hydrogen atmosphere to alloying temperature of 760° C. for 10 minutes to form a melt, and thereafter the temperature is maintained at about 750° C. and held for about three hours. During this period, the antimony in the melt diffuses into the solid portion of the wafer completely around the molten area so that upon cooling, a diffused base layer is formed. As previously indicated, if the concentration of the impurity material in the diffused layer 2, namely, N-type conductivity producing antimony in this specific example, is sufficiently high, the alloy dot 3 need not contain any N-type conductivity producing impurity. That is, the alloy dot may be 100% indium, and the N-type material is supplied from the diffused layer 2. The use of other materials will affect the temperature or the time factor when utilizing the method of this invention. For example, if 3% arsenic is used in place of the 3% antimony in the above example, the time factor would decrease approximately 20%; and if 3% phosphorous were used, the time would be increased to approximately 9 hours. If it is desired to maintain a constant time, such as 3 hours, and vary the temperature, the phosphorous combination would be heated at approximately 800° C. whereas the arsenic would require approximately 700° C. So it will be apparent that the optimum relationship between temperature and time must be determined fro each new material that is utilized, which in general will be from Group III of the periodic table for acceptors (P-impurities) and Group V for donors (N-impurities) to be combined with the basic material from Group IV, intermetallics, or other sources.

As an example of the fabrication of an NPN transistor, consider a wafer of silicon suitably doped with a donor material such as antimony and which has diffused into the upper surface thereof a quantity of boron to form the layer 2 about 0.5 mils thick. Thereafter, a dot 15 mils in diameter and 7 mils thick of 97% by weight tin and 3% by weight arsenic is placed on the upper surface of the wafer 2 and the assembly is heated in an evacuated atmosphere to alloying temperature at 1260° C. for 5 minutes to form a melt and thereafter the temperature is maintained at about 1250° C. for forty-five minutes. As previously indicated, if the concentration of the impurity material in the diffused layer 2, namely, P-type conductivity producing boron in this specific example, is sufficiently high, the alloy dot 3 need not contain any P-type conductivity producing impurity.

Reference is now made to Figs. 5—7 which disclose a modification of the present invention. Fig. 5 is the counterpart of Fig. 2, but according to this modification a dot of alloying material 14 is heated until it extends not only through a diffused layer12, but also entirely through a semiconductor wafer 11. Diffused layer 12 is of a conductivity type opposite the conductivity type of the wafer 11 as was described previously. Also the original composition of the alloying material 14 is primarily characteristic of the same conductivity type as the wafer 11 or entirely characteristic of the conductivity type of the wafer 11, if the concentration of the diffused layer 12 is sufficiently high. This feature was also described in detail with respect to Figs. 1—4.

Fig. 6 discloses the next step in the operation in which base layers 15 containing the same conductivity producing impurity material as the base 12 and substantially surrounding an emitter body 16 have been diffused. The transistor thus formed has a relatively thick base contact layer 12 which is readily available for connecting leads thereto, such as the ring contact lead 18 attached to an integral with ring 20. Also, an emitter 16 is produced which is quite thick and to which a lead may also be attached without fear of completely penetrating the emitter region. Such a lead to the emitter is shown at 19. A lead to a ring collector 20a is shown at 17. The transistor produced according to the steps shown in Figs. 5—7 are particularly valuable in high frequency applications. The transistor thus produced is very convenient for use with coaxial transistor structures. That is, the symmetrical device thus produced is symmetrical about the center which constitutes the emitter. As shown, both a ring base and a ring collector contact is used and two leads 19 are shown going to the emitter 16. Thus, as seen in Fig. 7, two separate wires can go to the emitter 16 and base 15, respectively, and two other wires can go to the emitter 16 and collector 17, respectively. The leads may be enclosed in cables in individual outer sheaths or a single common outer sheath, with an input cable containing the emitter and base leads and an output cable containing the collector and emitter leads.

As a specific example of the semiconductor device formed by the modification shown in Figs. 5—7, the manufacture of an NPN junction transistor will be described. A wafer of silicon is suitably doped with a donor material, such as antimony, and has diffused into the upper surface thereof a quantity of boron to form the layer 12 about 0.5 mils thick. Thereafter, a dot 20 mils in diameter and 10 mils thick of 97% by weight tin and 3% by weight arsenic is placed on the upper surface of the wafer 12 and the assembly is heated in an evacuated atmosphere to alloying temperature at 1260° C. for a duration sufficient to form a melt which extends entirely through the semiconductor wafer 12. Thereafter, the temperature is

maintained at about 1250 °C. for 45 minutes. At the end of 45 minutes, the device is cooled and a P-layer is formed substantially surrounding an emitter region formed by the solidified melt. As shown in Fig. 7, two leads 19 are attached to the emitter region 16 on the top and on the bottom of the transistor and leads 17 and 18 are attached to ring contacts on the collector and base regions, respectively, to form the completed transistor of the NPN type.

Referring now to Figs. 8—11, a third embodiment of the method of this invention will be described. A donor-containing semiconductor alloy dot 23 of N-characteristics is placed upon a larger wafer 21 of N characteristics, and the combined unit of Fig. 8 is then placed in a furnace filled with a gas of acceptor material, such as gallium vapor, or an inert gas such as helium containing a mixture of gallium vapor. When the dot 23 has been sufficiently heated it changes to a liquid state 24 as shown in Fig. 9. The assembly is not held at the alloying temperature for any longer than necessary, but the temperature is maintained high enough in this acceptor atmosphere for the dot to permit the acceptor material to pass through and form a P-type diffused layer 25 between the dot now 26 and the wafer 21 as shown in Fig. 10. The balance of the exposed area of the wafer is also covered by the diffused layer, and must be cut off where not necessary. By connecting suitable leads 27 to the wafer 21, 28 to the base layer 25, and 29 to the emitter region 26, an NPN transistor will be formed as shown in Fig. 11 In utilizing this method, a close control of the temperature is required so that the alloy dot will not be dispersed while the acceptor material is diffusing therethrough; and of course it will be essential that the acceptor material have a faster diffusing rate than the donor material.

Although the specific examples given suggest forming a PNP transistor from germanium and an NPN transistor from silicon, it will be appreciated that the invention is not limited thereby but includes forming PNP and NPN devices from silicon, germanium, or any other suitable semiconductor material. Generally, the donor impurities diffuse more rapidly in germanium than the acceptor impurities, while in silicon the acceptor impurities usually diffuse more rapidly than the donor impurities. As the material which diffuses the most rapidly must be employed to form the base layer of the device, and since most donors diffuse more rapidly in germanium, a PNP transistor is more easily formed using germanium. The converse holds true for silicon and an NPN transistor is more easily formed.

In addition to the definite advantage achieved relating primarily to the ease in making contact with the base and emitter of the transistor, another advantage arises from the fact that there is no base-to-emitter or a base-to-collector contact overlap to cause hysteresis losses at high currents or to add high frequency capacities.

Although the invention has been described and illustrated with reference to specific embodiments, it will be clear that variations of the details thereof may be resorted to without departing from the scope of the invention as defined in the appended claims.

WHAT WE CLAIM IS:—

1. A method of fabricating a junction transistor comprising first diffusing an impurity material of one conductivity producing type into one surface of a wafer of semiconductive material containing an impurity material of an opposite conductivity producing type, the wafer being of said opposite conductivity type, the surface becoming said one conductivity type, and then alloying a body containing an impurity material of said opposite conductivity producing type with a region of the wafer in said surface to form a melt, said melt containing impurity material of said one conductivity producing type having a higher diffusion coefficient than said impurity material of opposite conductivity producing type, maintaining said wafer at a sufficiently high temperature for a sufficient time to diffuse impurity material of said one conductivity producing type into the region of said wafer immediately surrounding the melt and allowing the melt to cool and solidify whereby an emitter and base zone of said opposite conductivity types and said one conductivity type, respectively, are simultaneously formed.

2. The method of Claim 1 wherein said semiconductive material is germanium.

3. The method of Claim 1 wherein said semiconductive material is silicon.

4. A method according to any of Claims 1 to 3, wherein the body contains no impurity material of said one conductivity producing type.

5. A method of fabricating a junction transistor comprising first diffusing an impurity material of one conductivity producing type into the surface of a wafer of semiconductive material containing an impurity material of an opposite conductivity producing type, the wafer being of said opposite conductivity type, the surface becoming said one conductivity type, and then alloying a body containing impurities of both conductivity producing types into said surface to form a melt therewith, the impurity material of said one conductivity producing type having a higher diffusion coefficient than the impurity material of said opposite conductivity producing type, maintaining said wafer at a sufficiently high temperature for a sufficient time to cause impurity material of said one conductivity producing type to diffuse into the region of said

wafer immediately surrounding the melt, and solidifying the melt whereby an emitter and base zone of said opposite conductivity type and said one conductivity type, respectively, are simultaneously formed.

6. The method of Claim 5, wherein said semiconductive material is germanium.

7. The method of Claim 5, wherein said semiconductive material is silicon.

8. A method according to Claim 5, wherein the one conductivity producing type impurity is a donor impurity material and the opposite conductivity producing type impurity is an acceptor material in the body having a lower diffusion coefficient than the donor material.

9. A method according to Claim 8, wherein the one conductivity producing type impurity is antimony, the body is comprised of 97% by weight indium and 3% by weight antimony and the wafer is maintained in an evacuated region and at a temperature of approximately 750° C. for approximately three hours to cause the antimony contained in said melt to diffuse into said wafer in the region immediately surrounding the melt.

10. A method according to Claim 1, wherein the one conductivity producing type impurity is boron, the body is comprised of 97% by weight tin and 3% by weight arsenic, and the wafer is a silicon wafer and is maintained in an evacuated region and at a temperature of approximately 1250° C. for approximately 45 minutes to cause boron contained in said melt to diffuse into the region of said wafer immediately surrounding the melt.

11. A transistor comprising a collector constituted by a wafer of semiconductive material of one conductivity type, a diffused layer formed on said wafer adjacent one surface thereof of an opposite conductivity type, an emitter constituted by a body containing an impurity of said one conductivity producing type extending through the diffused layer into the region of said wafer of said one conductivity type and alloyed therewith and a diffused base layer of opposite conductivity type surrounding the portion of said body in said wafer and contacting said first-mentioned diffused layer, and thin with respect to the first-mentioned diffused layer.

12. A transistor as defined in Claim 11 wherein said semiconductive material is germanium.

13. A transistor as defined in Claim 11 wherein said semiconductive material is silicon.

14. A transistor as defined in Claim 11 of the NPN type.

15. A transistor as defined in Claim 11 of the PNP type.

16. A method of fabricating a junction transistor comprising first diffusing an impurity material of one conductivity producing type into a surface of a wafer of semiconductive material containing an impurity material of an opposite conductivity producing type, said impurity material of one conductivity producing type having a higher diffusion coefficient than the impurity producing material of opposite conductivity producing type, the wafer being of said opposite conductivity type, the surface becoming said one conductivity type, and then alloying a body containing impurities of both conductivity producing types into said surface and completely through the wafer to form a melt therewith, maintaining said wafer at a sufficiently high temperature for a sufficient time to cause impurity material of said one conductivity producing type to diffuse into the region of said wafer immediately surrounding the melt, and solidifying the melt whereby an emitter and base zone of said opposite conductivity type and said one conductivity type, respectively, are simultaneously formed.

17. A method of fabricating a junction transistor comprising placing a dot of semiconductive material of one conductivity upon a wafer of the same conductivity type, heating the combined unit so that the dot forms a melt with a portion of the wafer, the heating being done in an atmosphere of impurity material of the opposite conductivity producing type until the latter material passes through the dot and diffuses into the surface of the wafer to form a layer of opposite conductivity material, solidifying the melt whereby an emitter and base zone of said opposite conductivity type and said one conductivity type, respectively are simultaneously formed, and attaching leads to the dot, the layer and the wafer.

18. The method of Claim 16, wherein the melt solidifies to form a centre member of one conductivity type material extending completely through a wafer of the opposite conductive material.

19. A method of fabricating a junction transistor substantially as hereinbefore des-

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cribed with reference to Figs. 1 to 3, or Figs. 5 and 6, or Figs. 8 to 10 of the accompanying drawings.

20. A transistor substantially as hereinbefore described with reference to Fig. 4, or Fig. 7, or Fig. 11 of the accompanying drawings.

21. A transistor fabricated in accordance with the method set out in any of Claims 1 to 10 or Claims 16 to 19.

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