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PATENT SPECIFICATION

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COMPLETE SPECIFICATION

DRAWINGS ATTACHED

Semiconductor Device and Method of Making Same

We, TEXAS INSTRUMENTS INCORPORATED, of 6000 Lemmon Avenue, Dallas, Texas, United States of America, a corporation organized and existing under the laws of the State of Delaware, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to semiconductor devices and methods of making same including semiconductor bodies containing transistors and/or circuit elements therein or thereon.

In modern day electronic packaging, the need for self-contained devices or "building blocks" which are light and occupy small volumes has become increasingly important. Thus, for example, with the advent of space vehicles, the need for exceedingly light and small electronic devices has become critical, and there has been a continuing search for methods of reducing size, weight, and power consumption of electronic devices. With the advent of the transistor and other semiconductor devices, a major breakthrough was made in the field of circuit miniaturization, and electronic equipment currently employed in air and space craft almost exclusively utilizes semiconductor devices as active operating elements.

As is well known to those familiar with the art of circuit miniaturization, various proposals hav been advanced for further minimizing the size of electronic equipment. Such proposals have included the practice of packaging techniques in which an entire electronic "building block" such as a counter, multivibrator, AND gate, OR gate, etc. is formed on a single supporting member, such as an insulating substrate. By the use of conventional methods of applying coatings to the substrate, various passive circuit elements (as hereinafter defined), such as resistors and capacitors, have been formed thereon with a minimum utilization of space.

Although circuit packaging techniques such as those to which reference is made above have obvious advantages, problems have arisen when it has been attempted to employ such techniques in the forming of semiconductor devices, such as diodes and transistors, for conventional semiconductor materials, such as germanium or silicon, do not readily lend themselves to evaporation or other methods heretofore employed for the application of passive elements (as hereinafter defined). Consequently, in circuit packages heretofore proposed, it has been conventional to form passive electrical elements upon a substrate and then to connect a separately formed transistor or other semiconductor component to the substrate by solder or conducting cement, thereby to complete the fabrication of the electronic package.

In an effort to further reduce cost and size, and to increase reliability and structural rigidity, the search has continued for a method of producing an electronic packaged assembly in which the necessity for external connection of semiconductor devices would be eliminated. To that end, it is proposed in the specification of co-pending application No. 3633/60 (Serial No. 945,734), that various circuit elements including diodes, transistors, and resistors all be formed within a single block of semiconductor material, thereby eliminating the necessity for separate fabrication of the semiconductor devices and the interconnections as mentioned above. Although the proposal constitutes a major advance in the art of circuit miniaturization,

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there may arise occasions in which the values of resistance which may be readily formed within bodies of semiconductor material lie outside the bounds of those easily obtained. In addition, since the resistivity of semiconductor material (as hereinafter defined) varies quite widely with temperature, there may arise occasions in which a need for resistor stability renders the utilization of circuits embodied in the form of the heretofore-mentioned application less attractive. Consequently, the present invention may provide in a package of minimum size electronic circuits which include not only active elements (as hereinafter defined) such as transistors or diodes but, in addition, passive elements of great electrical stability and which are electrically independent of the semiconductor material.

The term "semiconductor material" used herein is defined in "Transistors Handbook" by William D. Bevitt, *Prentice-Hall*, 1956 as — An electronic conductor with resistivity in the range between metals and insulators in which the electrical charge carrier concentration increases with increasing temperature over some temperature range — and this term is to be so construed herein.

According to the "Encyclopedic Dictionary of Electronics and Nuclear Engineering" edited by Sarbocher and published by *Prentice-Hall*, "active elements" are those which in an impedance network act as current generators, whereas "passive elements" do not so act. The terms "active elements" and "passive elements" are to be so construed herein. Furthermore, the term "passive circuit elements" as used herein and in the claims includes resistors, capacitors, diodes, inductors or the like as distinguished from highly conductive films or materials of relatively low resistance used solely for the purpose of interconnecting circuit elements.

The present invention is a device comprising a body of semiconductor material having a first region of one type conductivity and a second region of opposite type conductivity contiguous thereto to form a P-N junction, said regions extending to one and the same surface of said body, insulating material on said one surface, and at least one passive circuit formed on said insulating material..

The present invention is also a device comprising a body of semiconductor material having a first region of one type conductivity and a second region of opposite type conductivity contiguous thereto to form a P-N junction, said regions extending to one and the same surface of said body and being spaced from the opposite surface of said body, insulating material on said one surface, and at least one passive circuit element formed on said insulating material.

The present invention is also a device comprising an electrical network having at least one circuit element which includes a P-N junction and at least one passive other circuit element, a body of semiconductor material, the or each P-N junction circuit element of said electrical network being formed in said body and having regions of opposite conductivity types thereof extending to one and the same surface of said body, insulating material on said one surface, and the or each passive other circuit element of said electrical network being formed on said insulating material.

The present invention is also a method of producing a device comprising the steps of forming, in a body of semiconductor material, a first region of one type conductivity extending to one surface of said body, forming, in said body contiguous with said first region, a second region of opposite conductivity type extending to said one surface, forming insulating material on said one surface, and forming at least one passive circuit element on said insulating material.

The present invention is also a method of producing a device comprising the steps of forming, in a body of semiconductor material, a first region of one type conductivity extending to one surface of said body and spaced from the opposite surface of said body, forming, in said body contiguous with said first region, a second region of opposite conductivity type extending to said one surface and being spaced from said opposite surface, forming insulating material on said one surface, and forming at least one passive circuit element on said insulating material.

The present invention is also a method of producing a semiconductor device consisting of an electrical network having at least one circuit element which includes a P-N junction and at least one passive other circuit element, comprising the steps of forming, in a body of semiconductor material, the or each P-N junction circuit element of said electrical network with the regions thereof extending to one and the same surface of said body, forming insulating material on said one surface, and forming the or each passive other circuit element of said electrical network on said insulating material.

The present invention is also a transistor comprising a body of semiconductor material containing the emitter, base and collector regions of alternating conductivity type, the successive regions overlying one another and all extending to one and the same face of said body, insulating material on selected areas of said one face, and contact elements secured to said one face and ohmically connecting to each of said regions.

An embodiment of the invention will now be described by way of example, with reference to the accompanying drawing in which :—

Fig. 1 is a plan view of a semiconductor

device according to the invention;

Fig. 2 is an electrical schematic diagram of the circuit physically embodied in Fig. 1;

Fig. 3 is a cross-sectional view taken along the sectional lines 3-3 in Fig. 1; and

Fig. 4 is a cross-sectional view taken along the sectional lines 4-4 in Fig. 1.

Turning now to the drawing, and more particularly to Fig. 1, it will be noted that therein is shown a semiconductor device 1 which in the cross section of Figure 3 is seen to include a block or body 19 of semiconductor material. Formed within and upon block 19 is a transistor 14, which comprises a portion of block 19 together with layers 21 and 22 which are of conductivity types respectively opposite to and similar to the type of block 19. These two layers 21 and 22 form the base and emitter regions respectively of the transistor, and connections are made to collector, emitter, and base regions by terminals 11, 12 and 13, respectively, which terminals include ohmic contact elements and conductive material extending over the insulating material 20. Interconnecting films 15 and 23 of relatively low resistance serve to connect terminals 11 and 12 to external connection tabs 2 and 3; tab 4 provides an external connection to the upper conducting film 6 of capacitor C; and tab 5 provides an external connection to resistive films 9 and 10, which comprise resistors R2 and R3, respectively.

As also noted from an inspection of Figure 1, the collector terminal 11 of the transistor 14 is connected to resistor film 10, and the terminal 13 of base 21 of the transistor 14 is connected via relatively low resistance film 17 to relatively high resistance film 9 which comprises resistor R2, and the terminal 12 of emitter 22 of the transistor 14 is connected via relatively low resistance film 23 to relatively high resistance film 16 which comprises resistor R1. Relatively low resistance film 17 also extends in the manner shown to capacitor C, where it is enlarged to form the lower capacitor plate film 8.

Immediately over film 8 is located a dielectric film 7 which may be of any suitable material, such as silicon monoxide; and immediately above film 7 is positioned relatively low resistance film 6, which as heretofore mentioned, comprises the upper conducting film of the capacitor C.

It will now be apparent that the circuit schematically shown in Fig. 2 is physically embodied within the structure of Fig. 1. Furthermore, it will be apparent that the embodiment of Fig. 1 includes active, as well as passive, elements, all formed on a single substrate which comprises a block of semiconductor material itself.

Although the methods of producing semiconductor devices according to the invention may vary somewhat, depending upon the particular embodiment involved, one illustrative method for producing the embodiment of Fig. 1 is as follows.

Initially, a block of semiconductor material is procured and doped either in its entirety or over an area in which an active circuit element is to be formed. Such doping may be accomplished by any one of several processes, but the one selected for this illustrative description is that of diffusion. Thus, impurities may be diffused in successive operations into the surface of the semiconductor block to form emitter, base, and collector regions.

After doping has been accomplished, upper layer areas other than those required for the active circuit elements may be eliminated by etching, thereby leaving only those desired. Subsequently, the entire remaining block of material may be covered by an insulating coating, ohmic connections made to the several regions of the transistor or other active element, passive elements formed on the surface of the insulating coating, and terminals formed to provide means for making external connections.

Now considering the application of this process to the embodiment of Figs. 1, 3 and 4, it will be seen that the layers 21 and 22 of transistor 14 extend upwardly from block 19, for this structure is made by the initial doping of successive layers over the entire surface of the semiconductor block and the etching for removal of the two layers from all of the block surface except in the relatively small area shown. As is well known in the art, such etching may be accomplished by temporarily coating the semiconductor block with a protective substance in the area desired not to be etched, and then immersing or spraying the block with a suitable etching substance, such as CP-4, described at page 354, Vol. I of *Transistor Technology*, edited by Bridgers, Scaff, and Shive, published by Van Nostrand Company, New York.

The next step in fabrication of the semiconductor device consists of coating the entire member with an insulating layer 20. Although the areas particularly desired to be coated are those upon which the heretofore-mentioned resistive and conducting films are to be deposited, the coating has been shown in the Figures to cover the entire member, since it may be easier thus to apply it. After the insulating layer has been deposited, small apertures are etched therethrough at the desired positions of the emitter, base, and collector terminals 12, 13, and 11. These small apertures may be formed in any one of the variety of ways well known in the art. However, one illustrative manner in which this may be accomplished contemplates the coating of the entire top surface of the member 1 with a photo-resist compound which may then be

exposed to light through a mask having opaque areas immediately adjacent the areas in which it is desired to form the aforementioned apertures. The assembly may then be washed to remove the photo-resist material from those unexposed areas atop the emitter, base, and collector regions, and the assembly may then be bronght into contact with an etching solution which is effective to etch through the insulating coating to form recesses of the desired depth. After this has been accomplished, the photo-resist material is removed by immersion in methylene chloride.

Next, the assembly is mechanically masked over its entire surface except where the recesses have been etched, and suitable ohmic-contact-making material is evaporated or otherwise deposited therein. Thus, for example, if an NPN-type transistor is being formed, a mask might be used to cover all of the surface except the emitter and collector recesses, and antimony-doped gold or other suitable material could be evaporated or otherwise deposited through the mask into the recesses. Thereafter, the entire surface of the member 1 could be masked except for the base recess, into which a suitable ohmic-contact-making material such as aluminum might be evaporated or otherwise deposited. After this has been accomplished, the entire assembly is heated to a predetermined temperature at which the deposited material alloys with the base, emitter, and collector to form severally distinct ohmic contacts therewith. Since the principles of alloying ohmic contacts to semiconductor devices are well known in the art, no further description of details thereof will be given here.

After the afore-mentioned ohmic contacts have been made, either the resistive films or the highly conductive films can be next applied. Assuming, for the purposes of this description, that highly conductive films are next applied, a mask is fitted over the surface of the member 1 to expose only those areas shown (in Fig. 1) with a cross hatch line extending upwardly to the right. These areas comprise those identified with the numerals 15, 23, 17, 2, 3, 5, and the lowermost plate 8 of capacitor C. Next, any suitable highly conductive material, such as copper or gold, is applied by vacuum deposition technique such as that described in the book, *Vacuum Deposition of Thin Films*, by Holland, published by Chapman & Hall, 1956. A relatively thick film is applied to the indicated areas in order that the resistance thereof may be made low.

After the low resistance films have been applied, the surface is exposed through a different mask to permit deposition of a relatively thin film of highly resistive materials, such as nichrome (Registered Trade Mark), to the areas indicated in Fig. 1 with cross-hatched lines extending upwardly to the left.

Next, the entire surface may be covered with an insulating material which serves both as a dielectric for capacitor C and as a coating to protect the metal films from oxidation and deterioration. This dielectric film is shown in Fig. 1 as covering only the area identified with the symbol 7 and an extension over the plate 8 in order that the Figure may be more readily understood. Of course, if it were desired to coat only the area indicated by numeral 7, a mask having a rectangular aperture in the position of rectangle 7 could be employed to prevent deposit other than in this area.

After the dielectric has been deposited, the area indicated by the symbols 4 and 6 is coated with a highly conductive film similar to that employed for film 8, and the capacitor is thereby completed.

Although the embodiment of Fig. 1 does not include an inductance element, it will be obvious to one skilled in the art that a semiconductor device according to the invention could include such an element. For a detailed explanation of the manner in which one may apply spiral inductances to a flat surface, reference is hereby made to pages 17 and 18 of the booklet entitled, "Printed Circuit Techniques," by Cledo Brunetti and Roger Curtis, National Bureau of Standards Circular 468, issued November 15, 1947.

It will now be seen that the entire member depicted in Figs. 1, 3, and 4 has been formed in such manner that both active and passive elements are provided in one physically integrated member of extremely small size. Thus, in one actual embodiment according to Fig. 1, the dimensions in inches were only 0.10 by 0.10 by 0.01.

It will also be apparent that the teachings of the afore-mentioned pending application could be advantageously combined with the teachings of the invention described in this application to produce a structure exhibiting the advantages and features of both thereof. Thus, for example, the active semiconductor elements, the resistance elements whose value is not critical, and the distributed capacitance elements could be formed in the manner described in the pending application, and high stability resistors, capacitors, and inductors formed in the manner described herein. Connections therebetween could be made by etching apertures through the insulating coating at the desired points and the depositing of suitable ohmic-contact-making material to provide connections as described above.

WHAT WE CLAIM IS :—

1. A device comprising a body of semiconductor material having a first region of one type conductivity and a second region of opposite type conductivity contiguous

exposed to light through a mask having opaque areas immediately adjacent the areas in which it is desired to form the aforementioned apertures. The assembly may then be washed to remove the photo-resist material from those unexposed areas atop the emitter, base, and collector regions, and the assembly may then be bronght into contact with an etching solution which is effective to etch through the insulating coating to form recesses of the desired depth. After this has been accomplished, the photo-resist material is removed by immersion in methylene chloride.

Next, the assembly is mechanically masked over its entire surface except where the recesses have been etched, and suitable ohmic-contact-making material is evaporated or otherwise deposited therein. Thus, for example, if an NPN-type transistor is being formed, a mask might be used to cover all of the surface except the emitter and collector recesses, and antimony-doped gold or other suitable material could be evaporated or otherwise deposited through the mask into the recesses. Thereafter, the entire surface of the member 1 could be masked except for the base recess, into which a suitable ohmic-contact-making material such as aluminum might be evaporated or otherwise deposited. After this has been accomplished, the entire assembly is heated to a predetermined temperature at which the deposited material alloys with the base, emitter, and collector to form severally distinct ohmic contacts therewith. Since the principles of alloying ohmic contacts to semiconductor devices are well known in the art, no further description of details thereof will be given here.

After the afore-mentioned ohmic contacts have been made, either the resistive films or the highly conductive films can be next applied. Assuming, for the purposes of this description, that highly conductive films are next applied, a mask is fitted over the surface of the member 1 to expose only those areas shown (in Fig. 1) with a cross hatch line extending upwardly to the right. These areas comprise those identified with the numerals 15, 23, 17, 2, 3, 5, and the lowermost plate 8 of capacitor C. Next, any suitable highly conductive material, such as copper or gold, is applied by vacuum deposition technique such as that described in the book, *Vacuum Deposition of Thin Films*, by Holland, published by Chapman & Hall, 1956. A relatively thick film is applied to the indicated areas in order that the resistance thereof may be made low.

After the low resistance films have been applied, the surface is exposed through a different mask to permit deposition of a relatively thin film of highly resistive materials, such as nichrome (Registered Trade Mark), to the areas indicated in Fig. 1 with cross-hatched lines extending upwardly to the left.

Next, the entire surface may be covered with an insulating material which serves both as a dielectric for capacitor C and as a coating to protect the metal films from oxidation and deterioration. This dielectric film is shown in Fig. 1 as covering only the area identified with the symbol 7 and an extension over the plate 8 in order that the Figure may be more readily understood. Of course, if it were desired to coat only the area indicated by numeral 7, a mask having a rectangular aperture in the position of rectangle 7 could be employed to prevent deposit other than in this area.

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Although the embodiment of Fig. 1 does not include an inductance element, it will be obvious to one skilled in the art that a semiconductor device according to the invention could include such an element. For a detailed explanation of the manner in which one may apply spiral inductances to a flat surface, reference is hereby made to pages 17 and 18 of the booklet entitled, "Printed Circuit Techniques," by Cledo Brunetti and Roger Curtis, National Bureau of Standards Circular 468, issued November 15, 1947.

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It will also be apparent that the teachings of the afore-mentioned pending application could be advantageously combined with the teachings of the invention described in this application to produce a structure exhibiting the advantages and features of both thereof. Thus, for example, the active semiconductor elements, the resistance elements whose value is not critical, and the distributed capacitance elements could be formed in the manner described in the pending application, and high stability resistors, capacitors, and inductors formed in the manner described herein. Connections therebetween could be made by etching apertures through the insulating coating at the desired points and the depositing of suitable ohmic-contact-making material to provide connections as described above.

WHAT WE CLAIM IS :—

1. A device comprising a body of semiconductor material having a first region of one type conductivity and a second region of opposite type conductivity contiguous

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thereto to form a P-N junction, said regions extending to one and the same surface of said body, insulating material on said one surface, and at least one passive circuit element formed on said insulating material.

2. A device comprising a body of semiconductor material having a first region of one type conductivity and a second region of opposite type conductivity contiguous thereto to form a P-N junction, said regions extending to one and the same surface of said body and being spaced from the opposite surface of said body, insulating material on said one surface, and at least one passive circuit element formed on said insulating material.

3. A device according to claim 1 or 2, wherein said P-N junction defines at said one surface a first enclosed area, said first region overlies said second region, the region immediately underlying said second region having said one conductivity type thereby forming with said second region another P-N junction defining at said one surface a second enclosed area surrounding said first enclosed area.

4. A device according to any preceding claim, wherein said insulating material defines an aperture therein extending to said one surface, a contact element positioned at least partially within said aperture ohmically contacting one of said regions, and conductive material extending from said contact element and positioned on said insulating material.

5. A device according to claims 3 and 4, wherein said insulating material defines another aperture therein extending to said one surface, another contact element positioned at least partially within said other aperture ohmically contacting another of said regions, and conductive material extending from said other contact element and positioned on said insulating material.

6. A device according to claim 5, wherein said insulating material defines a further aperture therein extending to said one surface, a further contact element positioned at least partially within said further aperture ohmically contacting a further one of said regions, and conductive material extending from said further contact element and positioned on said insulating material.

7. A device according to any preceding claim, wherein the passive circuit element or passive circuit elements is or are connected to a selected one or both or selected ones of said regions or interconnected or provided with terminal connections by conductive material and/or conductive material overlying further insulating material on said first-mentioned insulating material.

8. A device according to any preceding claim, including insulating material overlying said passive circuit element or selected passive circuit elements.

9. A device according to claim 3, wherein said first region, said second region and said region immediately underlying said second region are the emitter, base and collector regions respectively of a transistor, said passive circuit element or one said passive circuit element is a resistor including a resistive film on said insulating material and including conductive material on said insulating material interconnecting one end of said resistive film and one of said regions.

10. A device comprising an electrical network having at least one circuit element which includes a P-N junction and at least one passive other circuit element, a body of semiconductor material, the or each P-N junction circuit element of said electrical network being formed in said body and having regions of opposite conductivity types thereof extending to one and the same surface of said body, insulating material on said one surface, and the or each passive other circuit element of said electrical network being formed on said insulating material.

11. A semiconductor device according to claim 10, including two or more passive circuit other elements and conductive material overlying said insulating material and interconnecting selected passive other circuit elements with each other and with selected ones of said regions.

12. A semiconductor device according to claim 10 or 11, including insulating material overlying said passive other circuit element or elements or selected ones of said passive other circuit elements.

13. A device according to claim 11 or claims 11 and 12, including insulating material overlying said conductive material.

14. A method of producing a device comprising the steps of forming, in a body of semiconductor material, a first region of one type conductivity extending to one surface of said body, forming, in said body contiguous with said first region, a second region of opposite conductivity type extending to said one surface, forming insulating material on said one surface, and forming at least one passive circuit element on said insulating material.

15. A method of producing a device comprising the steps of forming, in a body of semiconductor material, a first region of one type conductivity extending to one surface of said body and spaced from the opposite surface of said body, forming, in said body contiguous with said first region, a second region of opposite conductivity type extending to said one surface and being spaced from said opposite surface, forming insulating material on said one surface, and forming at least one passive circuit element on said insulating material.

16. A method according to claim 14 or



15, including the steps of forming an aperture in said insulating material extending to said one surface, positioning a contact element at least partially within said aperture to ohmically contact one of said regions, and extending conductive material from said contact element over said insulating material.

17. A method according to claim 16, comprising the steps of forming another aperture in said insulating material extending to said one surface, positioning another contact element at least partially within said another aperture to ohmically contact the other of said regions, and extending conductive material from said other contact element over said insulating material.

18. A method according to any of claims 14 to 17, including the step of connecting a selected one or both of said regions to the passive circuit element or elements.

19. A method according to claim 18, wherein said step of connecting includes applying conductive material on said insulating material.

20. A method according to any of claims 14 to 19, wherein said passive circuit elements or at least one of said passive circuit elements formed on said insulating material is formed by applying a resistive film thereon.

21. A method according to claim 16 or 17 and claim 19 and/or 20, wherein insulating material is formed over said conductive material and/or said resistive film.

22. A method according to claim 21, wherein another passive circuit element formed on said insulating material is a capacitor and one plate of said capacitor is formed on said insulating material concurrently with the application of said conductive material in said step of connecting.

23. A method according to any of claims 14 to 22, wherein at least one of said regions is formed by the step of diffusion.

24. A method of producing a semiconductor device consisting of an electrical network having at least one circuit element which includes a P-N junction and at least one passive other circuit element, comprising the steps of forming, in a body of semiconductor material, the or each P-N junction circuit element of said electrical network with the regions thereof extending to one and the same surface of said body, forming insulating material on said one surface, and forming the or each passive other circuit element of said electrical network on said insulating material.

25. A method according to claim 24, wherein the device includes two or more passive other circuit elements comprising the steps of applying conductive material on said insulating material to interconnect the or selected passive other circuit elements with each other and with selected ones of said regions.

26. A method according to claim 25, wherein at least one of said regions is formed by the step of diffusion.

27. A method according to claim 24, wherein said or at least one of said passive other circuit elements is a resistor formed on said insulating material by applying a resistive film thereon.

28. A method according to claim 27, wherein the other or another of said passive other circuit elements is a capacitor and one plate of said capacitor is formed on said insulating material concurrently with the application of said conductive material.

29. A method according to claim 24, wherein a resistor is formed on said insulating material by applying a resistive film thereon, one plate of a capacitor is applied on said insulating material, the capacitor dielectric is applied on said one plate, and insulating material is applied on said resistive film concurrently with the application of said capacitor dielectric.

30. A method according to any of claims 24 to 27, including the step of forming insulating material on said passive other circuit element or elements.

31. A method according to claims 25 and 30, including the step of forming insulating material on said conductive material.

32. A device when produced by the method of any of claims 14 to 31.

33. A semiconductor device substantially as hereinbefore described with reference to Figs. 1 to 4 of the accompanying drawing.

34. A transistor comprising a body of semiconductor material containing the emitter, base and collector regions of alternating conductivity type, the successive regions overlying one another and all extending to one and the same face of said body, insulating material on selected areas of said one face, and contact elements secured to said one face and ohmically connecting to each of said regions.

35. A transistor according to claim 34, including conductive material extending from each contact element and positioned on said insulating material.

36. A transistor according to claim 35, including further insulating material on said conductive material.

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