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(54) AN ELECTRONIC ALARM TIMEPIECE

(71) We, KABUSHIKI KAISHA DAINI SEIKOSHA, a Japanese Company of 6-31-1, Kameido, Koto-ku, Tokyo, Japan, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed to be particularly described in and by the following statement:—

This invention relates to electronic alarm timepieces.

In conventional electronic alarm timepieces an alarm device producing an audible warning when a predetermined alarm time is reached has many advantages but cannot, produce an alarm at a given time each day unless it is set each day. On the other hand, a repeat alarm device for producing an alarm at a predetermined time each day must be reset if it is desired to produce more than one alarm on any given day.

According to the present invention there is provided an electronic alarm timepiece comprising: a timekeeping circuit for producing an actual time of day indication; a once only alarm circuit in which a first alarm time is memorised; a continuous alarm circuit in which a second alarm time which may be the same as or different from the first alarm time is memorised; a coincidence circuit for producing an output signal when the alarm time memorised in the once only alarm circuit and/or continuous alarm circuit coincide with the actual time of day indication; and alarm means for producing an alarm indication in response to the output signal from the coincidence circuit.

Preferably the once only alarm circuit is connected to be reset by the output signal from the coincidence circuit.

The timepiece, in the preferred embodiment, includes means for alternately passing the contents of the one only alarm circuit and the continuous alarm circuit to the coincidence circuit.

The timepiece preferably includes selecting/setting means for selectively

setting an alarm time in the once only alarm circuit and in the continuous alarm circuit. 50

The continuous alarm circuit may be such that the alarm time is memorised therein until altered by means of the selecting/setting means.

The invention is illustrated, merely by way of example, in the accompanying drawings, in which:— 55

Figure 1 is a block diagram of an embodiment of an electronic alarm timepiece according to the present invention; 60

Figure 2 is a circuit diagram illustrating the electronic alarm timepiece of Figure 1 in greater detail; and

Figure 3 is a circuit diagram of a channel selecting/alarm time setting circuit, of the electronic alarm timepiece of Figure 1. 65

Figure 1 is a block diagram of an embodiment of an electronic alarm timepiece according to the present invention having a time counter 1 for producing an actual time of day indication, a coincidence circuit 2 for energising an alarm device 5 when the actual time of day indication and an alarm time, i.e. the time when an alarm is to be produced, coincide, a once only alarm counter 3, a continuous alarm counter 4 and a channel selecting/alarm time setting circuit 6 for selectively setting an alarm time in the alarm counters 3, 4. The alarm device 5 may be a buzzer or light emitting diode or liquid crystal element. 70

The above electronic alarm timepiece operates as follows. The alarm device 5 is energised when the actual time of day indication i.e. the contents of the time counter 1 which is fed with a standard time signal having a frequency of 1 Hz from an oscillator/frequency dividing circuit 7, coincides with the alarm time i.e. the contents of the alarm counters, 3, 4. When the contents of the alarm counter 3 coincides with the contents of the time counter 1, the alarm counter 3 is reset by a reset signal from the coincidence circuit 2 so that the alarm time memorised thereby is 85 90 95

erased, and the alarm counter 3 causes the alarm device 5 to be energised once when the alarm time and the time indication coincide.

5 When the contents of the alarm counter 4 coincide with the contents of the time counter 1, a reset signal is not applied to the alarm counter 3. Further, a reset signal is not applied to the alarm counter 4 which can only be reset by external means (not shown in Figure 1). Thus an alarm is generated by the alarm device whenever the alarm time set in the alarm counter 4 which can only be reset by external means (not shown in Figure 1). Thus an alarm is generated by the alarm device whenever the alarm time set in the alarm counter 4 is reached and the alarm is cancelled by the external means.

20 The alarm counters 3, 4 constitute different channels which are selected by the channel/selecting alarm timesetting circuit 6. It is, of course, possible to set different alarm times on the two alarm counters.

25 The electronic alarm timepiece of Figure 1 will be described in greater detail with reference to Figure 2. A clock pulse signal having a frequency of 32 Hz is generated by the oscillator/frequency dividing circuit 7. The comparison of the contents of the alarm counter 3 and the contents of the alarm counter 4 with the contents of the time counter 1 is effected every 1/32 seconds (31 msec) that is to say, the contents of the alarm counters 3, 4 are alternately compared with the contents of the time counter 1. When the clock pulse signal from the oscillator/frequency dividing circuit 7 is logical 1 and is applied to an AND gate 21, the latter turns ON to produce an output signal which is applied to one input of an OR gate 22 so that the contents of the time counter 1 and the alarm counter 4 are compared by the coincidence circuit 2 and the alarm device 5 is energised when coincidence occurs. The logical 1 signal from the oscillator/dividing circuit 7 is inverted by an inverter 25 and a logical 0 signal is applied to an AND gate 24 by the inverter 25, so that a reset signal is not applied to the alarm counter 3 to reset the content thereof. Moreover, this logical 0 signal is applied to an AND gate 23 to block the contents of the alarm counter 3.

55 When the clock pulse signal is logical 0, the AND gate 21 blocks the contents of the alarm counter 4 and is also inverted by the inverter 25 to turn the AND gate 23 ON so that the coincidence circuit compares the contents of the time counter 1 and the alarm counter 3 and the alarm device is energised when coincidence occurs. The logical 1 signal from the inverter 25 is also applied to one input of the AND gate 24

whose other input receives the output signal from the coincidence circuit 2 when coincidence occurs. The AND gate 24 therefore produces an output signal of logical 1 which is applied to the alarm counter 3 as a reset signal.

Figure 3 is a detailed circuit diagram of the channel selecting/alarm time setting circuit 6. A switch SW₁ selects the alarm counter 3 and the alarm counter 4 for setting of an alarm time therein, and switches SW₂, SW₃ are provided for amending or resetting the alarm time in the alarm counters 3, 4 respectively. Pulse generating circuits 10A, 10B, 10C each generate a pulse signal when the respective switches SW₁, SW₂, SW₃ are closed. Registers 11, 12 are respectively connected between the pulse generating circuits 10A, 10B and transmission gates 13 to 17.

When a logical 1 signal appears at the output terminal Q₁ of the register 11, the time counter 1 is selected for setting so that the transmission gates 13, 15 are conductive with the result that hours and minutes counters 1A, 1B of the time counter 1 may be set or corrected.

When the switch SW₁ is closed again a pulse signal is generated by the pulse generating circuit 10A and the memorised contents of the register 11 are shifted thereby so that a logical 0 signal appears at the output terminal Q₁. The transmission gates 13, 15 are connected to the transmission gates 16, 17 respectively. At this time a logical 0 signal appears at the output terminal Q₃ of the register 11 and fed to the transmission gate 16 which is connected to an hours counter 3A of the alarm counter 3 and fed to the transmission gate 17 which is connected to a minutes counter 3B of the alarm counter 3.

When the switch SW₂ is closed once to select the hours, a logical 1 appears at the output terminal Q₄ of the register 12. The transmission gate 14 is connected to the transmission gate 13. The transmission gate 13 is connected to the transmission gate 16 whereby the hours counter 3A of the alarm counter 3 may be set by the setting switch SW₁ via the transmission gates 13, 14, 16.

When the switch SW₂ is closed a second time a logical 0 signal appears at the output terminal Q₄ of the register 12 and the transmission gates 14, 15, 17 enable the minutes counter 3B of the alarm counter 3 to be selected. Minutes can thus be set in the minutes counter 3B by means of the switch SW₁.

When the switch SW₁ is closed a third time, a logical 1 signal appears at the output terminal Q₃ of the register 11 and the transmission gates 16, 17 enable minutes and hours of an alarm time to be set in the minutes counter 4B and hours counter 4A

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respectively. In the above manner an alarm time can be set in the alarm counter 3, 4.

WHAT WE CLAIM IS:—

5 1. An electronic alarm timepiece comprising: a timekeeping circuit for producing an actual time of day indication; a once only alarm circuit in which a first alarm time is memorised; a continuous alarm circuit in which a second alarm time
10 which may be the same as or different from the first alarm time is memorised; a coincidence circuit for producing an output signal when the alarm time memorised in the once only alarm circuit and/or
15 continuous alarm circuit coincide with the actual time of day indication; and alarm means for producing an alarm indication in response to the output signal from the coincidence circuit.

20 2. A timepiece as claimed in Claim 1 in which the once only alarm circuit is connected to be reset by the output signal from the coincidence circuit.

3. A timepiece as claimed in Claim 1

including means for alternately passing the contents of the once only alarm circuit and the continuous alarm circuit to the coincidence circuit. 25

4. A timepiece as claimed in any preceding Claim including selecting/setting means for selectively setting an alarm time in the once only alarm circuit and in the continuous alarm circuit. 30

5. A timepiece as claimed in Claim 4 in which the continuous alarm circuit is such that the alarm time is memorised therein until altered by means of the selecting/setting means. 35

6. An electronic alarm timepiece substantially as herein described with reference to and as shown in the accompanying drawings. 40

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4. A timepiece as claimed in any preceding Claim including selecting/setting means for selectively setting an alarm time in the once only alarm circuit and in the continuous alarm circuit. 30

20 2. A timepiece as claimed in Claim 1 in which the once only alarm circuit is connected to be reset by the output signal from the coincidence circuit.

5. A timepiece as claimed in Claim 4 in which the continuous alarm circuit is such that the alarm time is memorised therein until altered by means of the selecting/setting means. 35

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