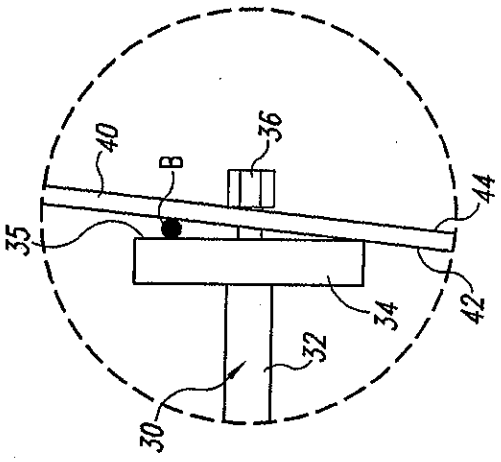

40
B
36
35
44
34
42
32
30

Fig. 2

14
12
16
62
DISPLAY
64
ALARM
38
36
34
44
46
A
40
42
3
3
Fig. 2
D
32
30
50
10
PROCESSOR
60
20
22
A

Fig. 1

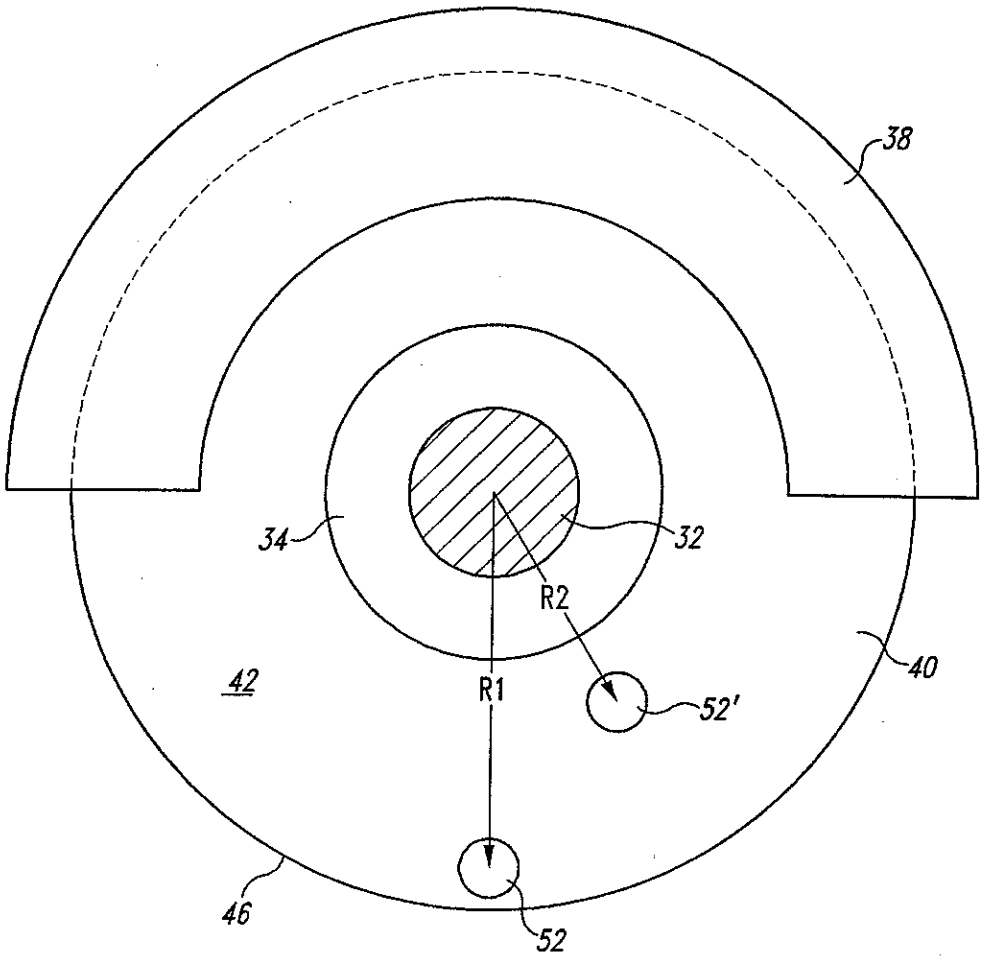


Fig. 3

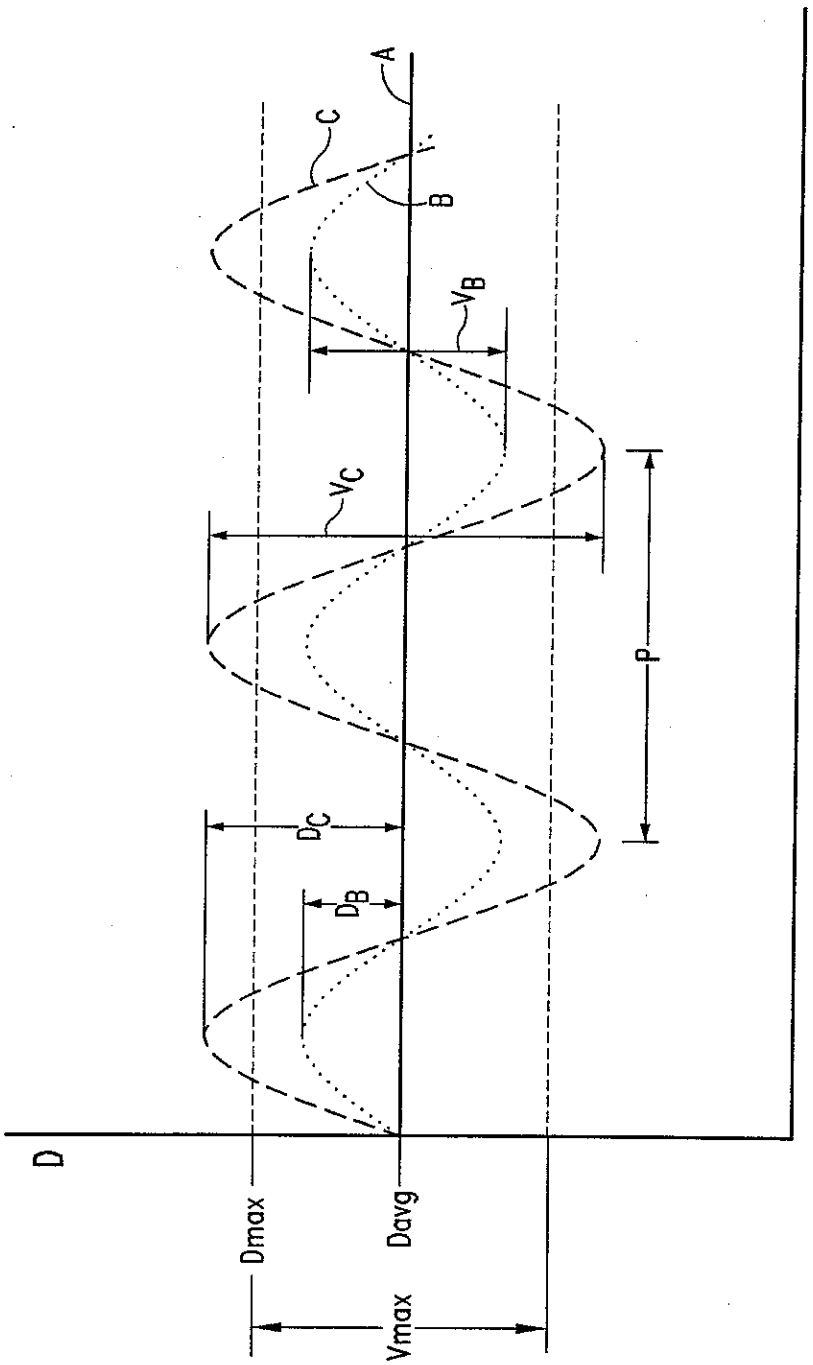


Fig. 4

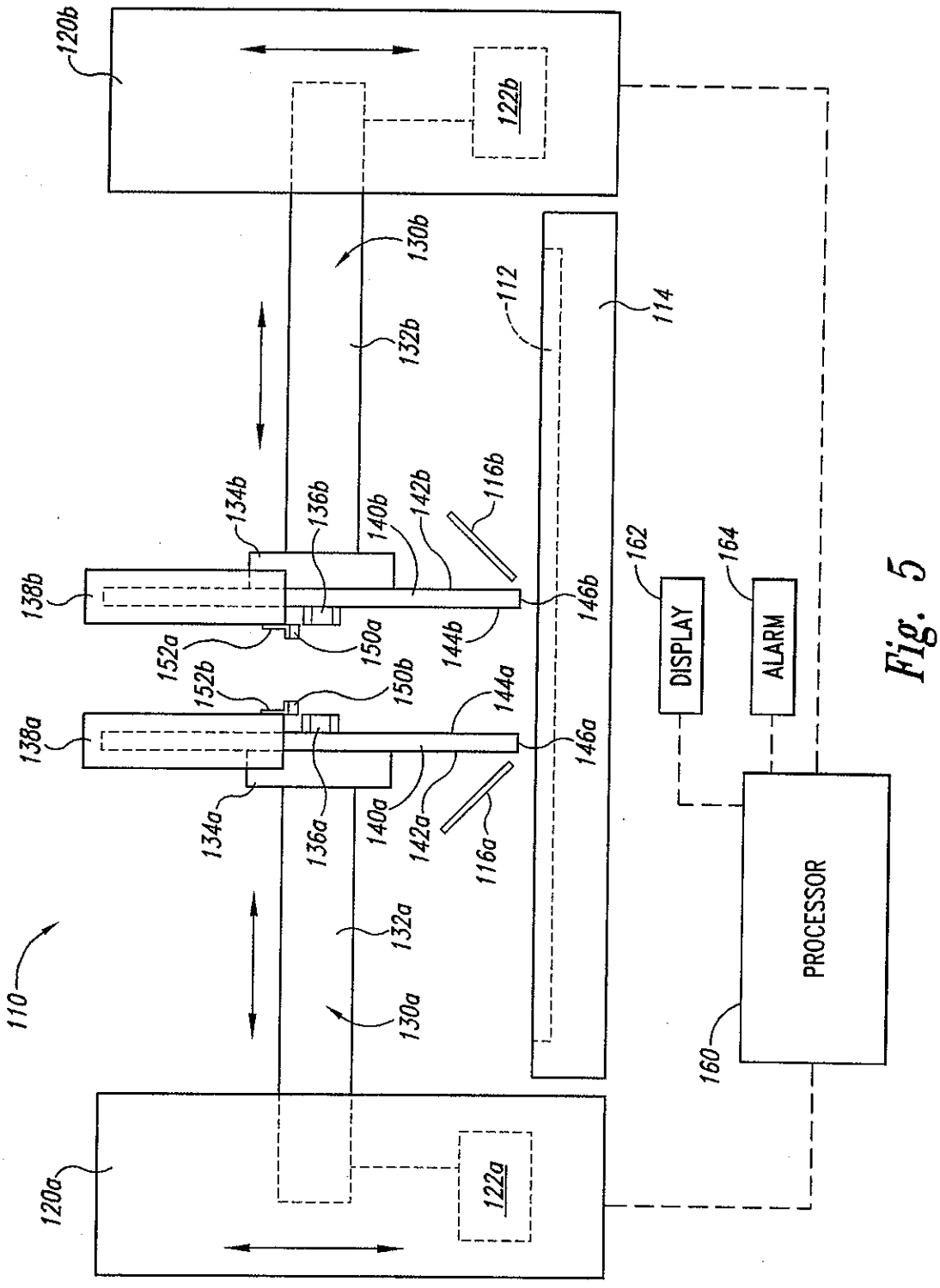

120b
122b
130b
132b
112
114
134b
136b
140b
142b
116b
138b
152a
150a
144b
146b
162
164
DISPLAY
ALARM
152b
150b
144a
138a
146a
134a
136a
140a
142a
116a
110
132a
130a
PROCESSOR
160
120a
122a

Fig. 5

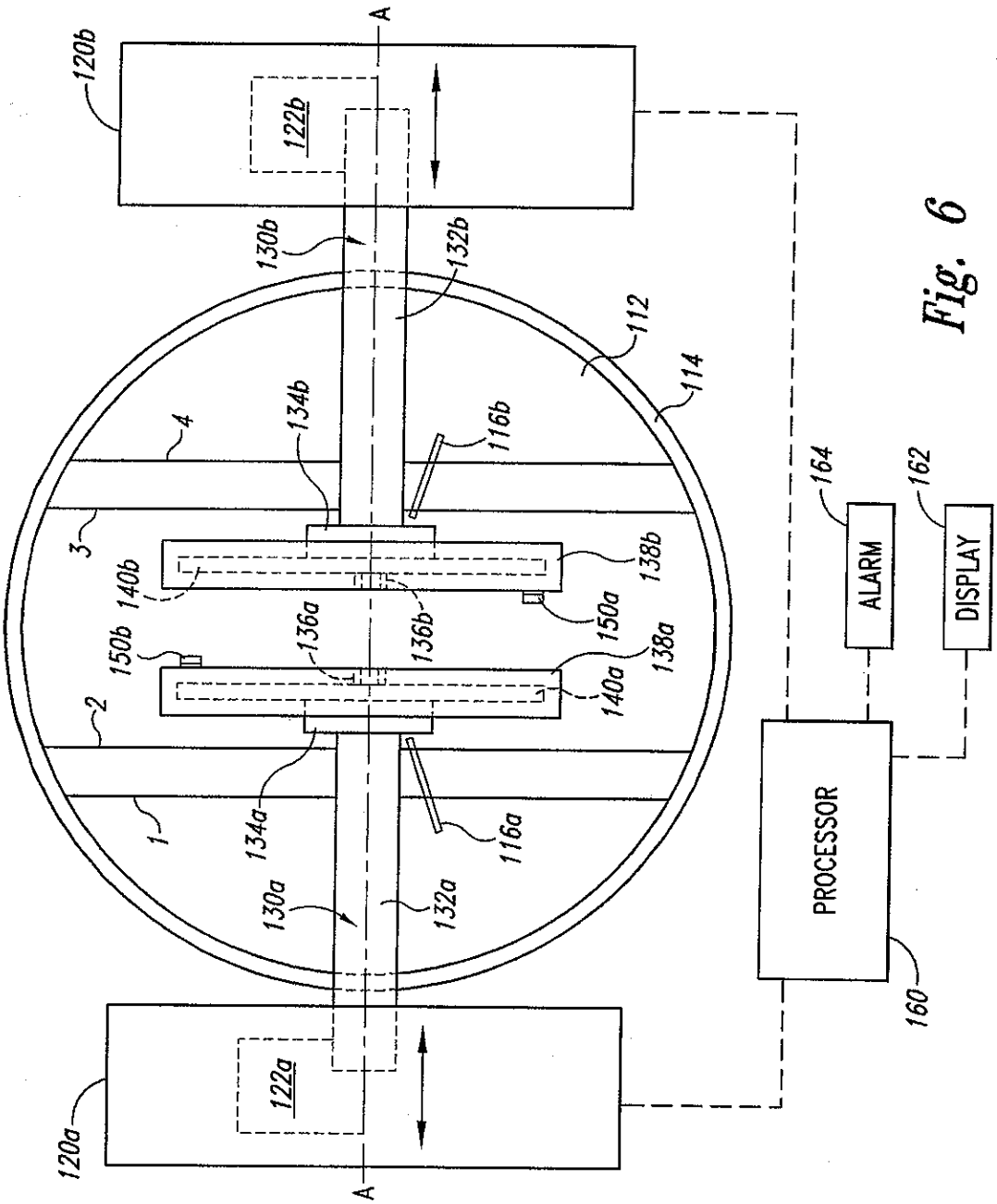

120b
122b
A
130b
132b
112
114
4
134b
116b
3
140b
138b
150a
150b
136a
136b
138a
140a
2
1
134a
116a
130a
132a
A
122a
120a
PROCESSOR
160
ALARM
164
DISPLAY
162

Fig. 6