



(51) International Patent Classification:

B32B 15/01 (2006.01) *H01L 23/26* (2006.01)
H01J 19/70 (2006.01) *H01L 23/10* (2006.01)

(21) International Application Number:

PCT/SG2013/000252

(22) International Filing Date:

18 June 2013 (18.06.2013)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

201204609-0 20 June 2012 (20.06.2012) SG

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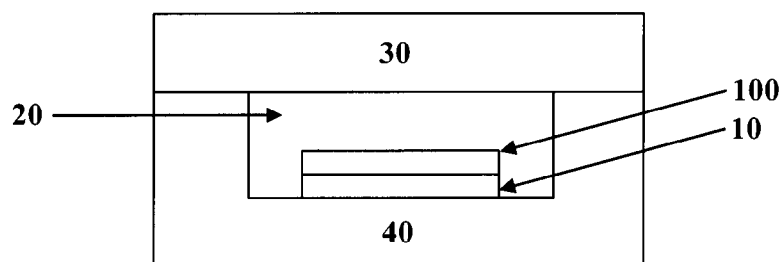
(81) **Designated States** (*unless otherwise indicated, for every
kind of national protection available*): AE, AG, AL, AM,
AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY,
BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM,
DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT,
HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KN, KP, KR,
KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME,
MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ,
OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC,
SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN,
TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) **Designated States** (*unless otherwise indicated, for every
kind of regional protection available*): ARIPO (BW, GH,
GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ,
UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ,
TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK,
EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV,
MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM,
TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW,
KM, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))

(54) Title: A LAYER ARRANGEMENT AND A WAFER LEVEL PACKAGE COMPRISING THE LAYER ARRANGEMENT



(57) **Abstract:** The invention relates to a layer arrangement and a wafer level package comprising the layer arrangement, and in particular, the layer arrangement comprises a getter layer and further comprises a sacrificial layer. The wafer level package may be used in microelectromechanical systems (MEMS) packaging at a vacuum level of about 10 mTorr or less such as close to 1 mTorr (i.e. MEMS vacuum packaging).