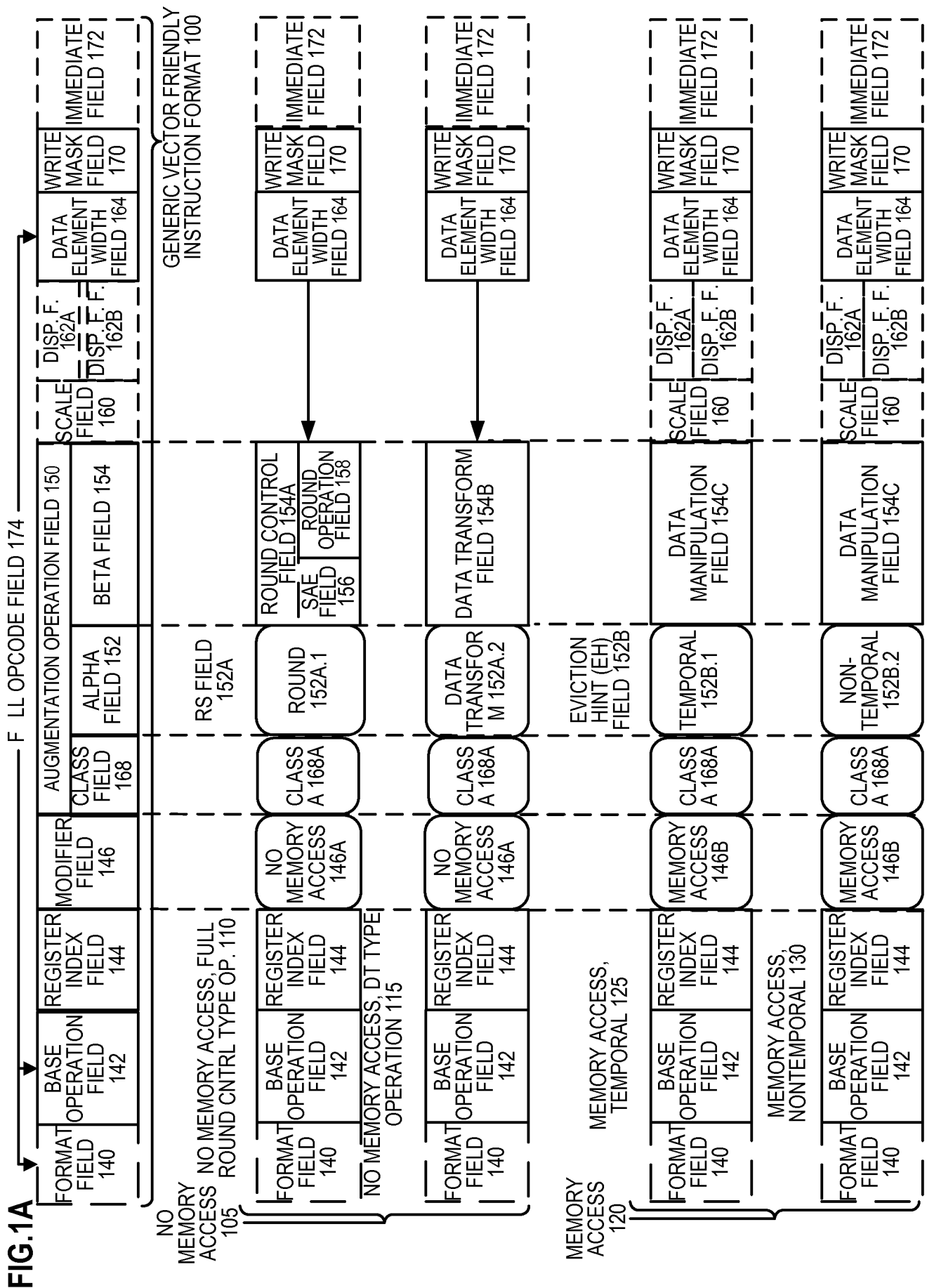
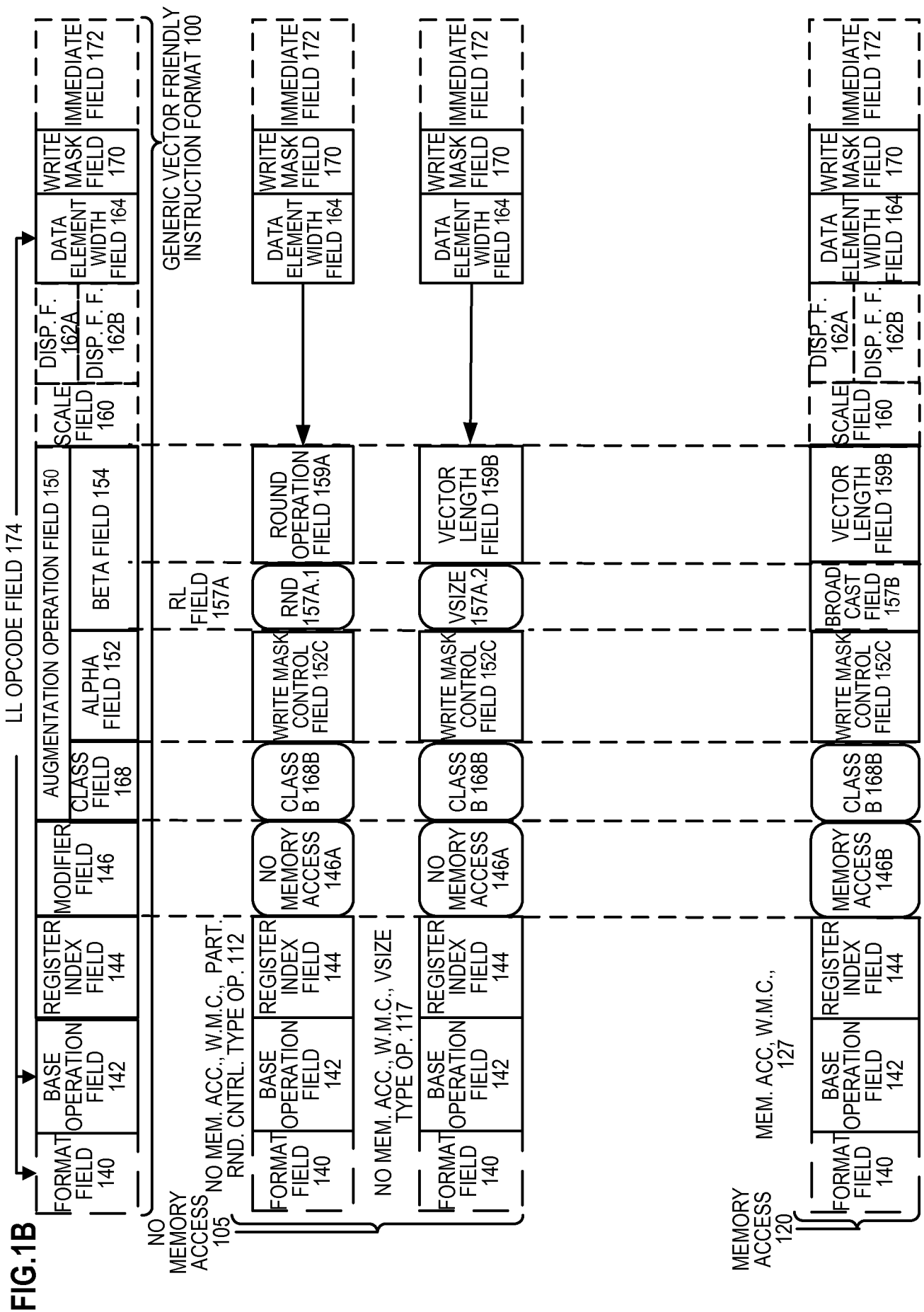






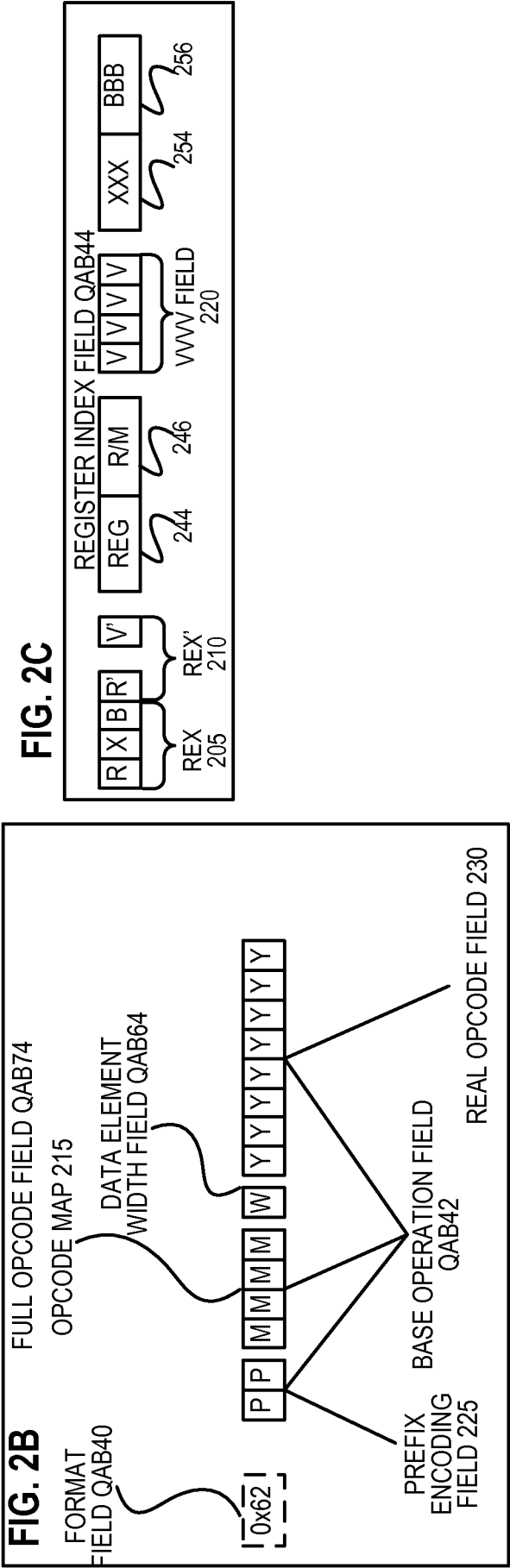
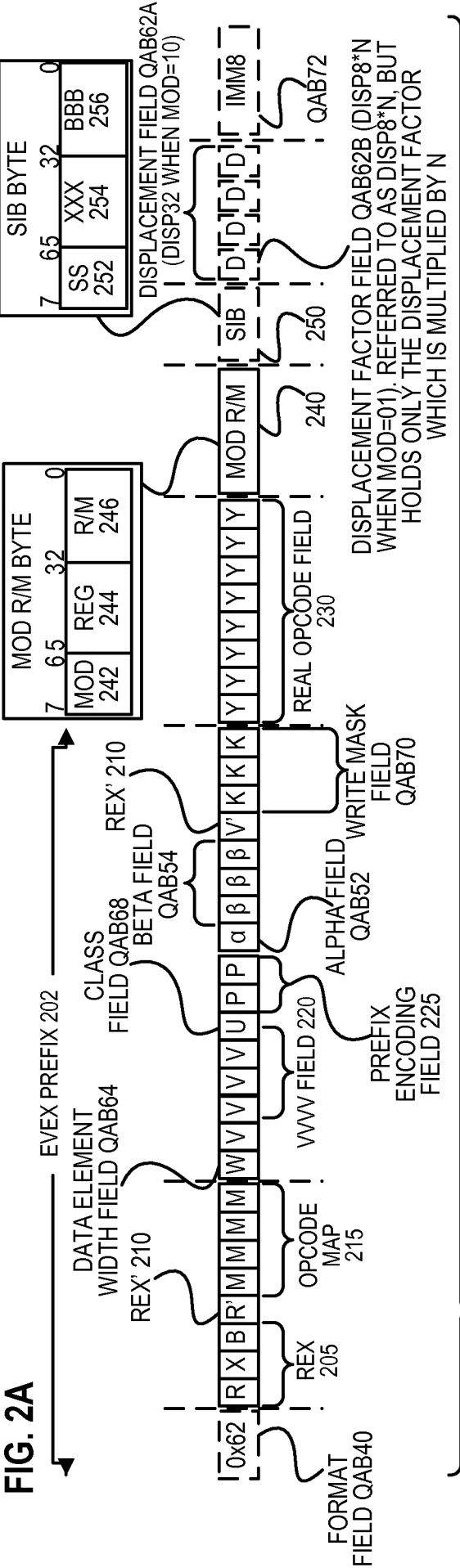
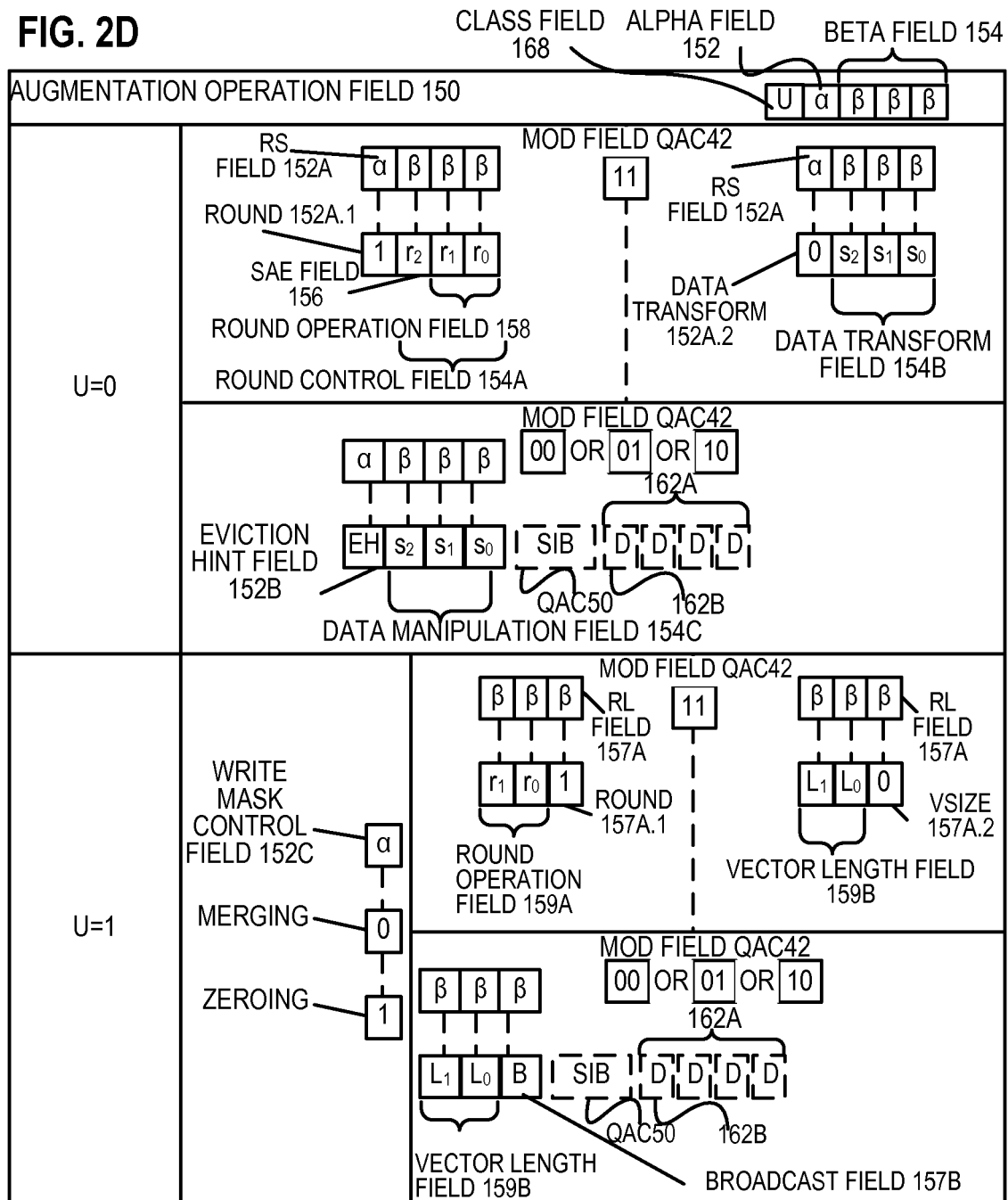
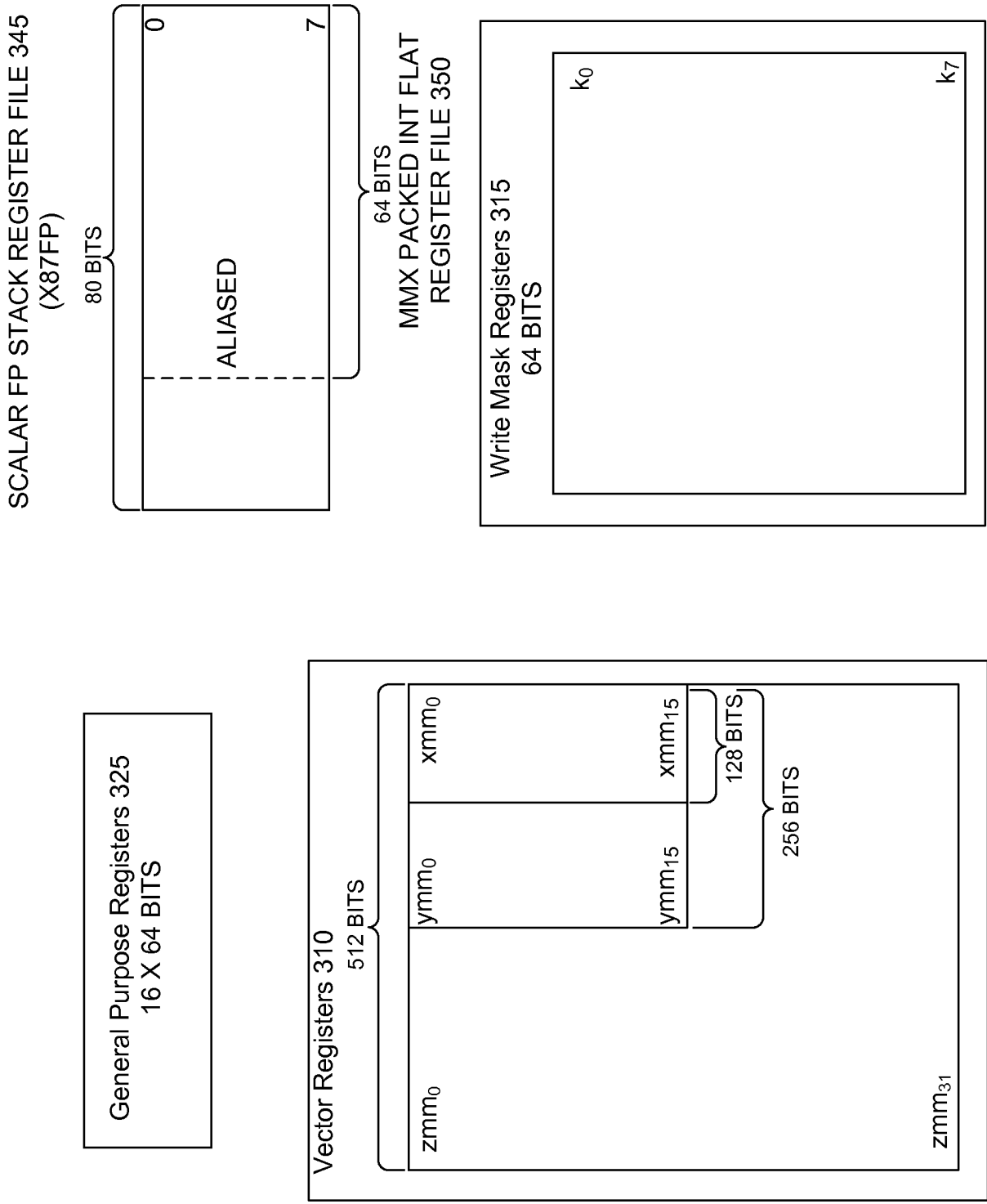


FIG. 2D

REGISTER ARCHITECTURE 300

FIG. 3



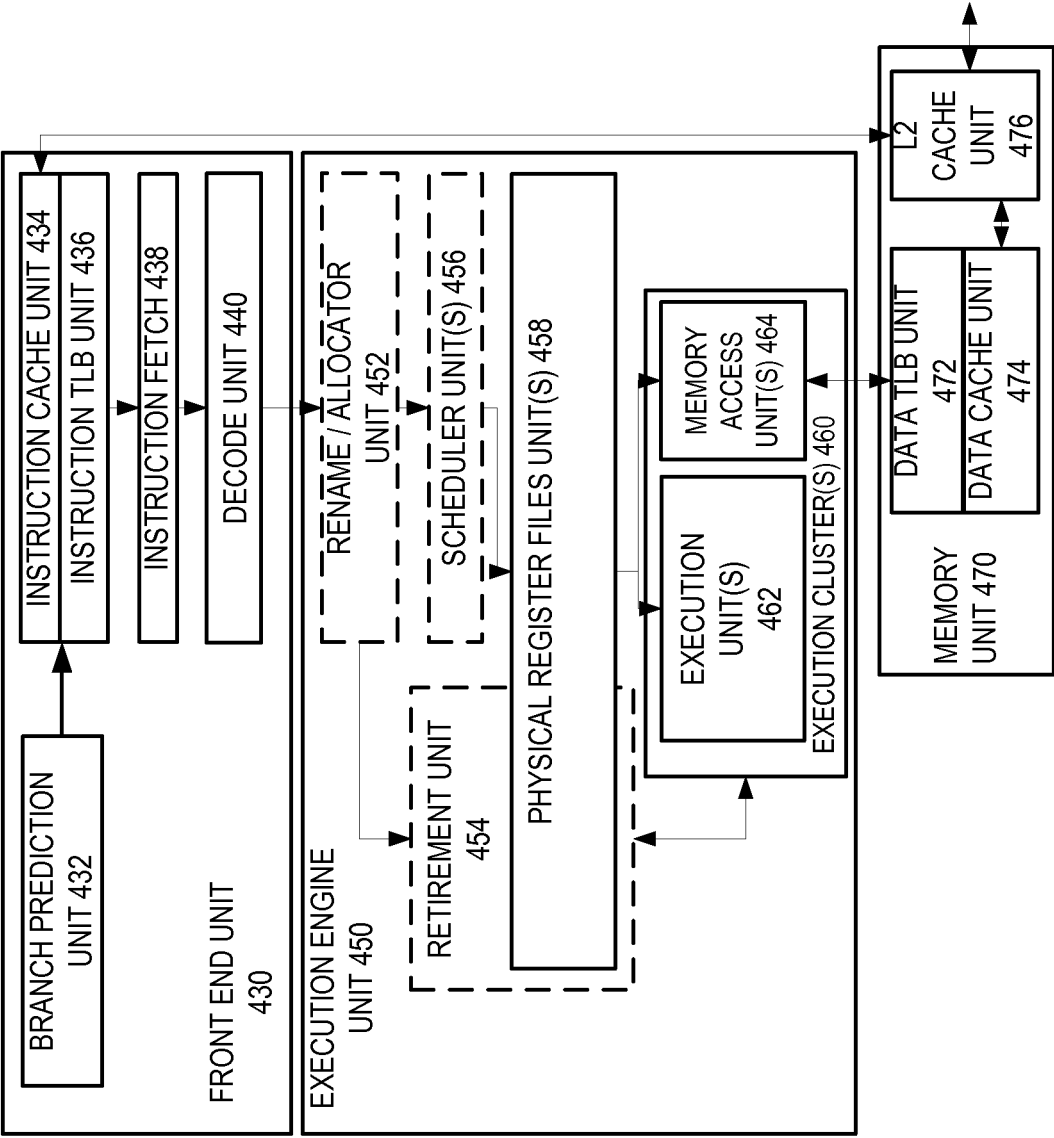
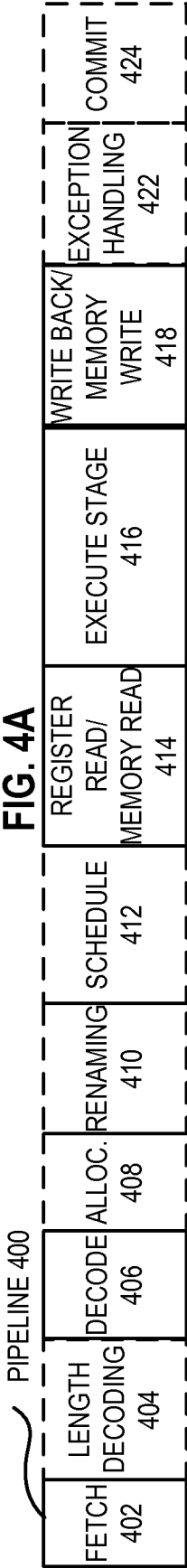


FIG. 5A

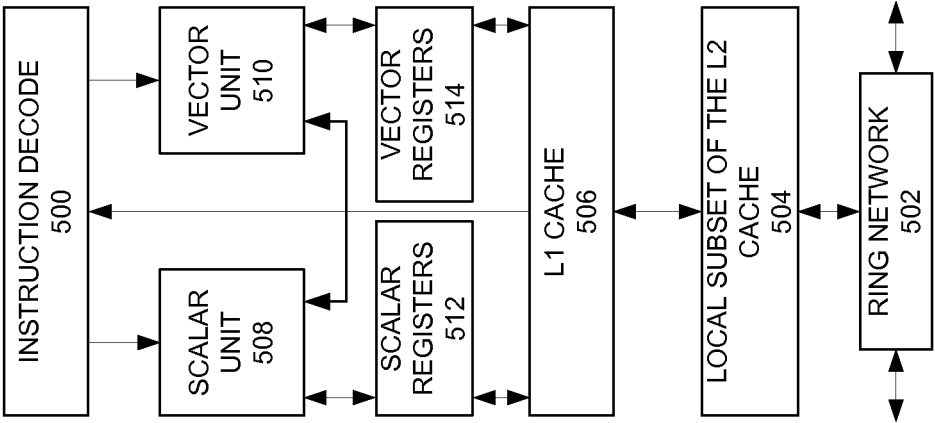
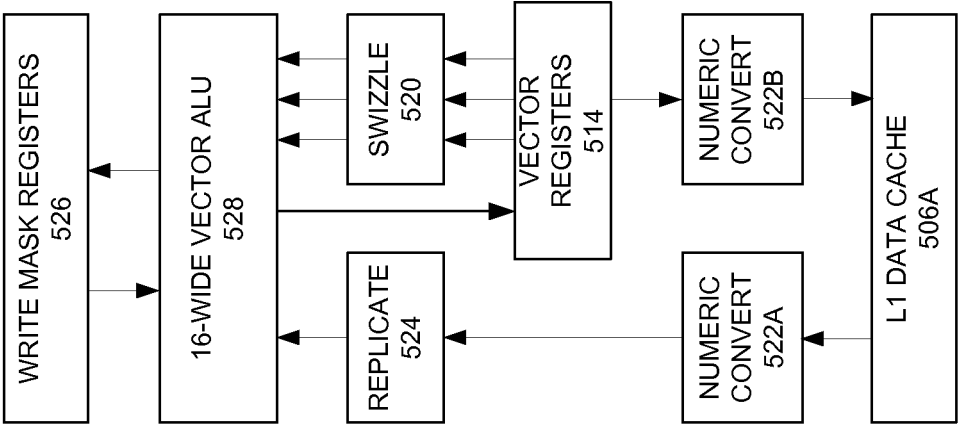


FIG. 5B



PROCESSOR 600

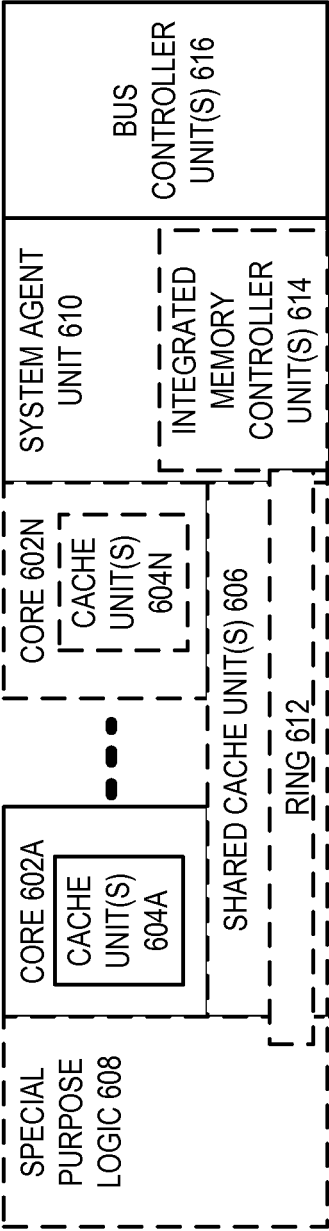
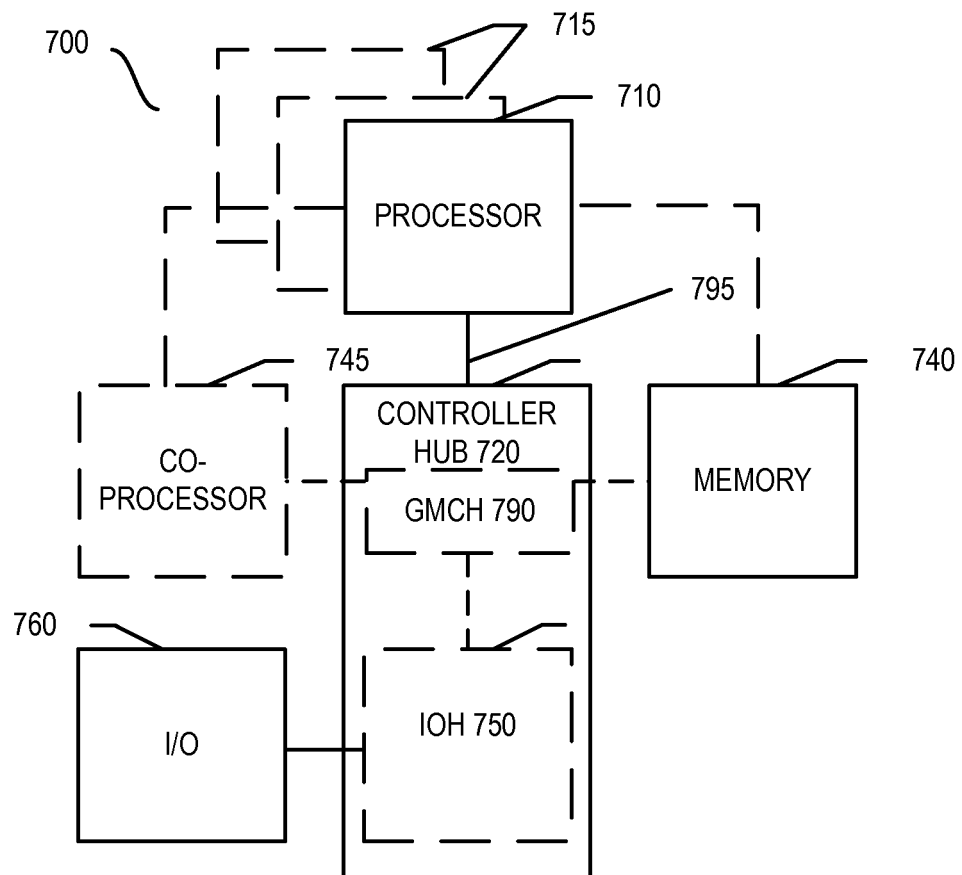


FIG. 6

**FIG. 7**

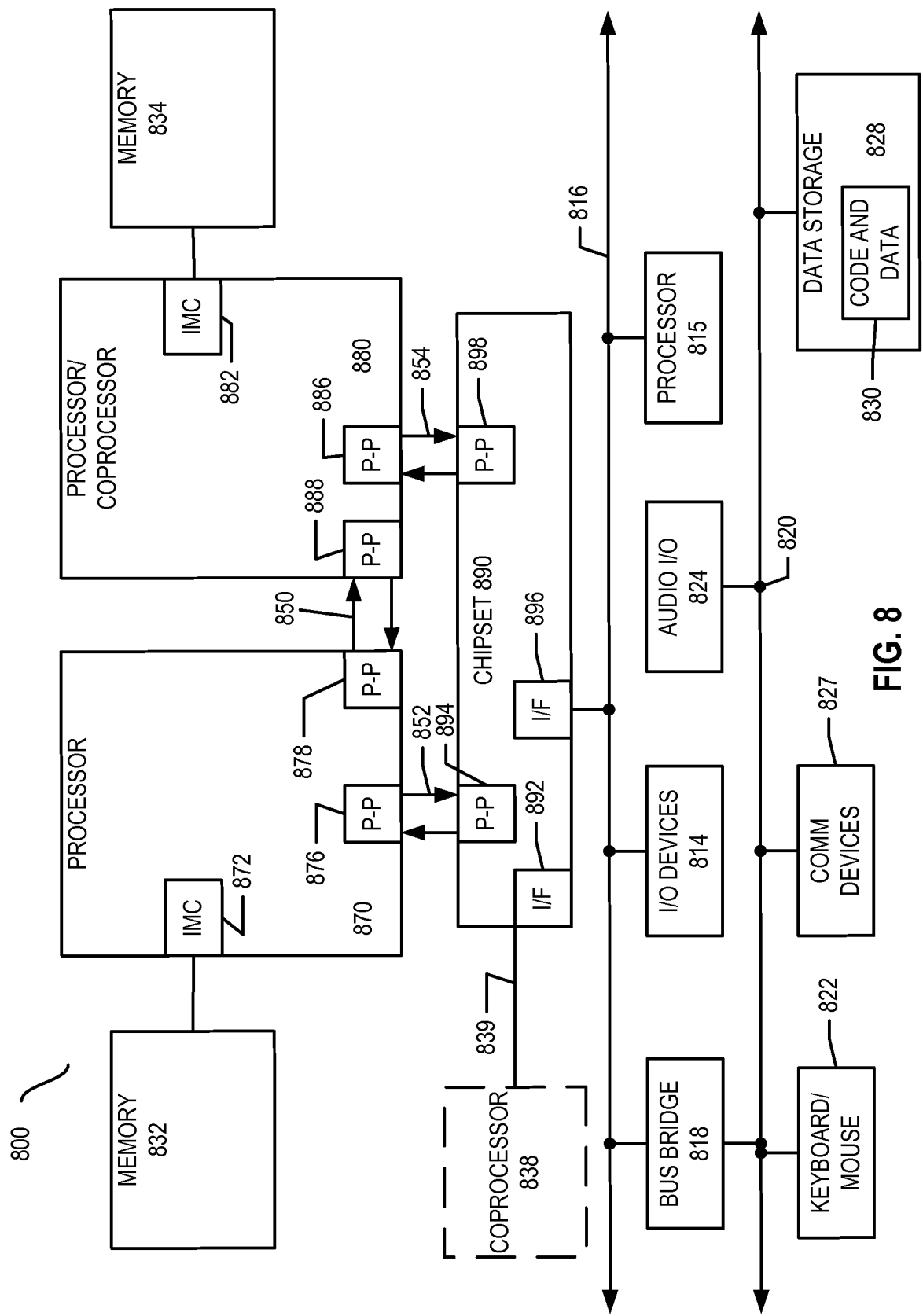


FIG. 8

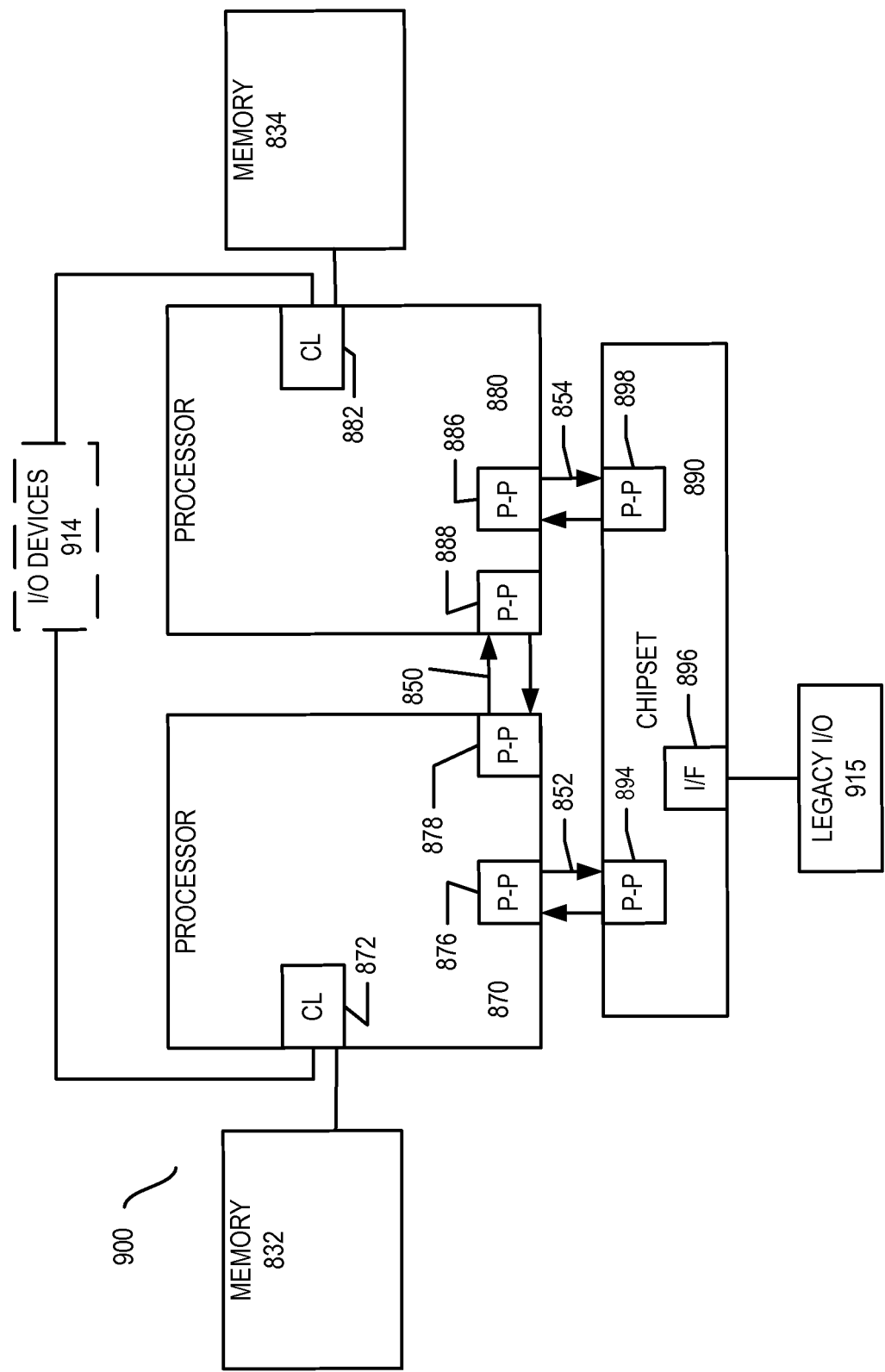


FIG. 9

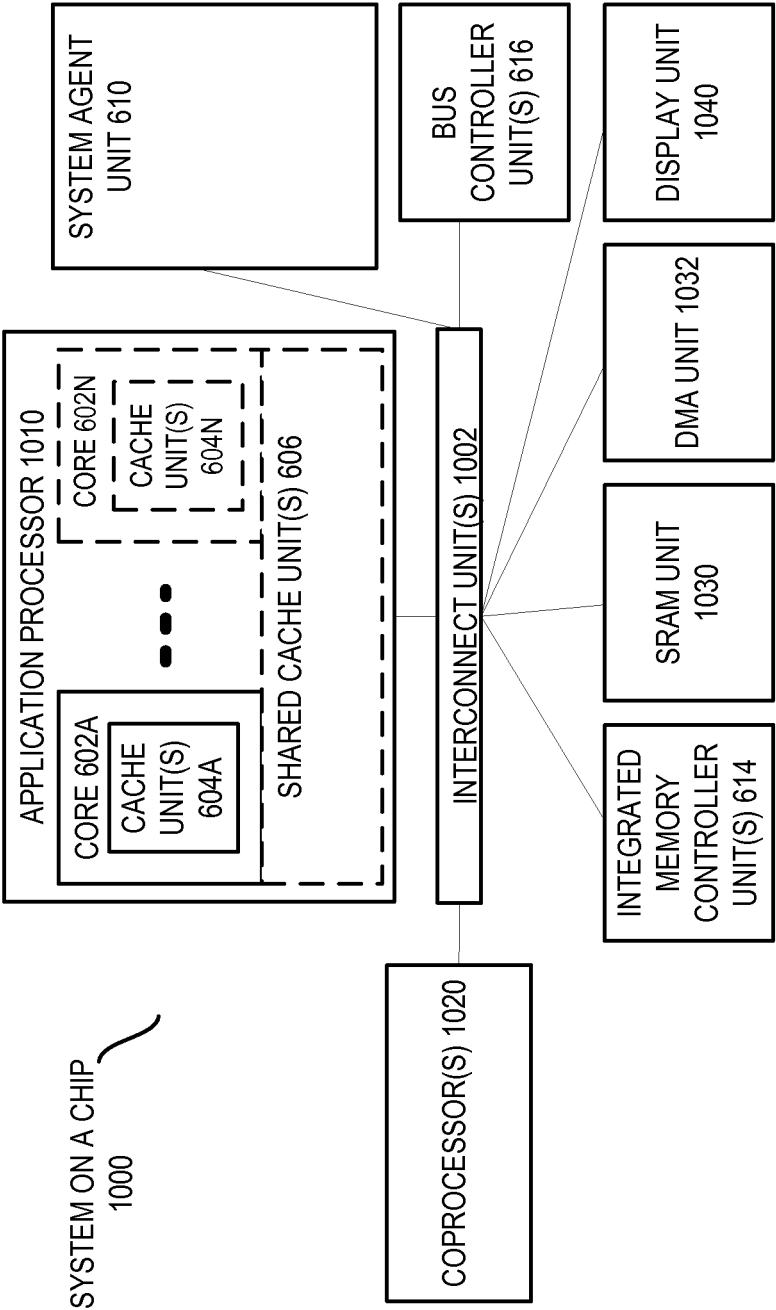
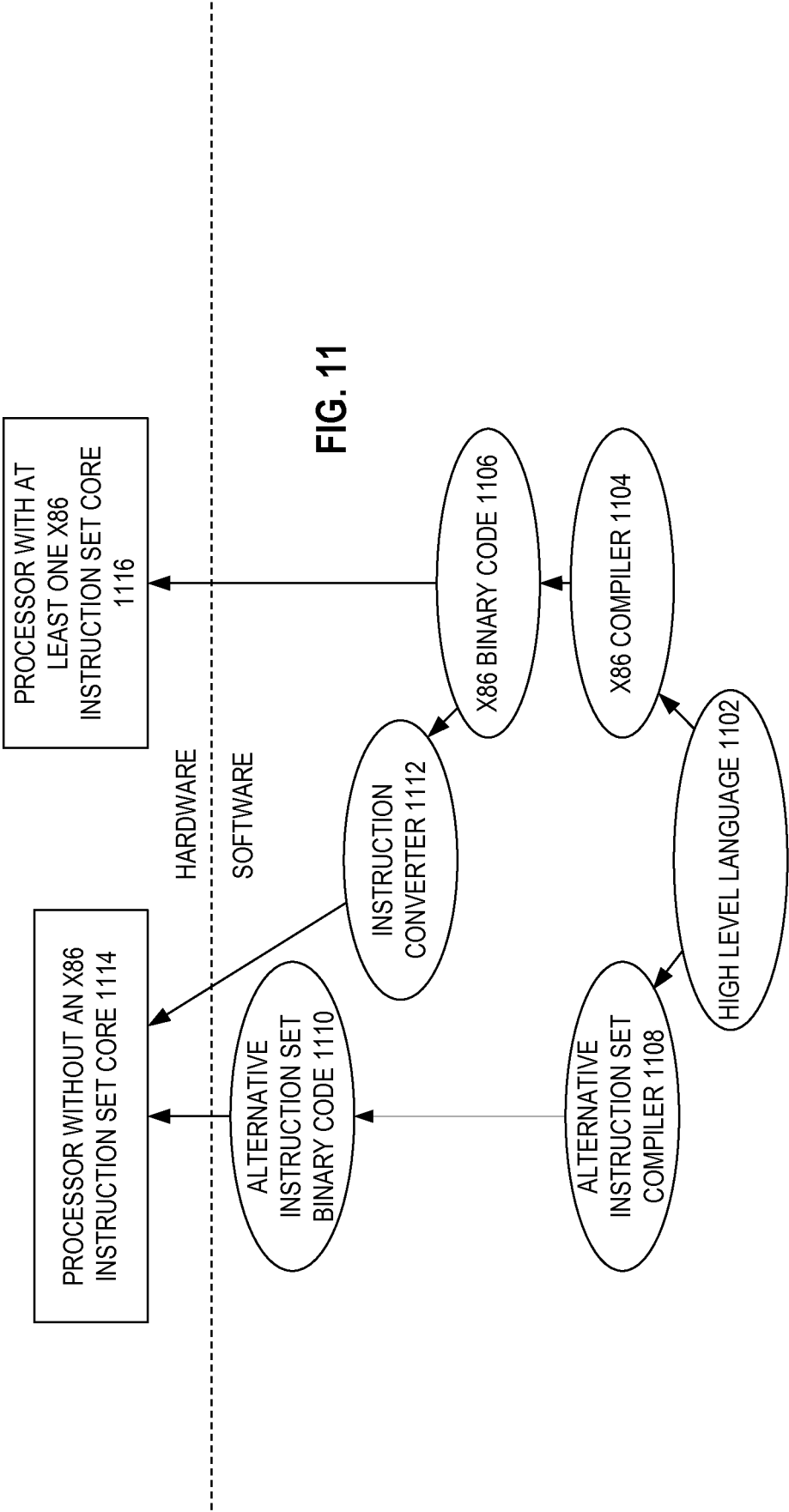


FIG. 10



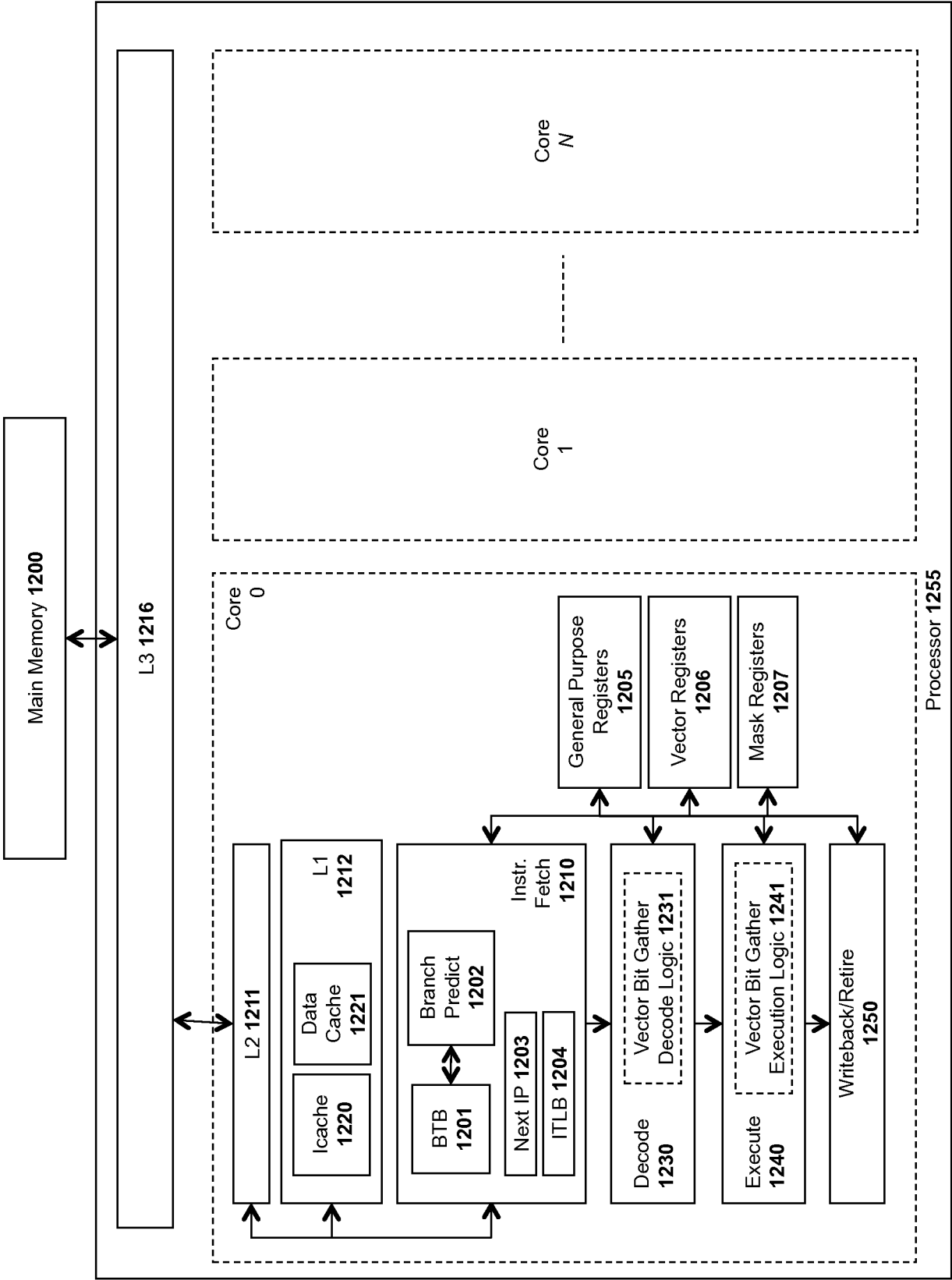


Fig. 12

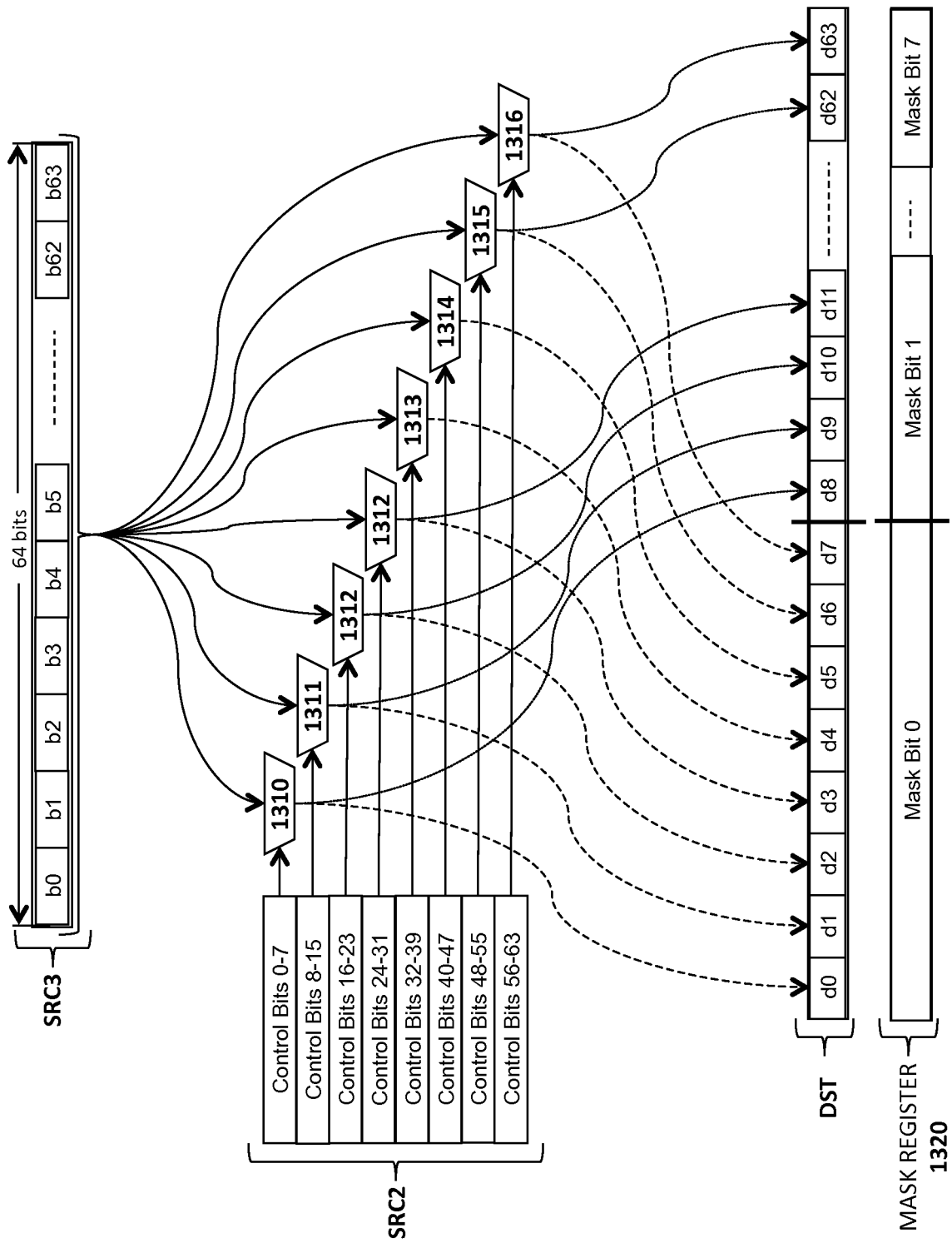
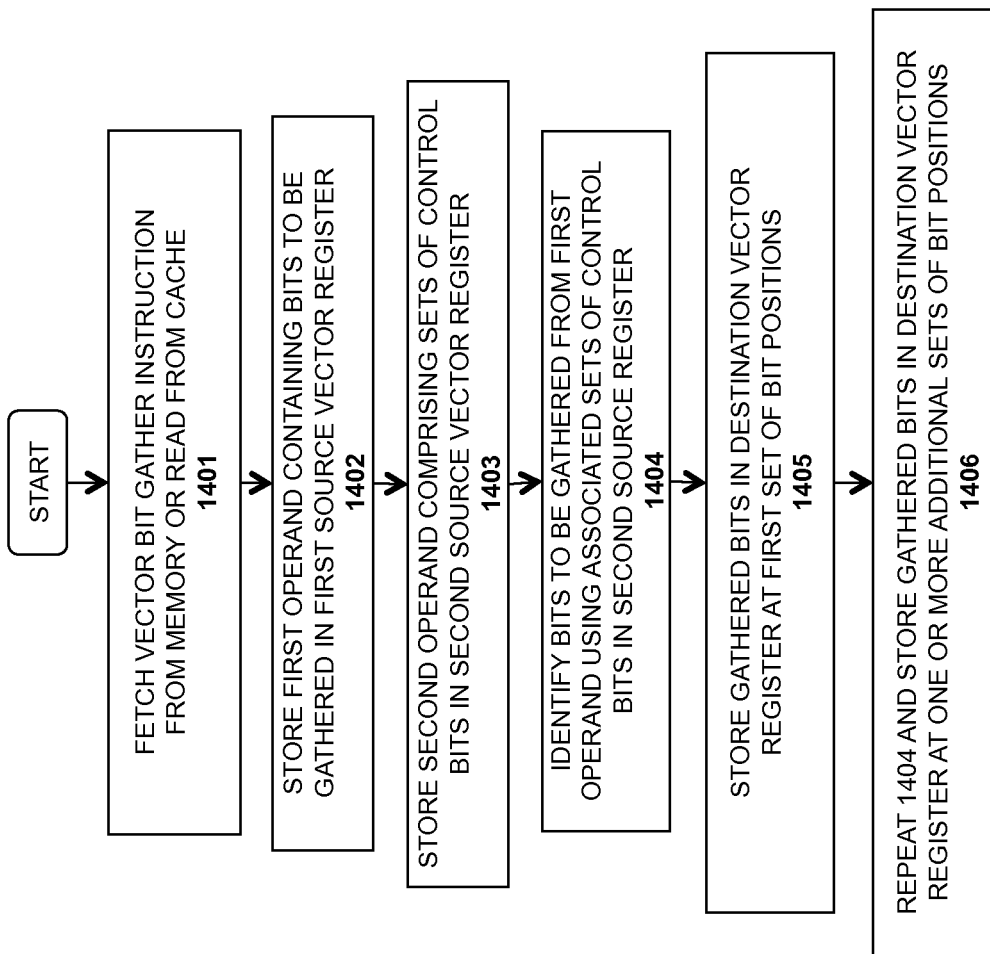


Fig. 13

**Fig. 14**