What is claimed is:

1. A method of fabricating a semiconductor device, comprising:
providing a layer of crystalline silicon on a recipient structure;
forming a metal silicide in a portion of the crystalline silicon adjacent an exposed major surface of the layer of crystalline silicon; and
etching the metal silicide using an etchant selective to the metal silicide relative to the crystalline silicon.

2. The method of claim 1, wherein providing the layer of crystalline silicon on the recipient structure comprises transferring the layer of crystalline silicon from a donor structure to the recipient structure.

3. The method of claim 2, further comprising selecting the layer of crystalline silicon to comprise active device structures.

4. The method of claim 1, wherein forming the metal silicide in the portion of the crystalline silicon adjacent the exposed major surface of the layer of crystalline silicon comprises:
depositing metal over the exposed major surface of the layer of crystalline silicon; and
annealing the deposited metal and the layer of crystalline silicon to form the metal silicide.

5. The method of claim 1, wherein forming the metal silicide in the portion of the crystalline silicon adjacent the exposed major surface of the layer of crystalline silicon comprises implanting metal ions into the crystalline silicon to form the metal silicide.

6. The method of claim 5, further comprising selecting the metal ions to comprise at least one of titanium, nickel, cobalt, and tungsten.

7. The method of claim 1, wherein forming the metal silicide in the portion of the crystalline silicon comprises forming the metal silicide in the portion of the crystalline silicon at a temperature of about 700°C or less.

8. The method of claim 1, wherein etching the metal silicide comprises etching the metal silicide using one or more of a wet etching process, a dry etching process, and an electrochemical etching process.

9. The method of claim 1, wherein etching the metal silicide comprises at least substantially removing the metal silicide and exposing a surface of the crystalline silicon.

10. The method of claim 9, further comprising smoothing a surface of the crystalline silicon using one or more of a wet cleaning process, a chemical-mechanical polishing process, a plasma cleaning process, and an ion trimming process.

11. The method of claim 1, wherein etching the metal silicide comprises etching the metal silicide at a temperature of about one hundred degrees Celsius (100°C) or less.

12. The method of claim 1, wherein etching the metal silicide using the etchant selective to the metal silicide relative to the crystalline silicon comprises etching the metal silicide with HF.

13. The method of claim 1, further comprising forming an SOI type substrate comprising the crystalline silicon, the recipient structure, and a dielectric layer therebetween.

14. The method of claim 1, further comprising forming one or more of an electronic signal processor, a memory device, a light-emitting diode, a laser diode, and a photocell comprising the crystalline silicon.

15. The method of claim 1, further comprising forming the layer of crystalline silicon to have an average layer thickness of about 100 nm or less after etching the metal silicide.

16. The method of claim 1, further comprising providing the exposed major surface of the layer of crystalline silicon with an average surface roughness R_a of about 2.0 nm or less after etching the metal silicide.

CLAIMS

What is claimed is:

1. A method of fabricating a semiconductor device, comprising:

providing a layer of crystalline silicon on a recipient structure; and

after providing the layer of crystalline silicon on the recipient structure, reducing a thickness of the layer of crystalline silicon, reducing the thickness including:

forming a layer consisting essentially of metal silicide in a portion of the crystalline silicon adjacent an exposed major surface of the layer of crystalline silicon, wherein forming the layer consisting essentially of the metal silicide comprises implanting metal ions into the crystalline silicon to form the layer consisting essentially of the metal silicide; and

after forming the layer consisting essentially of the metal silicide, etching the layer consisting essentially of the metal silicide using an etchant selective to the metal silicide relative to the crystalline silicon, the etchant removing the metal silicide at an etch rate higher than any etch rate at which the metal silicide removes the crystalline silicon.

2. The method of claim 1, wherein providing the layer of crystalline silicon on the recipient structure comprises transferring the layer of crystalline silicon from a donor structure to the recipient structure.

3. The method of claim 2, further comprising selecting the layer of crystalline silicon to comprise active device structures.

4. The method of claim 3, further comprising selecting the layer of crystalline silicon to include one or more of PN junctions, transistors, conductive lines, and conductive vias.

5. The method of claim 1, further comprising selecting the crystalline silicon to comprise monocrystalline silicon.

6. A method of fabricating a semiconductor device, comprising:

providing a layer of crystalline silicon on a recipient structure; and

after providing the layer of crystalline silicon on the recipient structure, reducing a thickness of the layer of crystalline silicon, reducing the thickness including:

forming a layer consisting essentially of metal silicide in a portion of the crystalline silicon adjacent an exposed major surface of the layer of crystalline silicon at a temperature of about 700°C. or less, wherein forming the layer consisting essentially of the metal silicide comprises:

depositing metal over the exposed major surface of the layer of crystalline silicon; and

annealing the deposited metal and the layer of crystalline silicon to form the layer consisting essentially of metal silicide; and

after forming the layer consisting essentially of the metal silicide, etching the layer consisting essentially of metal silicide using an etchant selective to the metal silicide relative to the crystalline silicon, the etchant removing the metal silicide at an etch rate higher than any etch rate at which the metal silicide removes the crystalline silicon.

7. The method of claim 1, further comprising selecting the metal ions to comprise at least one of titanium, nickel, cobalt, and tungsten.

8. The method of claim 1, wherein forming the layer consisting essentially of metal silicide in the portion of the crystalline silicon comprises forming the layer consisting essentially of metal silicide in the portion of the crystalline silicon at a temperature of about 700°C. or less.

9. The method of claim 8, wherein forming the layer consisting essentially of metal silicide in the portion of the crystalline silicon at a temperature of about 700°C. or less comprises forming the layer consisting essentially of metal silicide in the portion of the crystalline silicon at a temperature of about 500°C. or less.

10. The method of claim 9, wherein forming the layer consisting essentially of metal silicide in the portion of the crystalline silicon at a temperature of about 500°C. or less comprises forming the layer consisting essentially of metal silicide in the portion of the crystalline silicon at a temperature of about 300°C. or less.

11. The method of claim 1, wherein etching the layer consisting essentially of metal silicide comprises etching the layer consisting essentially of metal silicide using one or more of a wet etching process, a dry etching process, and an electrochemical etching process.

12. The method of claim 1, wherein etching the layer consisting essentially of metal silicide comprises at least substantially removing the layer consisting essentially of metal silicide and exposing a surface of the crystalline silicon.

13. The method of claim 12, further comprising smoothing a surface of the crystalline silicon using one or more of a wet cleaning process, a chemical-mechanical polishing process, a plasma cleaning process, and an ion trimming process.

14. The method of claim 1, wherein etching the layer consisting essentially of metal silicide comprises etching the layer consisting essentially of metal silicide at a temperature of about one hundred degrees Celsius (100°C.) or less.

15. The method of claim 1, wherein etching the layer consisting essentially of metal silicide at the temperature of about one hundred degrees Celsius (100°C.) or less comprises etching the layer consisting essentially of metal silicide at a temperature of about twenty-five degrees Celsius (25°C.) or less.

16. The method of claim 1, wherein etching the layer consisting essentially of metal silicide using the etchant selective to the metal silicide relative to the crystalline silicon comprises etching the metal silicide with HF.

17. The method of claim 1, further comprising forming an SOI type substrate comprising the crystalline silicon, the recipient structure, and a dielectric layer therebetween.

18. The method of claim 1, further comprising forming one or more of an electronic signal processor, a memory device, a light-emitting diode, a laser diode, and a photocell comprising the crystalline silicon.

19. The method of claim 1, further comprising forming the layer of crystalline silicon to have an average layer thickness of about 500 nm or less after etching the layer consisting essentially of metal silicide.

20. The method of claim 19, further comprising forming the layer of crystalline silicon to have an average layer thickness of about 100 nm or less after etching the layer consisting essentially of metal silicide.

21. The method of claim 1, further comprising providing an exposed major surface of the layer of crystalline silicon with an average surface roughness R_a of about 5.0 nm or less after etching the metal silicide.

22. The method of claim 21, further comprising providing the exposed major surface of the layer of crystalline silicon with an average surface roughness R_a of about 2.0 nm or less after etching the layer consisting essentially of metal silicide.

23. A method of forming a silicon-on-insulator (SOI) substrate, comprising:

providing a layer of crystalline silicon over a base substrate with a dielectric material between the layer of crystalline silicon and the base substrate; and

after providing the layer of crystalline silicon, thinning the layer of crystalline silicon to a thickness of about 500 nm or less, thinning the layer of crystalline silicon comprising:

forming a generally planar metal silicide layer in a portion of the layer of crystalline silicon adjacent an exposed major surface of the layer of crystalline silicon; and

etching the generally planar metal silicide layer using an etchant selective to the metal silicide layer relative to the crystalline silicon, the etchant removing the metal silicide at an etch rate higher than any etch rate at which the metal silicide removes the crystalline silicon.

24. The method of claim 23, wherein forming the generally planar metal silicide layer in the portion of the crystalline silicon adjacent the exposed major surface of the layer of crystalline silicon comprises:

depositing metal over the exposed major surface of the layer of crystalline silicon; and

annealing the deposited metal and the layer of crystalline silicon to form the generally planar metal silicide layer.

25. The method of claim 23, wherein forming the generally planar metal silicide layer in the portion of the crystalline silicon adjacent the exposed major surface of the layer of crystalline silicon comprises implanting metal ions into the crystalline silicon to form the generally planar metal silicide layer.

26. The method of claim 25, further comprising selecting the metal ions to comprise at least one of titanium, nickel, cobalt, and tungsten.

27. The method of claim 23, wherein forming the generally planar metal silicide layer in the portion of the crystalline silicon comprises forming the generally planar metal silicide layer in the portion of the crystalline silicon at a temperature of about 700°C. or less.

28. The method of claim 27, wherein forming the generally planar metal silicide layer in the portion of the crystalline silicon at a temperature of about 700°C. or less comprises forming the generally planar metal silicide layer in the portion of the crystalline silicon at a temperature of about 500°C. or less.

29. The method of claim 28, wherein forming the generally planar metal silicide layer in the portion of the crystalline silicon at a temperature of about 500°C. or less comprises forming the generally planar metal silicide layer in the portion of the crystalline silicon at a temperature of about 300°C. or less.

30. The method of claim 23, wherein etching the generally planar metal silicide layer comprises etching the metal silicide at a temperature of about one hundred degrees Celsius (100°C.) or less.

31. The method of claim 30, wherein etching the generally planar metal silicide layer at the temperature of about one hundred degrees Celsius (100°C.) or less comprises etching the generally planar metal silicide layer at a temperature of about twenty-five degrees Celsius (25°C.) or less.

32. The method of claim 23, further comprising forming the layer of crystalline silicon to have an average layer thickness of about 100 nm or less after etching the generally planar metal silicide layer.

33. The method of claim 23, further comprising providing an exposed major surface of the layer of crystalline silicon with an average surface roughness R_a of about 5.0 nm or less after etching the generally planar metal silicide layer.

34. The method of claim 33, further comprising providing the exposed major surface of the layer of crystalline silicon with an average surface roughness R_a of about 2.0 nm or less after etching the generally planar metal silicide layer.

35. The method of claim 1, further comprising selecting the crystalline silicon to comprise a single crystal of silicon.