

ABSTRACT OF THE DISCLOSURE

Provided is a nonvolatile memory including a clock pin configured to receive an external clock signal during a duty correction circuit training period; a plurality of memory chips configured to perform a duty correction operation on an internal clock signal based on the external clock signal, the plurality of memory chips configured to perform the duty correction operation in parallel during the training period; and an input/output pin commonly connected to the plurality of memory chips, wherein each of the plurality of memory chips includes: a duty correction circuit (DCC) configured to perform the duty correction operation on the internal clock signal; and an output buffer connected between an output terminal of the DCC and the input/output pin.

FIG. 8