FIG. 1

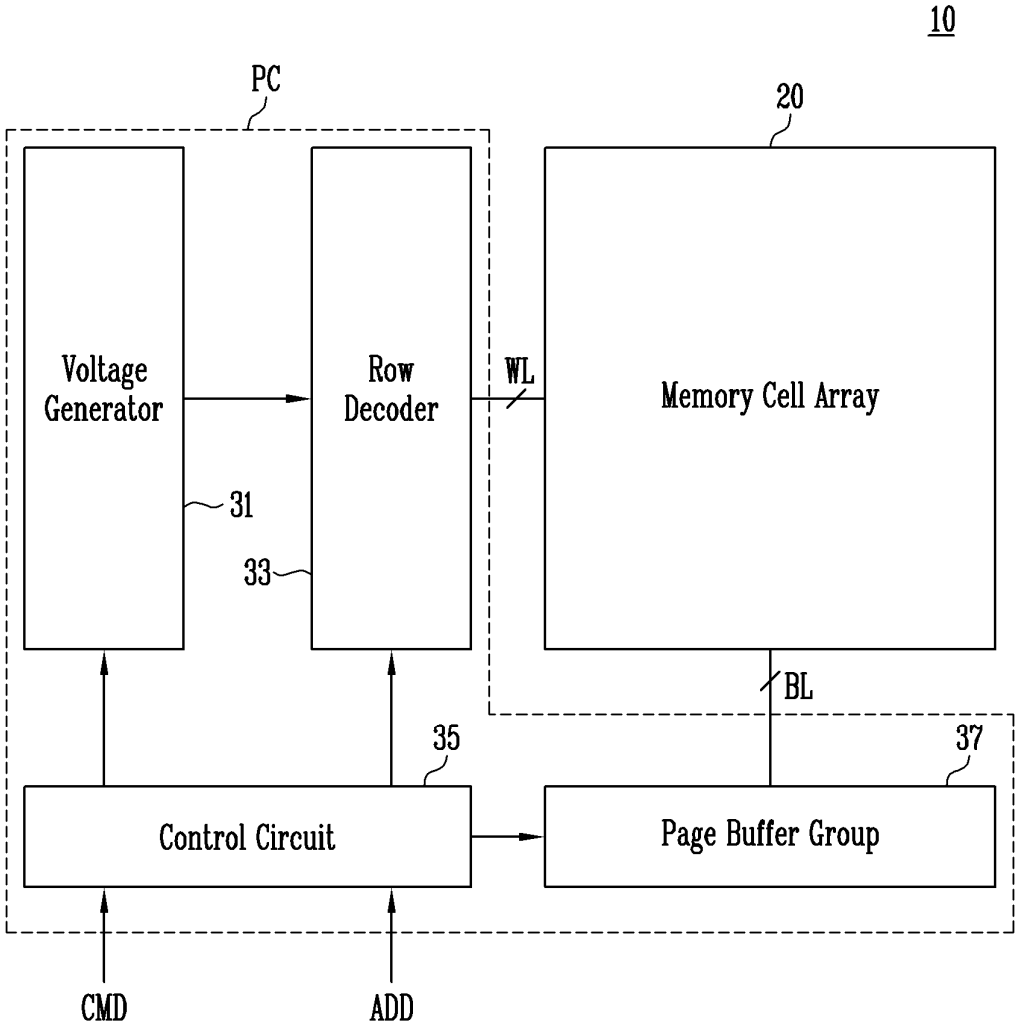

10
PC
20
Voltage Generator
Row Decoder
WL
Memory Cell Array
31
33
BL
35
37
Control Circuit
Page Buffer Group
CMD
ADD

FIG. 2

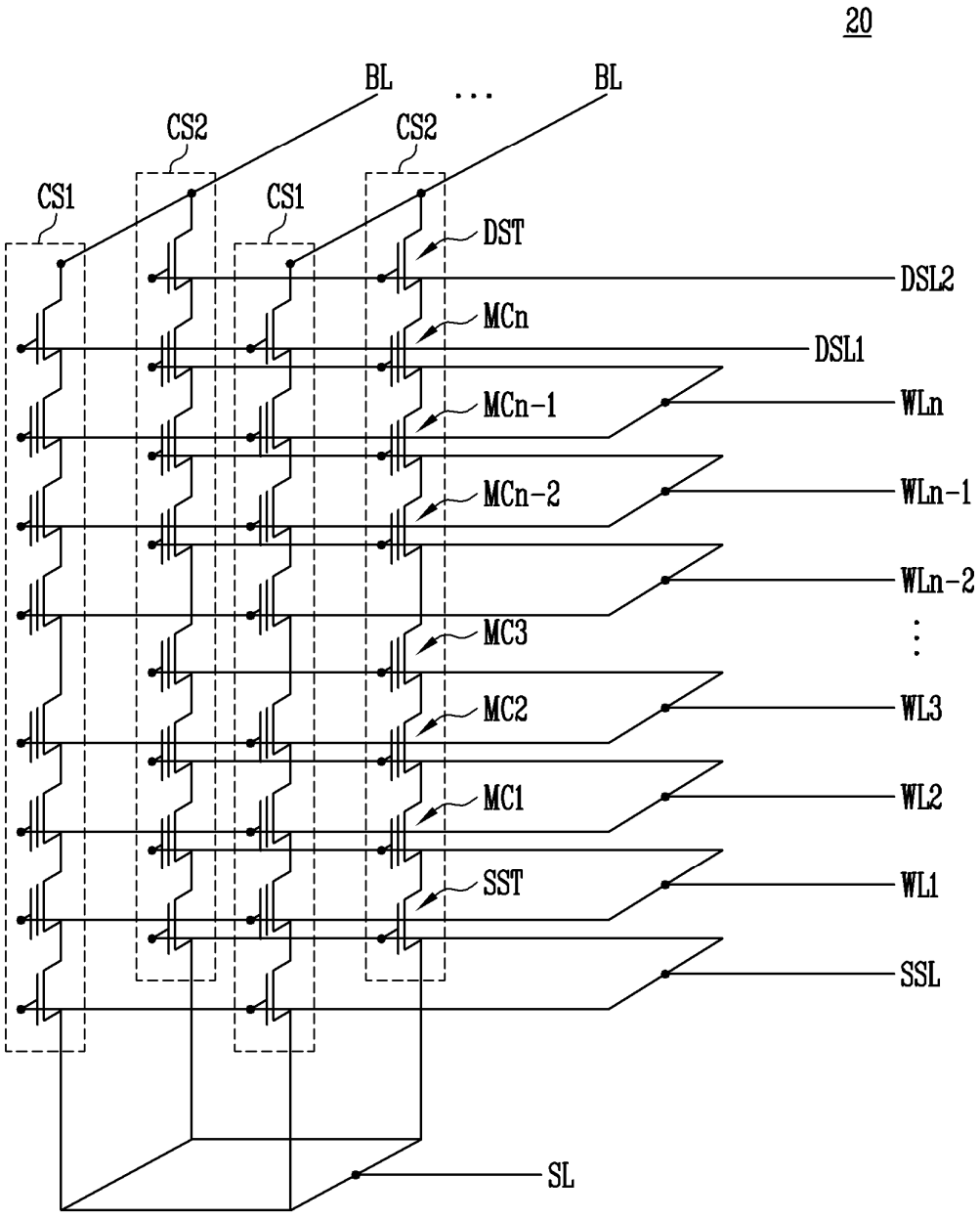

20
BL
BL
CS2
CS2
CS1
CS1
DST
DSL2
MCn
DSL1
MCn-1
WLn
MCn-2
WLn-1
WLn-2
MC3
MC2
WL3
MC1
WL2
SST
WL1
SSL
SL

FIG. 3

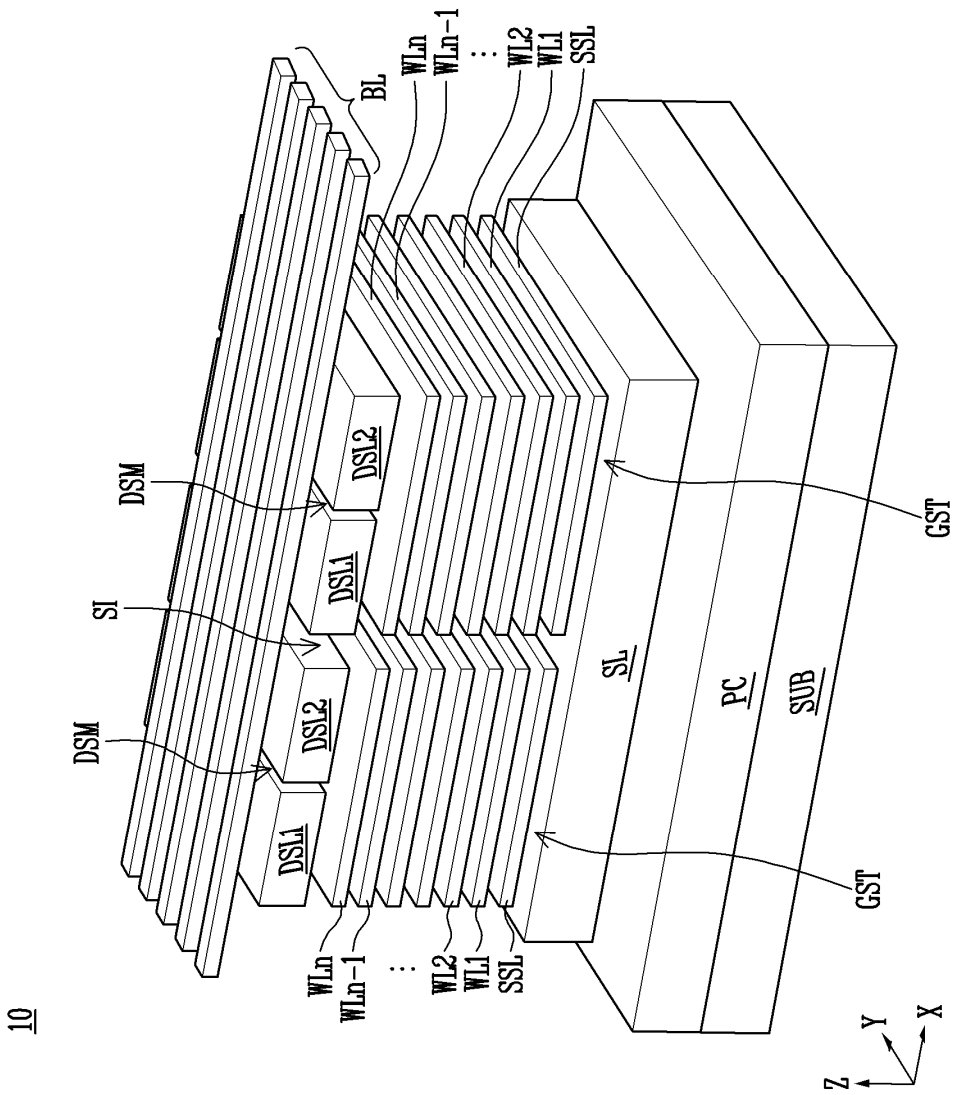


FIG. 4

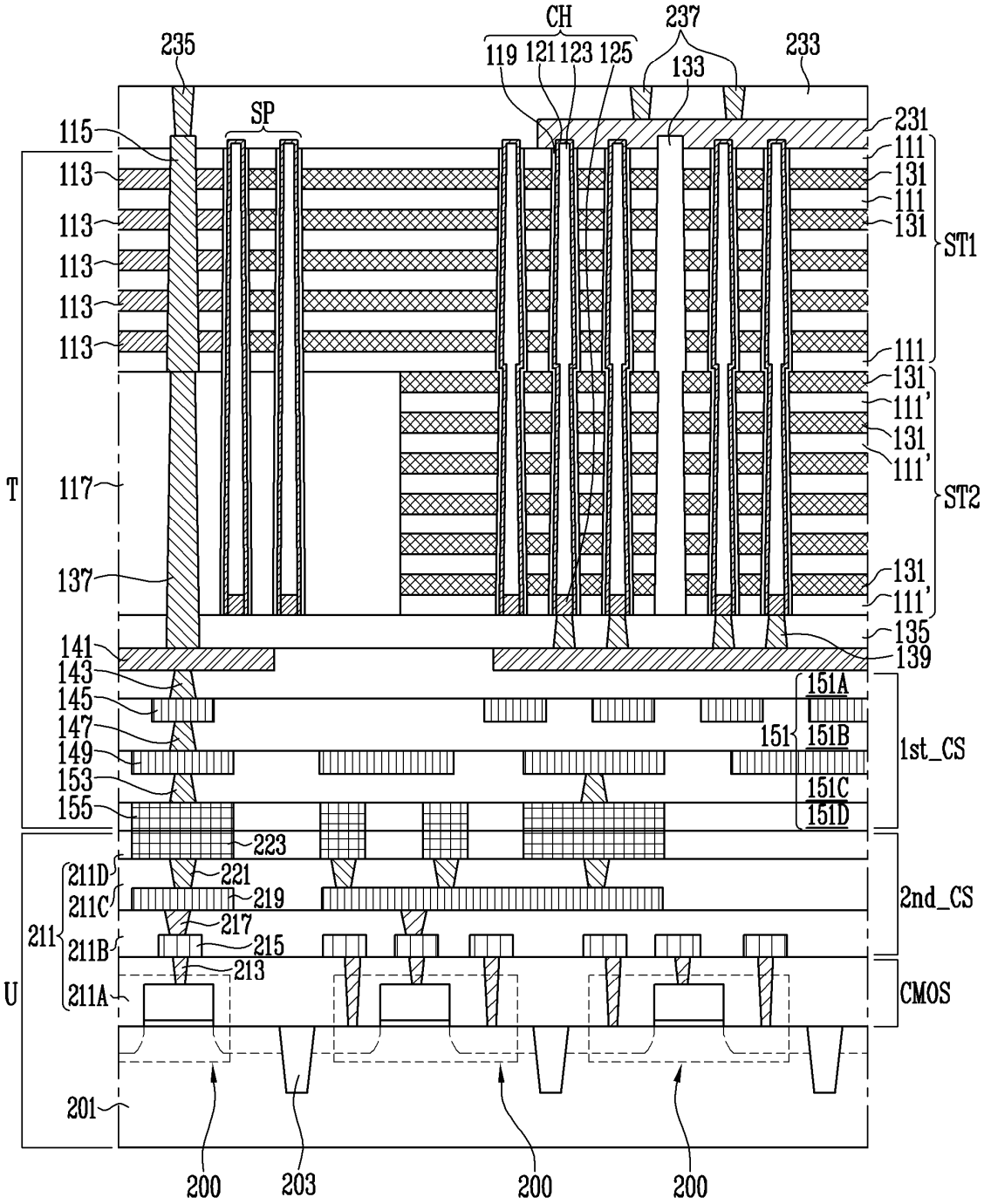

CH
237
235
119 121 123 125
133
233
SP
115
231
111
113
131
111
131
113
ST1
113
113
113
111
131'
111'
131'
111'
T
117
ST2
137
131'
111'
135
141
139
143
151A
145
151
151B
147
1st_CS
149
153
151C
155
151D
223
211D
221
211C
219
2nd_CS
217
211
211B
215
213
U
211A
CMOS
201
200
203
200
200

FIG. 5A

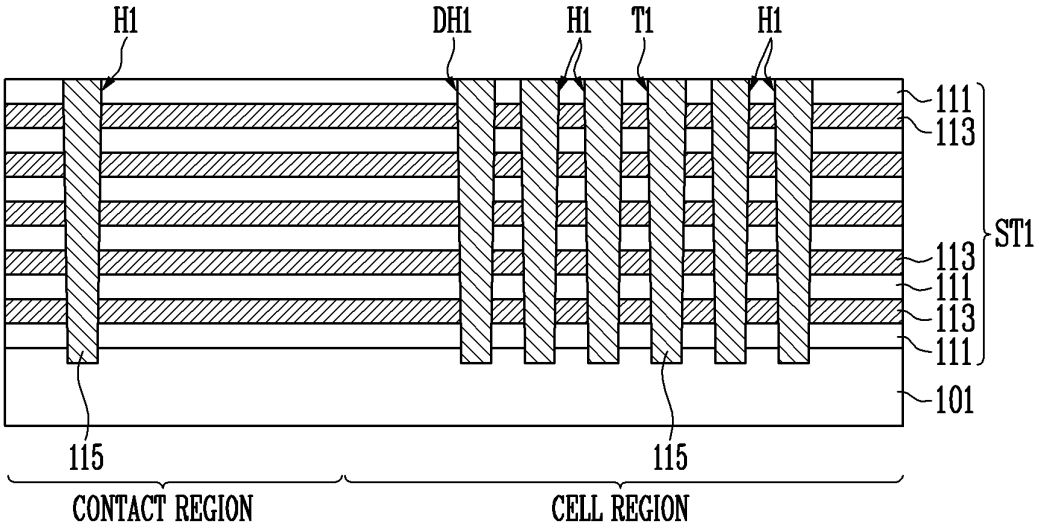

H1
DH1
H1
T1
H1
111
113
ST1
113
111
113
111
101
115
115
CONTACT REGION
CELL REGION

FIG. 5B

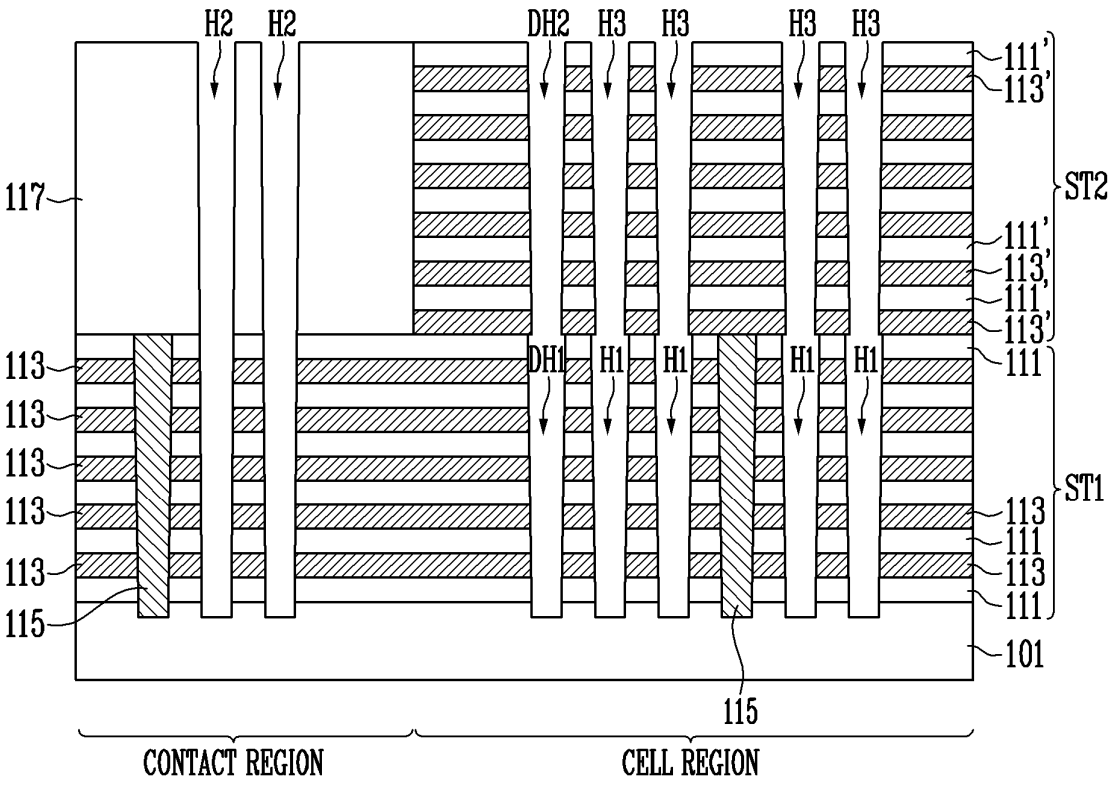

H2
H2
DH2
H3
H3
H3
H3
111'
113'
ST2
117
111'
113'
111'
113'
113
113
113
113
113
115
DH1
H1
H1
H1
H1
111
ST1
113
111
113
111
101
115
CONTACT REGION
CELL REGION

FIG. 5C

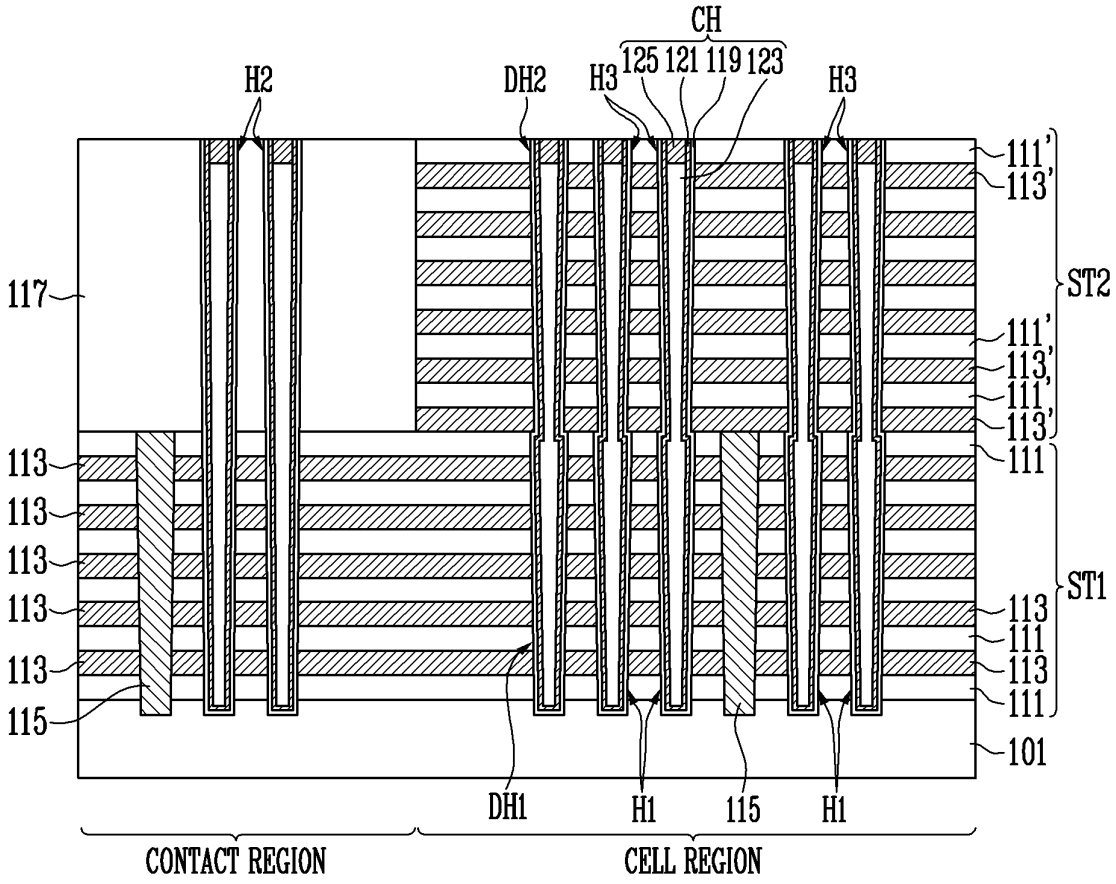

CH
125 121 119 123
H2
DH2
H3
H3
111'
113'
ST2
117
111'
113'
111'
113'
111
113
113
113
113
113
ST1
113
111
113
111
115
101
DH1
H1
115
H1
CONTACT REGION
CELL REGION

FIG. 5D

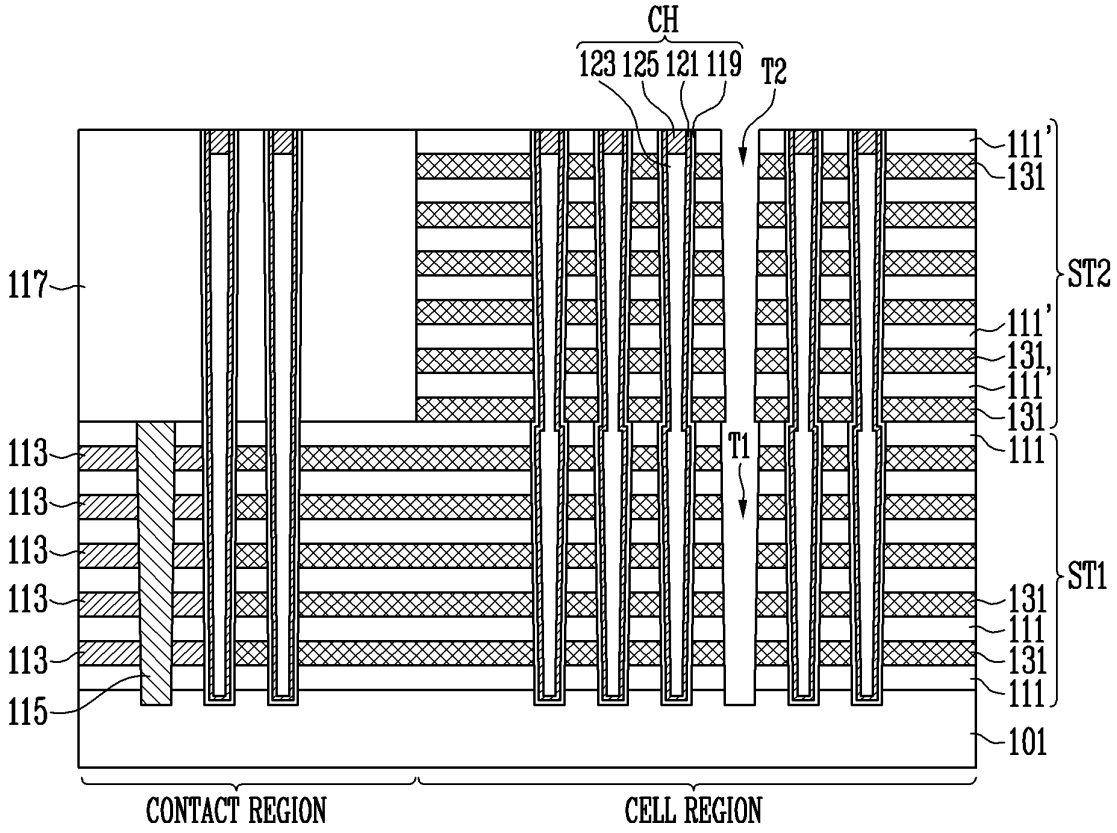

CH
123 125 121 119
T2
111'
131
ST2
117
111'
131,
111
131
113
T1
111
113
113
ST1
113
131
111
113
131
115
111
101
CONTACT REGION
CELL REGION

FIG. 5E

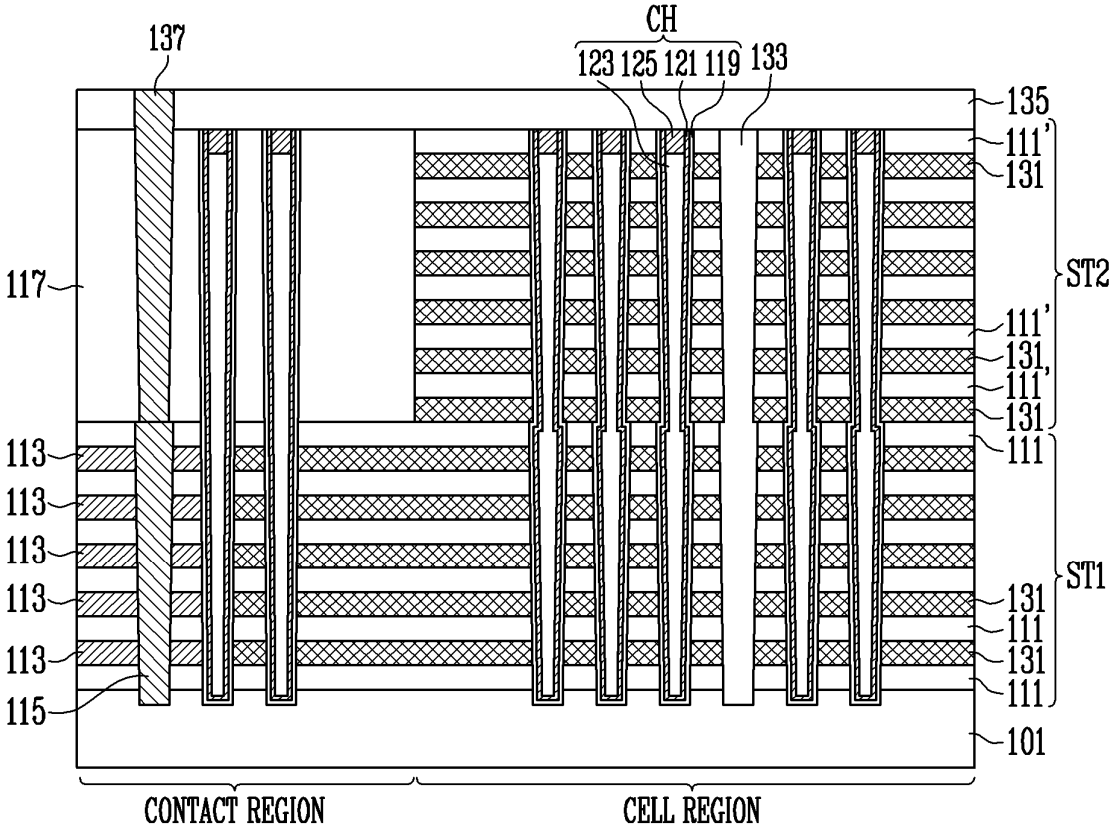

137
CH
123 125 121 119
133
135
111'
131
117
ST2
111'
131
111'
131
113
111
113
113
ST1
113
131
111
113
131
115
111
101
CONTACT REGION
CELL REGION

FIG. 5F

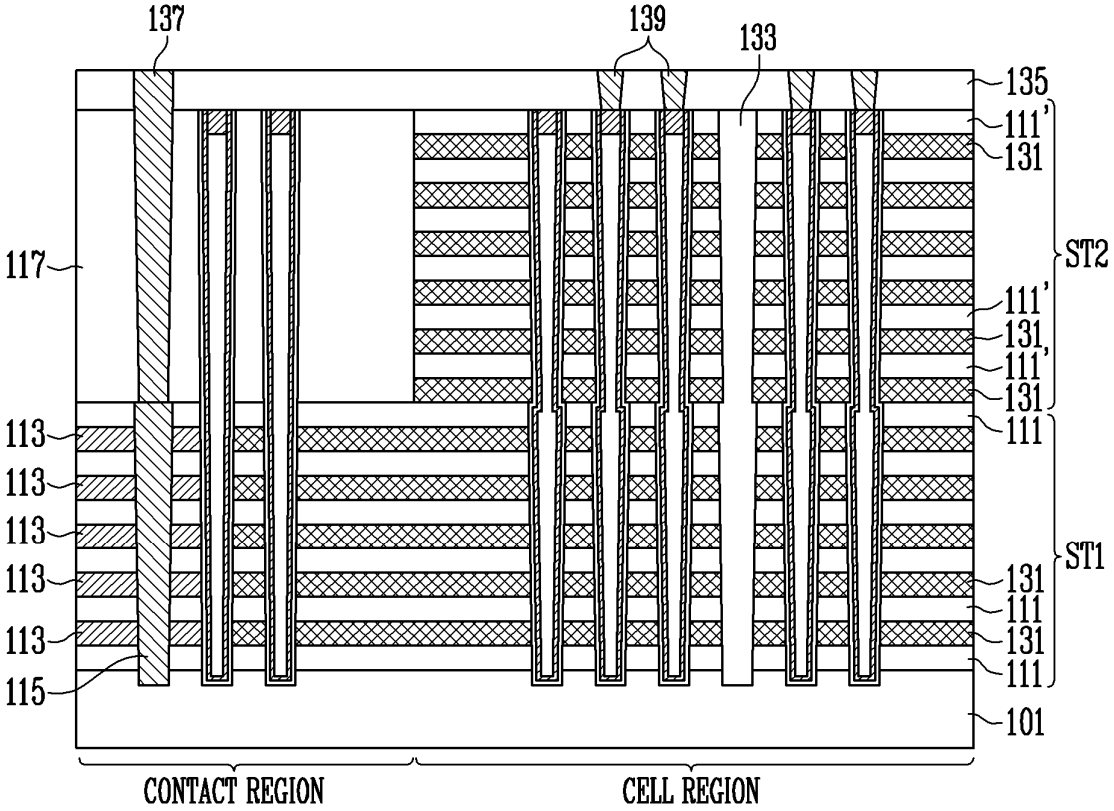

137
139
133
135
111'
131
117
ST2
111'
131,
111'
131
113
113
113
113
113
115
111
ST1
131
111
131
111
101
CONTACT REGION
CELL REGION

FIG. 5G

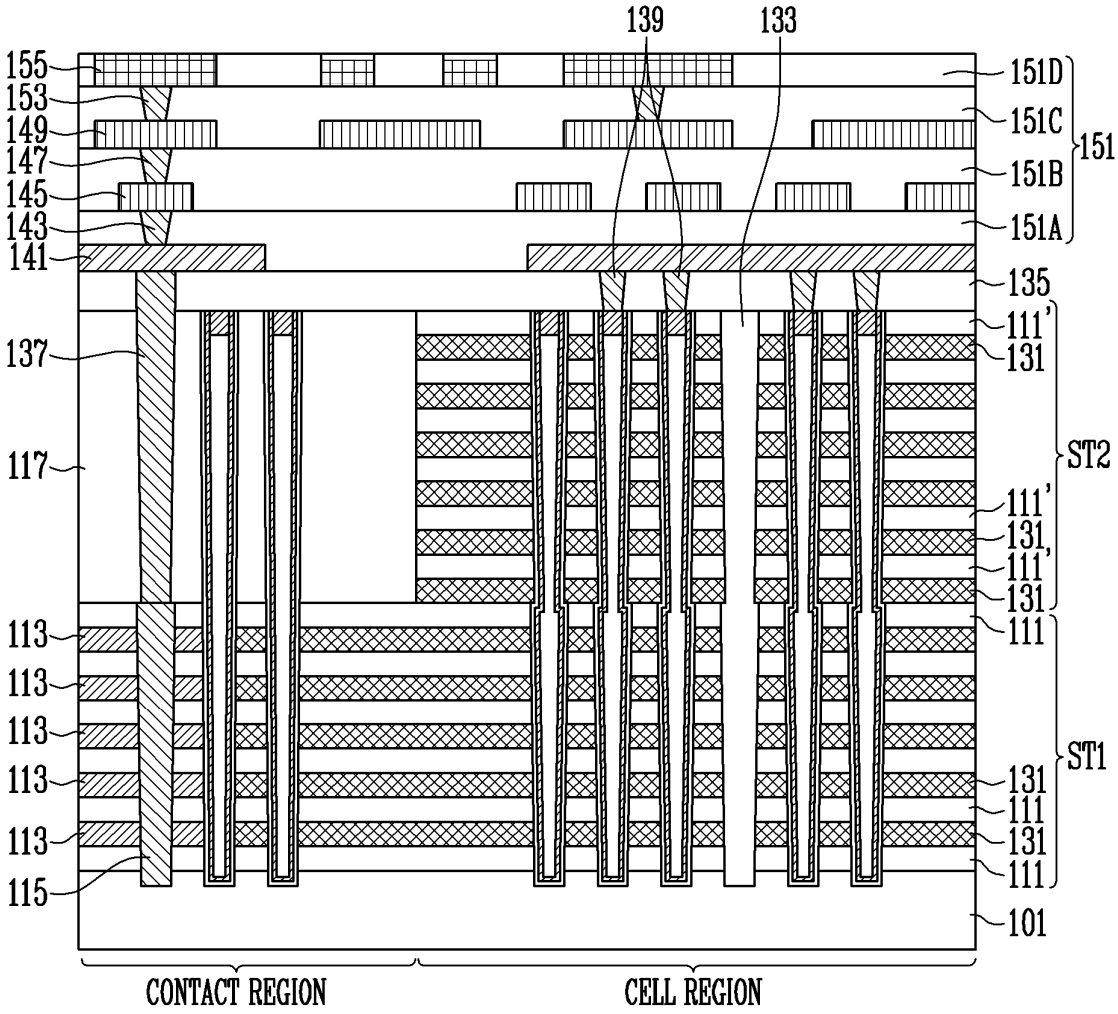

139
133
155
153
149
147
145
143
141
137
117
113
113
113
113
113
115
151D
151C
151B
151A
151
135
111'
131
ST2
111'
131,
111'
131
111
131
111
131
111
131
ST1
101
CONTACT REGION
CELL REGION

FIG. 6

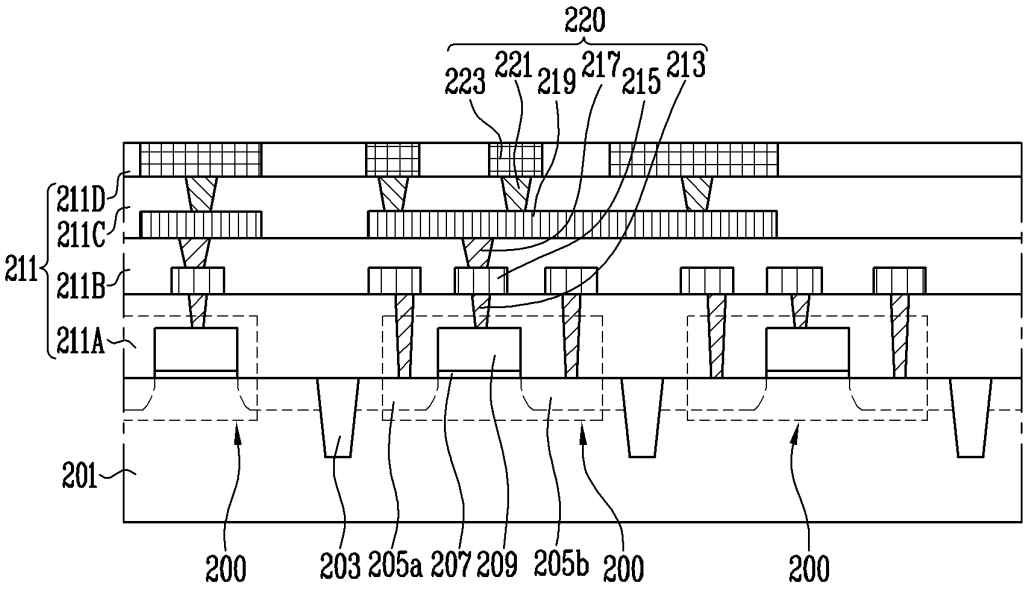

220
223
221
219
217
215
213
211D
211C
211
211B
211A
201
200
203
205a
207
209
205b
200
200

FIG. 7

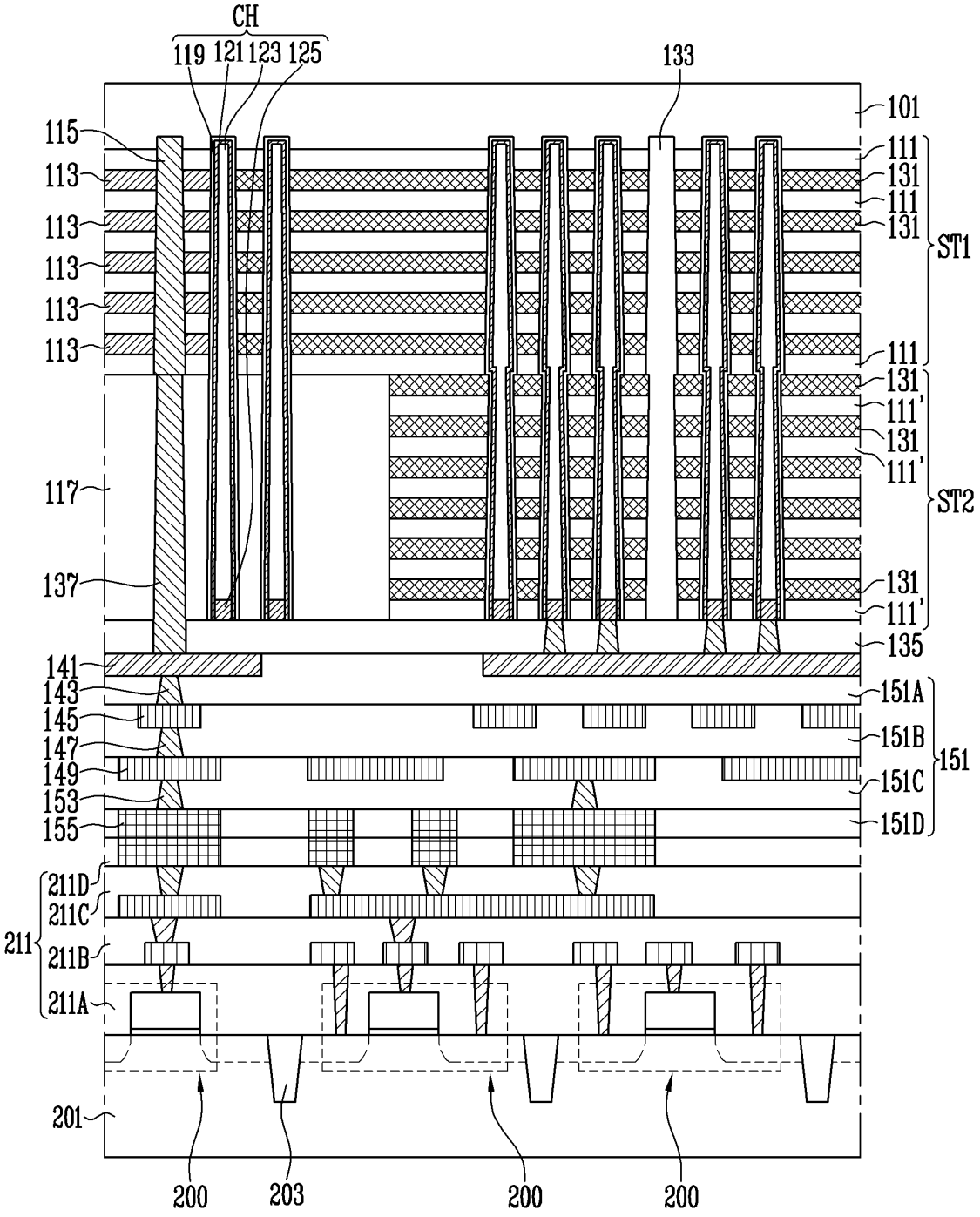

CH
119
121
123
125
133
101
115
113
113
113
113
113
111
131
111
131
111
131
ST1
117
137
131
111'
131
111'
131
111'
ST2
135
141
143
145
147
149
153
155
151A
151B
151C
151D
151
211D
211C
211
211B
211A
201
200
203
200
200

FIG. 8A

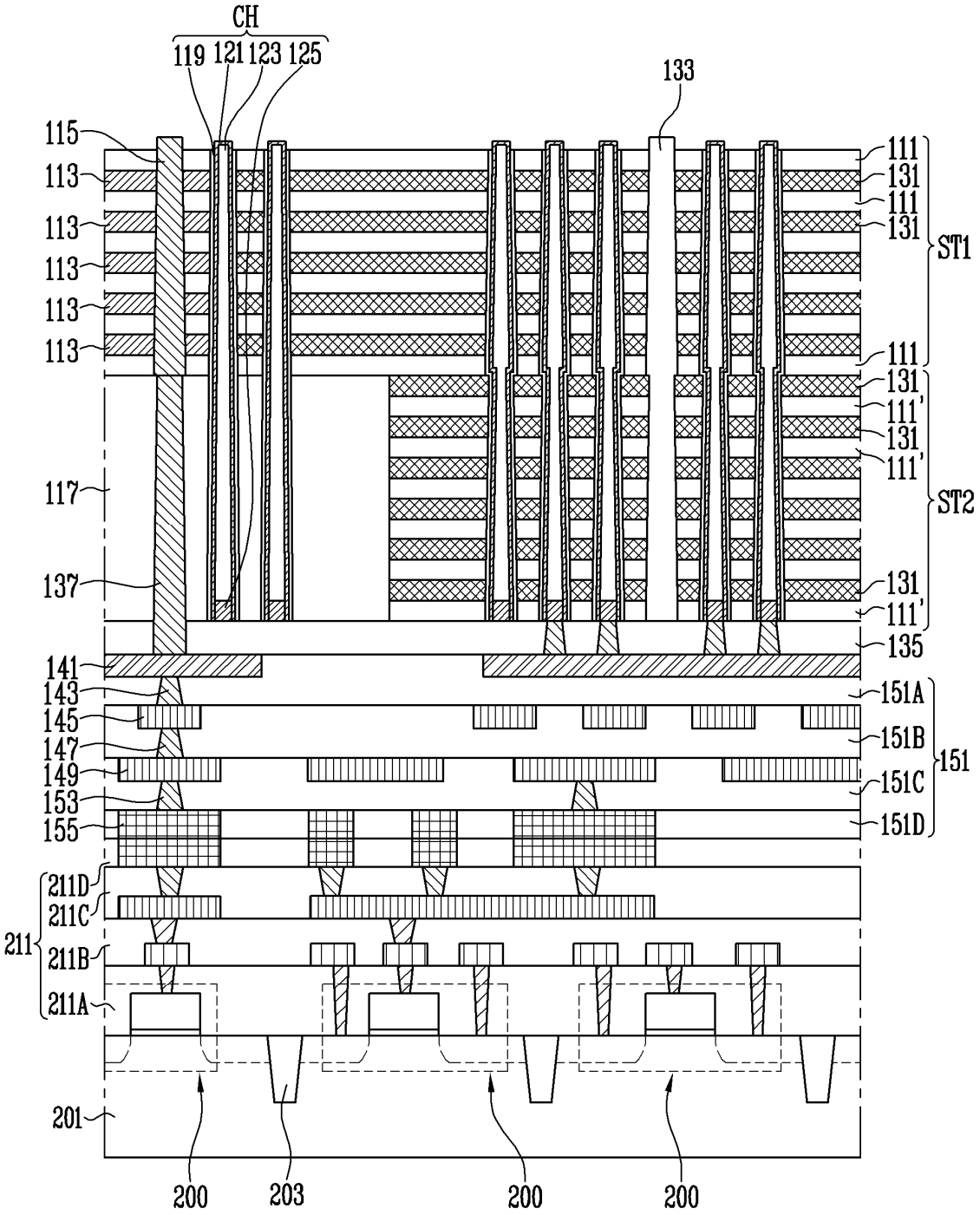

CH
119
121
123
125
133
115
113
113
113
113
113
117
137
141
143
145
147
149
153
155
211D
211C
211
211B
211A
201
200
203
200
200
111
131
111
131
ST1
111
131
111'
131
111'
ST2
131
111'
135
151A
151B
151
151C
151D

FIG. 8B

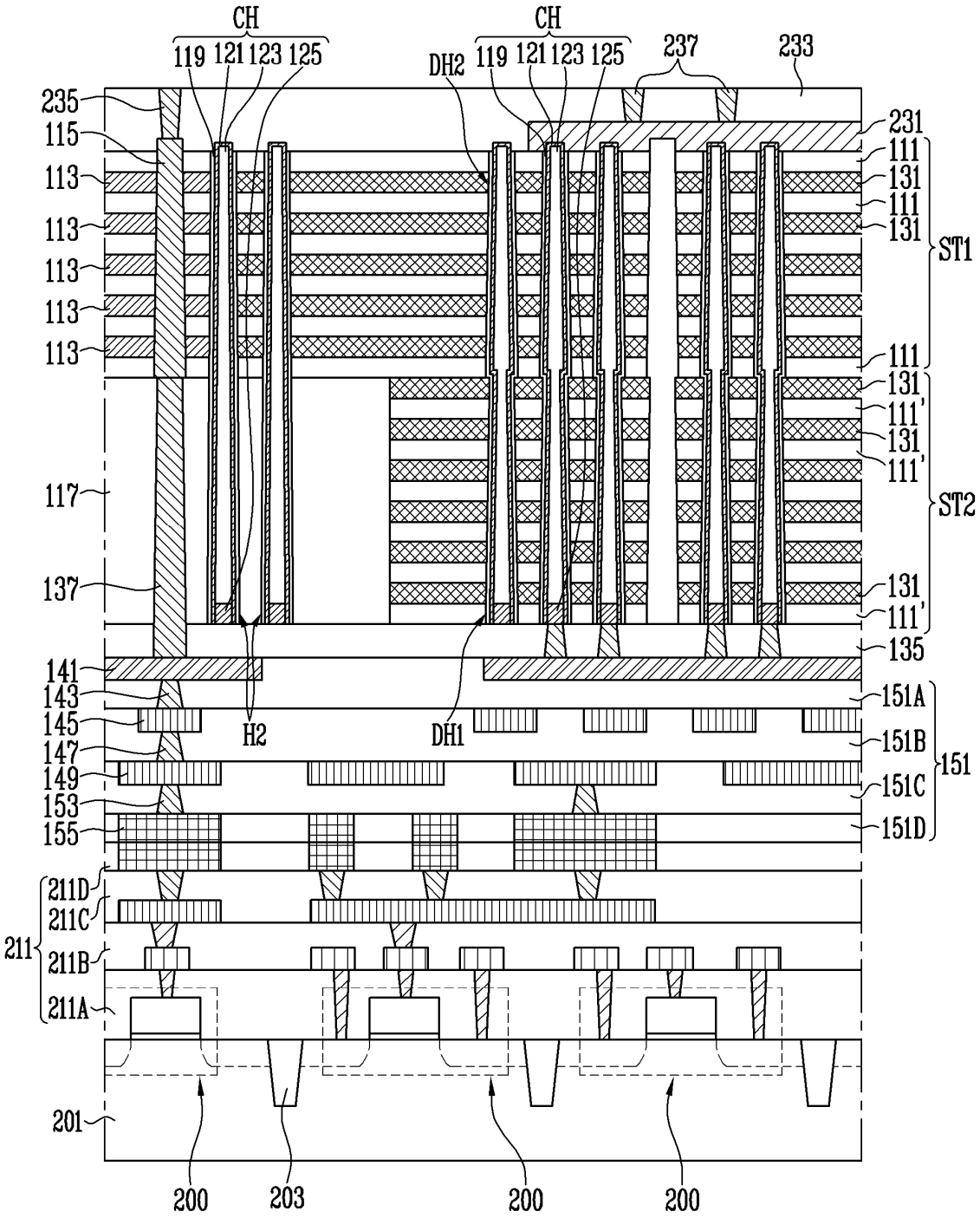

CH
119 121 123 125
CH
DH2 119 121 123 125
237
233
235
115
113
113
113
113
113
231
111
131
111
131
ST1
111
131
111'
131
111'
ST2
117
137
131
111'
135
141
143
145
147
149
153
155
H2
DH1
151A
151B
151C
151D
151
211D
211C
211
211B
211A
201
200
203
200
200

FIG. 9

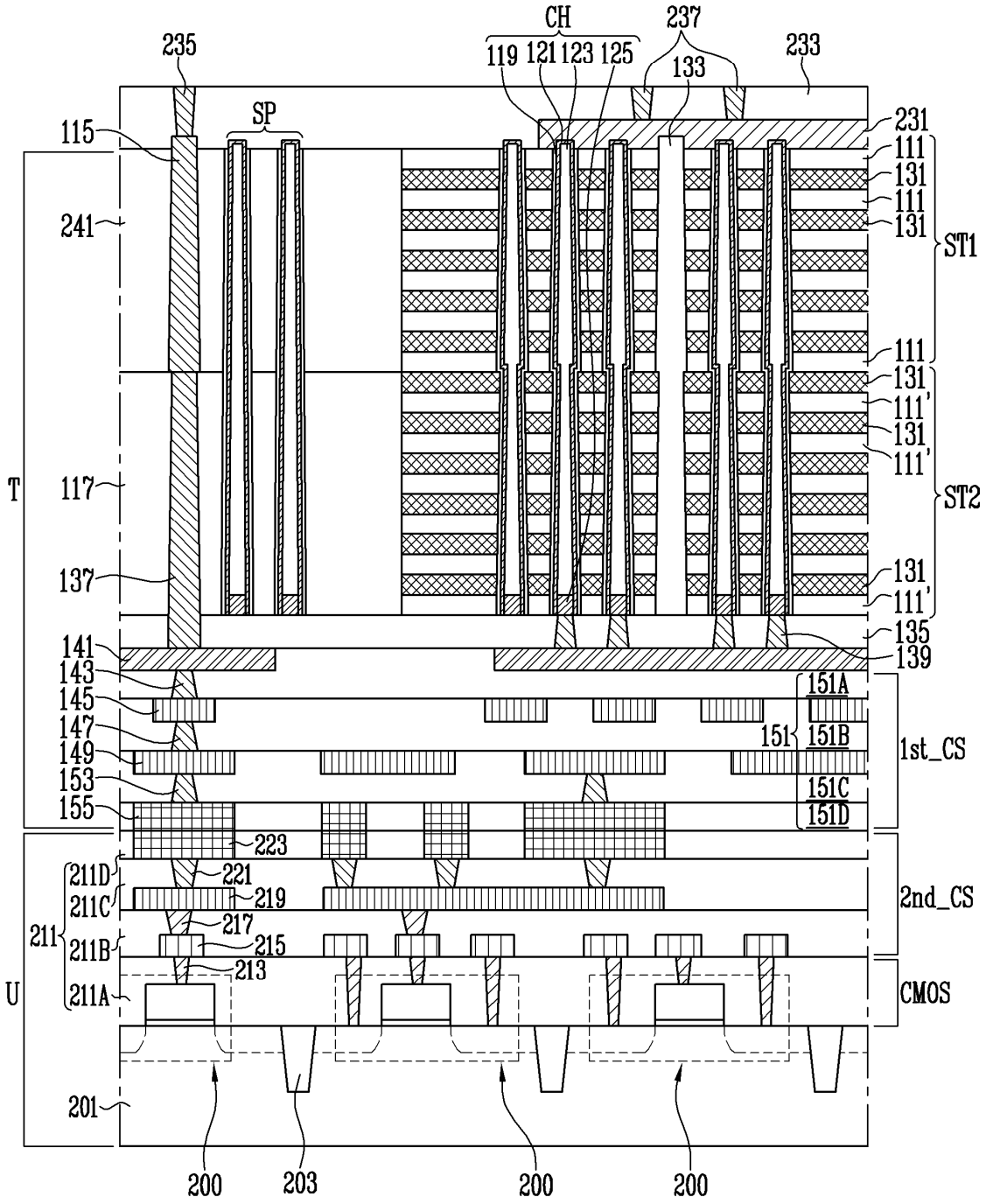

CH
237
235
119 121 123 125
133
233
SP
115
231
111
131
111
131
241
ST1
111
131'
111'
131
111'
T
117
ST2
137
131'
111'
135
141
139
143
151A
145
151
151B
147
1st_CS
149
153
151C
155
151D
223
211D
221
211C
219
2nd_CS
211
217
211B
215
213
U
211A
CMOS
201
200
203
200
200

FIG. 10

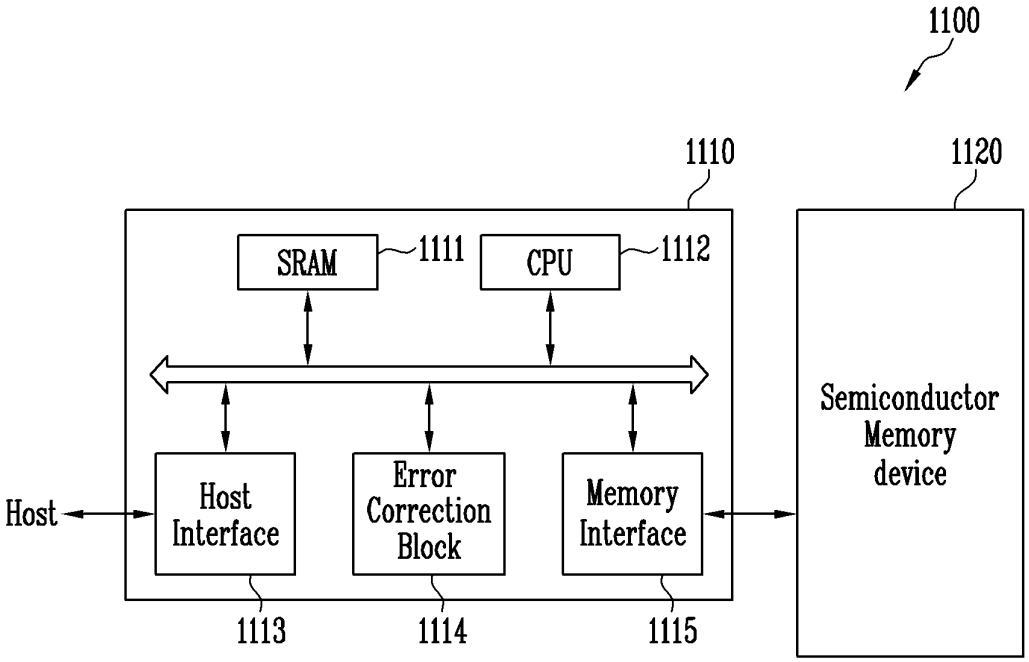
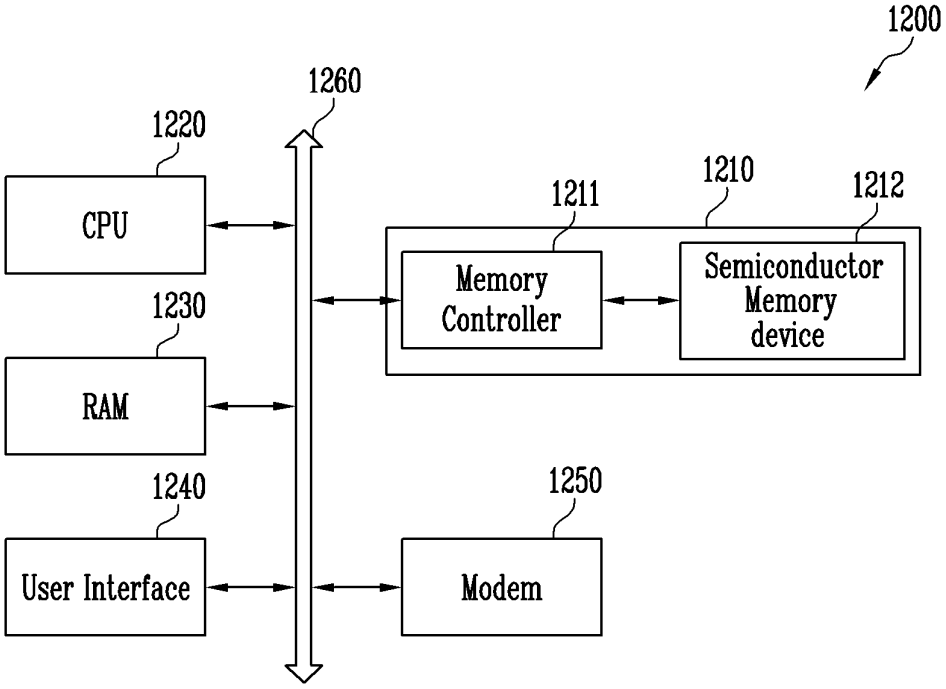

1100
1110
1120
SRAM
1111
CPU
1112
Host
Host Interface
Error Correction Block
Memory Interface
Semiconductor Memory device
1113
1114
1115

FIG. 11


1200
1260
1220
CPU
1230
RAM
1240
User Interface
1211
1210
1212
Memory Controller
Semiconductor Memory device
1250
Modem