What is claimed :

1. A processor comprising:

a vector register file comprising a multi-port memory, and

a plurality of tiles configured to process an N by N matrix of data elements and an N by 1 vector of data elements, wherein N is an integer equal to or greater than 8, and wherein each of the plurality of tiles is configured to process N data elements, and wherein the vector register file is configured to:

in response to a write instruction, during a single clock cycle store N data elements in the multi -port memory and during each one of out of P clock cycles provide N data elements to each one of P input interface circuits of the multi-port memory, wherein P is an integer equal to N divided by L, wherein L is an integer equal to or greater than 2, and wherein each of the P input interface circuits comprises an input lane configured to carry L data elements in parallel, and wherein during the each one of the P clock cycles the multi-port memory is configured to receive N data elements via a selected at least one of the P input interface circuits, and

in response to a read instruction, during a single clock cycle retrieve N data elements from the multi-port memory and during each one of out of Q clock cycles provide L data elements from each one of Q output interface circuits of the multi-port memory, wherein Q is an integer equal to N divided by L, and wherein each of the Q output interface circuits comprises an output lane configured to carry L data elements in parallel, and wherein during the each one of the Q clock cycles the multi-port memory is configured to provide N data elements to a selected at least one of the Q output interface circuits.

2. The processor of claim 1, wherein the multi-port memory is a dual-port memory, and wherein the dual-port memory comprises a single read port and a single write port.

3. The processor of claim 1, wherein the read instruction is scheduled to execute simultaneously with the write instruction.

4. The processor of claim 1, wherein each one of the P input interface circuits comprises an input buffer configured to store N by 1 vectors.

5. The processor of claim 1, wherein each one of the Q output interface circuits comprises an output buffer configured to store N by 1 vectors.

6. The processor of claim 4, wherein each of the P input interface circuits comprises at least one shift register coupled to receive the N by 1 vectors from the input buffer.

7. The processor of claim 5, wherein each of the Q output interface circuits comprises at least one shift register coupled to provide the N by 1 vectors to the output buffer.

8. A method in a system comprising a plurality of tiles and a vector register file comprising a dual-port memory, wherein each of the plurality of tiles is configured to process an N by N matrix of data elements and an N by 1 vector of data elements, wherein N is an integer equal to or greater than 8, and wherein each of the plurality of tiles is configured to process N data elements, the method comprising:

in response to a write instruction, during a single clock cycle storing N data elements in the dual-port memory and during each one of out of P clock cycles providing N data elements to each one of P input interface circuits of the dual-port memory, wherein P is an integer equal to N divided by L, wherein L is an integer equal to or greater than 2, and wherein each of the P input interface circuits comprises an input lane configured to carry L data elements in parallel, and wherein during the each one of the P clock cycles the dual-port memory is configured to receive N data elements via a selected one of the P input interface circuits; and

in response to a read instruction, during a single clock cycle retrieving N data elements from the dual-port memory and during each one of out of Q clock cycles providing L data elements from each one of Q output interface circuits of the dual-port memory, wherein Q is an integer equal to N divided by L, and wherein each of the Q output interface circuits comprises an output lane configured to carry L data elements in parallel, and wherein during the each one of the Q clock cycles the dual-port memory is configured to provide N data elements to a selected one of the Q output interface circuits.

9. The method of claim 8, wherein the dual-port memory comprises a single read port and a single write port.

10. The method of claim 8, wherein the read instruction is scheduled to execute simultaneously with the write instruction.

11. The method of claim 8, wherein each one of the P input interface circuits comprises an input buffer configured to store N by 1 vectors.

12. The method of claim 8, wherein each one of the Q output interface circuits comprises an output buffer configured to store N by 1 vectors.

13. The method of claim 11, wherein each of the P input interface circuits comprises at least one shift register coupled to receive the N by 1 vectors from the input buffer.

14. The method of claim 12, wherein each of the Q output interface circuits comprises at least one shift register coupled to provide the N by 1 vectors to the output buffer.

15. A processor comprising:

a vector register file comprising a dual-port memory including a single read port and a single write port; and

a plurality of tiles configured to process an N by N matrix and an N by 1 vector, wherein N is an integer equal to or greater than 8, and wherein each of the plurality of tiles is configured to process N data elements, and wherein the vector register file is configured to:

in response to a write instruction, during a single clock cycle store N data elements in the dual-port memory via the single write port and during each one of out of P clock cycles provide N data elements to each one of P input interface circuits of the dual-port memory, wherein P is an integer equal to N divided by L, wherein L is an integer equal to or greater than 2, and wherein each of the P input interface circuits comprises an input lane configured to carry L data elements in parallel, and wherein during the each one of the P clock cycles the dual-port memory is configured to receive N data elements via a selected one of the P input interface circuits, and

in response to a read instruction, during a single clock cycle retrieve N data elements from the dual-port memory via the single read port and during each one of out of Q clock cycles provide L data elements from each one of Q output interface circuits of the dual-port

memory, wherein Q is an integer equal to N divided by L, and wherein each of the Q output interface circuits comprises an output lane configured to carry L data elements in parallel, and wherein during the each one of the Q clock cycles the dual-port memory is configured to provide N data elements to a selected one of the Q output interface circuits.

16. The processor of claim 15, wherein each one of the P input interface circuits comprises an input buffer configured to store N by 1 vectors.

17. The processor of claim 15, wherein each one of the Q output interface circuits comprises an out put buffer configured to store N by 1 vectors.

18. The processor of claim 16, wherein each of the P input interface circuits comprises a shift register coupled to receive the N by 1 vectors from the input buffer.

19. The processor of claim 17, wherein each of the Q output interface circuits comprises a shift register coupled to provide the N by 1 vectors to the output buffer.

20. The processor of claim 15, wherein the read instruction is scheduled to execute simultaneously with the write instruction.