EEPROM CELL

ABSTRACT

A method of forming a device is disclosed. The method includes providing a substrate prepared with a cell area separated by other active areas by isolation regions. First and second gates of first and second transistors in the cell area are formed. The first gate includes first and second sub-gates separated by a first intergate dielectric layer. The second gate includes a second sub-gate surrounding a first sub-gate. The first and second sub-gates of the second gate are separated by a second intergate dielectric layer. First and second junctions of the first and second transistors are formed. The method also includes forming a first gate terminal coupled to the second sub-gate of the first transistor and a second gate terminal coupled to at least the first sub-gate of the second transistor.

Fig. 1a