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DESCRIPTION

Optical Data Storage and Retrieval System and Method

Cross-Reference to Related Applications

This is a continuation-in-part of application Serial No. 07/934,401, filed 8/24/92, which in turn is a continuation-in-part of Serial No. 07/698,673, filed 5/10/91 [abandoned], and Serial No. 07/758,059, filed 9/12/91 [abandoned].

Background of the Invention

This invention relates to digital data storage and retrieval and, more particularly, an optical data storage and retrieval system and method.

Recordable/erasable optical disks are currently available for use as data storage media. Magneto-optical recording is the technique commonly used to store the data on and/or retrieve the data from the disk. During recording, a magnetic field orients the polarity of a generalized area on the disk, while a laser pulse heats a localized area thereby fixing the polarity of the smaller area. The localized area with fixed polarity is commonly called a pit. Some encoding systems use the existence or absence of a pit on the disk to define the recorded data as a "1" or "0", respectively. The most commonly used encoding system for this pit-type recording is the run length limited (RLL) 2,7 code because it gives the highest data-to-pit ratio. This type of recording, however, does not lead to higher density because amplitude and timing margins deteriorate very rapidly as frequency is increased.

Summary of the Invention

According to a feature of the invention, a method for storing and retrieving digital data on an optical disk is provided. For writing on the disk, a binary signal having

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first and second binary values at a given clock interval is generated. Energizing pulses that have a duration less than the clock interval are generated during each clock interval having one of the binary values. The energizing pulses turn a laser beam on and off depending on the value of the binary signal. The laser beam is focused on a recording surface of a rotating disk such that the laser beam can selectively access one of a plurality of concentric or spiral tracks on the recording surface.

For reading data on a disk, a focused laser beam is directed at the recording surface of a rotating optical disk such that the laser beam can selectively access one of a plurality of tracks on the recorded surface. The rotation of the laser beam reflected off of the recorded surface is detected by means of Kerr rotation. A change in Kerr rotation to the first type represents the first binary value. A change in Kerr rotation to the second type represents the second binary value. A binary signal that represents the binary values that occur at a clock interval generated from the occurrences of the binary values and changes in rotation occurring at boundaries of the clock interval is generated.

An apparatus for recording data on an optical disk is provided. A source originates digital data at a given clock interval. A circuit converts the data to a binary signal having first and second binary values at a given clock interval and representative of the data. A pulse generator produces energizing pulses having a duration less than a clock interval for converted data having the first binary value. A laser controller applies the energizing pulses to a laser to turn the focused laser beam on and off responsive to the energizing pulses. A circuit directs the laser at a recording surface on a rotating optical data storage disk, such that the laser beam can selectively access one of a plurality of tracks on the recording surface.

An apparatus for reading data on an optical disk is provided. A circuit rotates an optical data storage disk having a recorded surface. A controller directs a laser with a focused beam at the recorded surface such that the laser beam can selectively access one of a plurality of tracks on the recorded surface. A circuit detects the rotation of the laser beam reflected off of the recorded surface. A decoder converts changes in rotation of a first and second type into first and second binary values, respectively. A circuit generates a binary signal that represents the binary values that occur at a clock interval generated from the occurrences of the binary values and changes in rotation occurring at boundaries of the clock interval.

An optical data storage and retrieval system is provided with data recording and reading utilizing cell boundary transition codes, special signal processing, and control of write pulses. Specifically, a data encoder encodes digital data in a code where transitions occur only at cell boundaries. A cell is defined as the encoded bits that represent one data bit. For example, in RLL 2,7, bits can be recorded at the cell boundary or at the center of the cell. The detection window is +/- 25% of a cell. Preferably in this invention, a pulse group code recording (GCR) 8/9 code is used. Because eight data bits are encoded into nine bits, a cell is effectively defined as one data bit. For this invention, a cell will occur at each clock interval. The detection window becomes +/- 50% of the cell. Furthermore, the GCR 8/9 code allows a limited number of consecutive zeros, e.g., three, even across word boundaries. This code also contains self clocking.

With certain data patterns, the timing margin can be enhanced. A monitor that looks for data sequences which match these predetermined data patterns is included. When one of these data patterns occurs, the laser is pulsed earlier, preferably 4 to 6 nanoseconds. Under normal

writing, the laser is pulsed uniformly. With some data patterns an increase in effective write power creates better defined edges. A second monitor looks for these data sequences and when one occurs, the laser will not be pulsed off as it would under other data patterns. Thus, the effective write power is increased.

To reduce the asymmetry of the rise and fall of an isolated pulse, signal processing will be performed for reshaping the read data waveform. For example, the pulse will be narrowed and amplified. The preferred embodiment differentiates the amplified read waveform. The amplified signal is summed with its derivative resulting in a narrowed and symmetrical pulse.

For lower frequency signals, the pulse slimming will produce overshoot. Because this overshoot is predictable, the threshold of the read circuitry can be increased momentarily to prevent false data reads. A monitor will monitor the reshaped waveform, and, upon the occurrence of an overshoot, the monitor will increase the threshold of the read waveform detector.

According to another feature of the invention, an optical data storage and retrieval system is provided with downward compatibility from a high-density recording format to a low-density, ANSI format. Specifically, a first write encoder encodes digital data in a first, preferably high-density format. A second write encoder encodes digital data in a second (i.e., ANSI) format. A first read decoder decodes digital data from the first format. A second read decoder decodes digital data from the second format. A disk drive receives a 90 millimeter replaceable optical disk. A read/write head reads encoded data from and writes encoded data to a 90 millimeter optical disk received by the drive. In a first mode, the first encoder is connected between a source of digital data and the read/write head, and the first decoder is connected between the read/write head and the utilizing apparatus. In a second mode, the second encoder is

connected between the source and the read/write head, and the second decoder is connected between the read/write head and the utilizing apparatus. Control electronics switch between the first and second modes, depending upon the format in which data is recorded on the disk received by the disk drive. As a result, the system can exploit high-density recording formats, while achieving downward compatibility to the low-density, ANSI format. Thus, data can be stored and retrieved in different formats in a single system that employs the same read/write head and disk drive.

According to yet another feature of the invention, the first and second formats are organized into sectors having the same number of bytes, there being more sectors in the first format than in the second format in accordance with the higher density. As a result, the same interface electronics can be employed to store and retrieve data in both formats.

Brief Description of the Drawings

FIG. 1 is a block diagram showing the optical data storage and retrieval system;

FIG. 2 is a series of waveforms showing uniform laser pulsing under a pulsed GCR format and nonuniform laser pulsing under an RLL 2,7 format;

FIG. 3 is a series of waveforms showing laser pulsing for various data patterns adjusted by the write compensation circuit;

FIG. 4 is a schematic diagram showing the write compensation circuit;

FIG. 5 is a series of waveforms showing laser pulsing for amplitude asymmetry correction;

FIG. 6 is a schematic diagram showing the amplitude asymmetry correction circuit;

FIG. 7 is a block diagram showing the basic relationship of elements of the pulse slimming means;

FIG. 8 is a series of waveforms showing threshold adjustments by the dynamic threshold circuit;

FIG. 9 is a schematic diagram for the dynamic threshold circuit;

FIG. 10 is a schematic block diagram of an optical data storage and retrieval system incorporating downward compatibility;

FIG. 11 is a diagram of the track layout of the high-density optical disks;

FIG. 12 is a diagram of the sector format of the high-density optical disks;

FIG. 13 is a block diagram in more detail showing the read/write circuitry of FIG. 10;

FIG. 14 is a table depicting, for each of the 21 zones in the preferred format of the high-density optical disk, the tracks within the zone, the number of sectors per track within the zone, the total number of sectors in the zone, and the write frequency of the data recorded in the zone;

FIG. 15 provides the equations used to compute the CRC bits of the ID field;

FIG. 16a is the first half of a table (Hex 00 to 7F) showing how the 8-bit bytes in the three address fields and in the data field, except for the resync bytes, are converted to channel bits on the disk; and

FIG. 16b is the second half of a table (Hex 80 to FF) showing how the 8-bit bytes in the three address fields and in the data field, except for the resync bytes, are converted to channel bits on the disk.

Detailed Description of the Specific Embodiments

In FIG. 1, during the write mode, a data source 10 transmits data to an encoder 12. The encoder 12 converts the binary data into binary code bits. The code bits are then transmitted to a laser pulse generator 14, where the code bits are converted to energizing pulses for turning a laser 16 on and off. In the preferred embodiment, a

code bit "1" indicates that the laser will be pulsed on for a fixed duration independent of the code bit pattern. However, depending on the laser and optical medium being used, performance may be enhanced by adjusting the occurrence of the laser pulse or by extending the otherwise uniform pulse duration. The output of laser 16 heats localized areas of an optical medium 18, which is being exposed to a magnetic flux that sets the polarity of the magnetic material on the optical medium 18. During reads of the optical medium, a laser beam is impinged on the surface of the medium. The polarization of the reflected laser beam will be dependent upon the polarity of the magnetic surface of the optical medium.

During the read mode, the reflected laser beam will be inputted into an optical reader 20, where the read code output will be sent to the waveform processor 22. The processed read code will be sent to a decoder 24, where output data will be transmitted to a data output port 26 for transmission.

FIG. 2 depicts the differences between the laser pulsing in GCR 8/9 and RLL 2,7 code formats. In GCR 8/9, a cell 28 is defined as a code word corresponding to a data bit. For GCR 8/9, a cell is equal to one data bit. Thus, cells 30 through 41 each correspond to one clock period 42 of clock waveform 45. For a 3½" optical disk rotating at 2,400 revolutions per minute (RPM) with a storage capacity of 256 Mbytes, clock period 42 will typically be 63 nanoseconds or a clock frequency of 15.879 Mhz. GCR data waveform 47 is the encoded data output from the encoder 12. A representative data sequence is depicted in FIG. 2. The code data sequence "010001110101" is shown in GCR data 50 through 61, where GCR data 50 is low. GCR data 51 is high. GCR data 52 is high and so forth for GCR data 53 through 61. Pulse GCR waveform 65 is the output from laser pulse means 14 inputted into pulse laser 16. In practicing the invention, a non-return-to-zero driving signal is utilized to energize the

magnetic recording head. Thus, the magnetization of the optical medium reverses polarity as the laser is pulsed on and off and the data is recorded. Pulse GCR waveform 65 as shown has not been adjusted in time or duration to reflect performance enhancement for specific data patterns. Pulse GCR 67 through 78 reflect no pulse when the corresponding GCR data 47 is low and reflect a pulse when GCR data 47 is high. For example, pulse GCR 67 has no pulse because GCR data 50 is low. Conversely, pulse GCR 68, 69, 70, and 71 show a laser pulse because GCR data 51 through 54 are each high, respectively, and similarly for pulse GCR 72 through 78. Under the depicted uniform scenario, pulse GCR pulse width 79 is uniform for pulse GCR 68, 69, 70, 71, 73, 76, and 77. For the preferred embodiment, this pulse width is 28 nanoseconds. Each laser pulse corresponding to pulse GCR waveform 65 creates a recorded pit on optical medium 18. Recorded pit 82 corresponds to pulse GCR 68. Recorded pit 83 corresponds to pulse GCR 69. Similarly, recorded pits 84 through 88 correspond to pulse GCR 70, 71, 73, 76, and 77, respectively.

Because of thermal dissipation and spot size on the optical medium 18, the recorded pits 80 are wider in time than pulse GCR 65. Successive recorded pits 80 merge together to effectively create a larger recorded pit. Thus, the elongated recorded pit has a leading edge, corresponding to the first recorded pit, and a trailing edge, corresponding to the last recorded pit. For example, the pit created by recorded pits 82 through 85 has a leading edge from recorded pit 82 and a trailing edge from pit 85. Under the GCR 8/9 data format, a leading edge corresponds to GCR data 47 going high, and a trailing edge corresponds to GCR data 47 going low. Hence, for data pattern "10001" as shown by GCR data 51 through 55, a leading edge occurs for the first "1" (GCR data 47 going high) as shown by recorded pit 82; and, at

the end of the GCR data 54, a trailing edge occurs as shown by recorded pit 85, because GCR data 55 is low.

Playback signal 90 will be low when recorded pits 80 shows no pits. At the leading edge of a pit, playback signal 90 will rise and remain high until the trailing edge of the pit is reached. The signal will go low and remain low until the next pit. For example, playback signal 91 is low because GCR data 50, which is low, did not create a pit. At the front edge of recorded pit 82, playback signal 90 has a leading edge as shown in playback signal 92. Playback signal 90 will then remain unchanged until a trailing edge occurs on a recorded pit. For example, because recorded pits 83 and 84 show no trailing edge, playback signals 93 and 94 remain high. The signal remains high during playback signal 95 because of recorded pit 85. However, because GCR data 55 is low, recorded pit 85 creates a trailing edge. Thus, playback signal 96 decays. The signal will decay to "0" until a recorded pit occurs, creating a leading edge. Thus, with the occurrence of recorded pit 86, which corresponds to GCR data 56 being high, playback signal 97 rises. Because there is no immediate successor to recorded pit 86 when GCR data 57 is low, playback signal 98 decays. Playback signal 99 remains low because there is no recorded pit when GCR data 58 is low. With GCR data 59 and 60 being high, recorded pits 87 and 88 overlap creating one larger pit. Thus, playback signal 100 rises and playback signal 101 remains high. Playback signal 102 falls at the trailing edge of recorded pit 88 when GCR data 61 is low.

For RLL 2,7 a cell consists of two data bits, which corresponds to two clock periods 121 of 2F clock waveform 120. For a 256 Mbyte disk, an RLL 2,7 encoding format will require a 2F clock pulse width 121 of 35.4 nanoseconds or a clock frequency of 28.23 MHz. The calculation of this value is straightforward. In order to maintain the same disk density, the GCR 8/9 and RLL 2,7 encoding formats must contain the same amount of

information in the same recording time. Because two code bits are required per data bit in the RLL 2,7 format, it requires a clock frequency approximately twice that of the GCR data format. The GCR data format records nine bits of code bits per eight bits of data. Thus, the GCR data bit clock is nine-eighths of the clock period 42. Thus, for a GCR clock period 42 of 63 nanoseconds, the RLL 2,7 pulse width 121 must be 35.4 nanoseconds in order to maintain the same disk density.

The RLL 2,7 data waveform 122 reflects two code bits per cell. For example, RLL 2,7 data 124 shows a data pattern "00" while RLL 2,7 data 125 shows a data pattern "10". In this data format, a "1" represents a transition in data. Thus, RLL 2,7 data 125 goes high when the "1" occurs in the data pattern. Similarly, RLL 2,7 data 126 goes low when the "1" occurs in the data pattern. While a "0" occurs, RLL 2,7 data 122 remains in the same state. Pulsed 2,7 waveform 137 reflects the pulsing of laser 16 corresponding to RLL 2,7 data 122. Thus, for RLL 2,7 data 125 and 126, during the period when that signal is high, pulsed 2,7 waveform 140 and 141 is high. Because of the thermal elongation of the pit, pulsed 2,7 waveform 141 goes low prior in time to RLL 2,7 data 126. For longer data patterns of "0", the pulsing must remain on. For example, during the data pattern "10001" as shown in RLL 2,7 data 128 and 129, pulsed 2,7 waveform 143 and 144 remains high longer than pulsed 2,7 waveform 140 and 141. For data patterns of successive "0", the pulsed 2,7 waveform 137 can be pulsed as separate pulses. For example, for the data pattern "1000001", RLL 2,7 data 132, 133, and 134 can be pulsed in two separate pulses as shown in pulsed 2,7 147, 148, and 149.

As with the GCR 8/9 format, recorded pits 160 show thermal elongation. For example, recorded pit 162 is wider in time than the pulse from pulsed 2,7 waveform 140 and 141; a similar result may be seen for recorded pit 163. Physical limitations of existing lasers and optical

disks prevent recorded pit 163 from being recorded in two successive pulses at 2F clock 120 frequency. Thus, for these intermediate size pits, the thermal accumulation distortion effects will be greater than in either recorded pit 162 or the combined recorded pits 164 and 165. Again, playback signal 167, depicted by playback signal 168 through 174, goes high on leading edges of recorded pits 160, decays on trailing edges of recorded pits 160, and remains constant during the presence or absence of pits.

The pulsed GCR code can be improved by correcting predictable position shifts. FIG. 3 shows the timing diagram for the write compensation of the laser pulse generator 14. Experimental testing showed that recording early when the laser 16 is off for two bits or greater enhances performance. Clock waveform 176 is the code bit clock used for clocking data 177, 203, and 229, which show the worst case data patterns for enhancement. Other patterns can be corrected, but will suffer in signal amplitude. Data 180 through 184 correspond to the data sequence "10100". The uncompensated pulse waveforms 188 through 192 correspond to this data pattern without write compensation. Uncompensated pulse waveforms 189 and 191 occur in the second half of the clock period. After write compensation, the output of laser pulse generator 14 corresponds to compensated pulse waveform 195, where compensated pulse waveforms 197 and 198 remain unchanged, and a shortened off-period for compensated pulse waveform 199 provides an earlier compensated pulse waveform 200. During compensated pulse 201, laser 16 remains off for a longer duration than uncompensated pulse 192. Similarly, for data 206 through 209, corresponding to data pattern "1100", uncompensated pulse waveform 211 would be off for uncompensated pulse waveform 213 followed by two pulses, i.e., uncompensated pulse waveforms 214 and 216. Again, the write compensation circuit adjusts compensated pulse waveform 220 so that compensated pulse waveform 225 will occur closer in time to compensated pulse waveform 223 so

that compensated pulse waveform 224 is shorter than uncompensated pulse waveform 215. Finally, data 231 through 235, corresponding to the data pattern "00100", have uncompensated pulse waveform 237 occurring at uncompensated pulse waveform 240. Write compensation would move compensated pulse waveform 243 earlier in time to compensated pulse waveform 246.

FIG. 4 shows the schematic diagram of the write compensation circuit, which comprises data pattern monitor 248, write compensation pattern detector 249, and delay circuit 269. Data pattern monitor 248 is a serial shift register that sequentially clocks encoded data from encoding means 12. The last five clocked in data bits are sent to write compensation pattern detector 249, where they are analyzed for determining whether to pulse the laser earlier than normal.

Data pattern monitor 248 consists of data sequence D flip-flops 250 through 256. Encoded data is input into the D port of data sequence D flip-flop 250, whose Q output WD1 becomes the input of the D port of data sequence D flip-flop 251. This clocking continues through data sequence D flip-flops 252 through 256, whose Q output WD7 is the data sequence delayed by seven clock periods from when it was first input into data pattern monitor 248. The Q outputs WD1, WD2, WD3, WD4, and WD5 of data sequence D flip-flops 250 through 254, respectively, represent the last five of the last seven data bits inputted into a data pattern monitor 248. These five bits are sent to a write compensation pattern detector 249, where they are compared to predetermined data patterns; and, if they match, an enable write signal is sent to a delay circuit 269 to indicate that the laser pulse is to occur earlier than normal.

The first data pattern is detected by inverting the Q data WD1, WD2, WD4, and WD5 from data sequence D flip-flops 250, 251, 253, and 254, respectively, through data inverters 260, 261, 262, and 263, respectively. The

output of these inverters is AND'ed with the output from data sequence D flip-flop 252 in detect AND gate 264. Thus, when a sequence "00100" occurs, the output of detect AND gate 264 goes high, indicating that a detect of the data pattern occurred. Similarly, the second data pattern is detected by inverting the Q outputs WD1, WD2, and WD4 from data sequence D flip-flops 250, 251, and 253, respectively, through the data inverters 282, 283, and 284, respectively, and AND'ing these inverted outputs with the outputs WD3 and WD5 of data sequence D flip-flops 252 and 254 in detect AND gate 286. Thus, a data pattern of "010100" will trigger a high from detect AND gate 286, indicating a detect. The third data sequence is detected by inverting the Q outputs WD1 and WD2 from data sequence D flip-flops 250 and 251, respectively, through data inverters 287 and 288 and AND'ing these inverted outputs with the Q outputs WD3 and WD4 from data sequence D flip-flops 252 and 253, respectively, in data detect AND gate 289. Thus, the data pattern of "1100" will trigger a detect from detect AND gate 289, indicating the presence of the data. The data pattern detect output of detect AND gates 264, 286, and 289 is OR'ed in detected pattern OR gate 266, whose output goes high when one of the three data patterns is detected. The detected pattern output is clocked in enable write D flip-flop 268, whose Q output, the enable write signal, is then sent to delay circuit 269.

Delay circuit 269 takes the clocked data output WD4 of data sequence D flip-flop 253 and simultaneously inputs it into delay circuit 276 and not-delay-select AND gate 274. The delayed output of delay circuit 276 is inputted into delay-select AND gate 272. The enable write signal from write compensation pattern detector 249 will enable either delay-select AND gate 272 or not-delay-select AND gate 274. When the enable write signal is low, which indicates that one of the three data patterns has not occurred, it is inverted by enable write inverter 270.

This allows the delayed data from delay circuit 276 to be clocked. On the other hand, if enable write is high, which indicates that one of the three data patterns has occurred, then the not-delay-select AND gate 274 allows the transmission of the data from data sequence D flip-flop 253, which is undelayed. The output from delay-select AND 272 and not-delay-select AND gate 274 is OR'ed in data OR gate 278, where it is outputted from delay circuit 269. Although prior discussions about the write compensation circuit or timing indicated that for the three data patterns, the write pulse would occur 10 nanoseconds earlier, in actual implementation, data is delayed 10 nanoseconds for all data but the three data patterns. The delay of delay circuit 276 is set between 8 to 12 nanoseconds for the frequency of the preferred embodiment.

When recording lower frequency data patterns, the resultant magneto-optical signal has a slower rise time than fall time. This causes the final output from the waveform processor 22 to have degraded amplitude on positive peaks, which can be corrected by recording with higher effective power at the leading edge of the data pattern. For the preferred embodiment, the data pattern "000111" will trigger a wide-write signal during the second "1" of the data pattern, thereby pulsing the laser during its normal off period.

In FIG. 5, clock waveform 301 clocks data waveform 303 through the laser pulse generator 14 for the data pattern "000111". As depicted by data 305 through 310, the laser pulse generator 14 generates pulse waveform 312 with pulses 314, 315, and 316 when data waveform 303 is a "1". During the second "1" of this data pattern, the laser pulse generator 14 will turn on for the increase power waveform 318 and generate a pulse 320. The output laser pulse waveform 322 results from the OR of pulse 312 and turn on for the increase power waveform 318 that creates laser pulses 323, 324, and 325. Under normal

operations, laser pulse 324 would be off during the first half of the clock period. However, under this particular data pattern, keeping the laser on for the laser pulses 323 and 324, effectively increases the power fifty percent during this time period.

In FIG. 6, amplitude asymmetry correction circuit 291 generates the write-wide pulse 292 (corresponds to increase power waveform 318 in Fig. 5), which will be OR'ed with the laser pulse output from delay circuit 269 (corresponds to pulse waveform 312 in Fig. 5) in laser pulse OR gate 280 (Fig. 4), resulting in output laser pulse waveform 322. The data pattern monitor 248 operates as shown in FIG. 4. The Q outputs WD2, WD3, WD4, WD5, WD6, and WD7 of data sequence D flip-flops 251 through 256, respectively, are inputted into the amplitude asymmetry correction circuit 291, where the outputs WD5, WD6, and WD7 of data sequence D flip-flops 254, 255, and 256, respectively, are inverted in data inverters 293, 294, and 295, respectively. The outputs of data inverters 293, 294, and 295 and data sequence D flip-flops 251, 252, and 253 are AND'ed in detect AND gate 296. The output of detect AND gate 296 indicates a detected pattern form "000111", which will be clocked out of write-wide D flip-flop 297 at the next clock 301.

The waveform output of the optical reader 20 will be degraded as a function of frequency and data pattern. Amplitude and timing can be enhanced by processing the signal through the waveform processor 22. The asymmetry of the rise and fall times of an isolated pulse can be improved by summing an equalized, differentiated signal with its derivative. In FIG. 7, magneto-optical signal 327 is differentiated by a differential amplifier 329. The differentiated signal is inputted into an equalizer 331, where it is equalized by 5 dB in the preferred embodiment, and the amplitude is equalized as a function of frequency. The derivative of the equalized signal is taken by a derivative processor 333 and summed with the equalized

signal in an adder 335. The output of the adder 335 is the read signal 337.

FIG. 8 shows the timing diagram for the dynamic threshold circuit shown in FIG. 9.

Read signal 337 will contain an overshoot produced by the pulse slimming. Because this overshoot is predictable, the threshold for the read circuitry can be increased during the overshoot to prevent false data reads during positive peaks 339, 340, 341, and 342, and during negative peaks 343, 344, and 345 of read signal 337. Threshold waveform 348 is switched high during positive peaks. Threshold waveforms 349, 350, and 351 are high during positive peaks 339, 340, and 341, respectively. Threshold waveforms 352, 353, and 354 are low during negative peaks 343, 344, and 345, respectively. Each peak, whether positive or negative, of the read signal 337 generates peak waveform 356, which is a short clocking pulse that occurs shortly after the read signal 337 peaks. Peaks 339, 343, 340, 344, 341, 345, and 342 of the read signal 337 generate peak waveforms 358 through 364, respectively.

As shown in Fig. 9, threshold waveform 348 is inputted into the D port of threshold delay D flip-flop 366. Peak waveform 356 clocks threshold waveform 348 through this flip-flop. Delayed threshold waveform 368 is the Q output of threshold delay D flip-flop 366, which is exclusively OR'ed with threshold waveform 348 in threshold-exclusive OR gate 370. The EXOR signal 372 is the output of threshold-exclusive OR gate 370. The EXOR signal 372 has twice the frequency of the original threshold waveform 348. The EXOR signal 372 is inputted into the D port of EXOR D flip-flop 374, where it is clocked at read clock 375. F1 waveform 376 is the Q output of EXOR D flip-flop 374. Read clock waveform 375 has a leading edge during high pulses of EXOR signal 372, except when EXOR signal 372 is low for more than one read clock waveform 375. Thus, the F1 waveform 376 is high

except for the time between the first read clock 375 pulse after the EXOR signal 372 is low for more than one read clock 375 and the next EXOR signal 372 pulse.

F1 waveform 376 is OR'ed with the EXOR signal 372 in envelope OR gate 378. The output of envelope OR gate 378 is high except for the time from the first read clock 375 after the EXOR signal 372 has been low for more than one clock period until the signal 372 goes high again. The output of envelope OR gate 378 is clocked through the D input of envelope D flip-flop 379, which is clocked by read clock 375. The Q output of the envelope D flip-flop 379 is F2 waveform 381. The F2 waveform 381 is high except from the second read clock 375 period after the EXOR signal 372 goes low until the next read clock 375 clocks a high for the EXOR signal 372. The F2 waveform 381 is inverted through the F2 inverter 383 and NOR'ed with the EXOR signal 372 in dynamic threshold NOR gate 385 to produce the dynamic threshold waveform 387. The dynamic threshold waveform 387 is high any time the EXOR signal 372 is low, except when the F2 waveform 381 is low. Thus, the dynamic threshold waveform 387 has an on-time less than a half read clock 375 period except when the EXOR signal 372 is low on the next read clock 375 period. For this exception, the dynamic threshold waveform 387 stays high from the end of the EXOR signal 372 until the second read clock 375 pulse.

The dynamic threshold waveform 387 is used to forward or reverse bias a biasing diode 389. When dynamic threshold 387 is high, biasing diode 389 is reverse biased. Conversely, when the dynamic threshold waveform 387 is low, the biasing diode 389 is forward biased.

When the dynamic threshold waveform 387 forward biases the biasing diode 389 (i.e., is low), the potential of the filter bias signal 390 is higher by the junction voltage of the biasing diode 389. This potential is 0.6 volts for standard devices. The 5-volt supply voltage drops across the limiting resistor 393 to the potential of

the filter bias signal 390, because the voltage across the charging capacitor 394 is the difference between the filter bias signal 390 and ground. The charging capacitor 394 charges up to this potential, which is also the base voltage of a transistor 395. This turns on the transistor 395, causing the voltage drop across a limiting resistor 392 to be almost 5 volts. Because the emitters of the transistors 395 and 396 are connected, the emitter voltage of the transistor 396 is less than the 2.5-volt base voltage of the transistor 396. Accordingly, the transistor 396 is off so that the collector voltage across the collector resistor 397 produces an increase threshold waveform 399 which is low. The increase threshold waveform 399 is the signal that increases the threshold of the read signal 377 detector during periods of overshoot.

When the dynamic threshold waveform 387 is high, the biasing diode 389 is reversed biased, thereby no longer grounding the base of the transistor 395. When the dynamic threshold waveform 387 goes high, the charging capacitor 394 starts charging, creating a potential at the base of the transistor 395 that will rise exponentially up to the supply voltage, 5 volts. As the filter bias signal 390 rises in voltage, the voltage at the emitter of the transistor 395 increases, which equally increases the emitter voltage of the transistor 396. When this emitter voltage exceeds the base voltage by the junction potential across the emitter-to-base junction, the transistor 396 is turned on. Turning on the transistor 396 causes the increase threshold waveform 399 to go high.

Under normal operations, the dynamic threshold waveform 387 is pulsed as described above. During normal read signals, the dynamic threshold 387 is on for a period equivalent to the on-period of read clock 375. The charge time for the voltage across the charging capacitor 394 to exceed the base voltage of 2.5 volts is longer than this half clock period of time. Thus, under normal circumstances, the increase threshold waveform 399 remains

low. However, during periods of overshoot, the dynamic threshold waveform 399 is on for a longer period of time, thereby allowing the charging capacitor 394 to charge to a voltage that exceeds 2.5 volts, thereby triggering the increase threshold waveform 399 to go high.

In FIG. 10, a host computer 410, which serves as a source and utilizer of digital data, is coupled by interface electronics 412 to a data bus 414. As host computer 410 processes data, and it wants to access external memory from time to time, a connection is established through interface electronics 412 to data bus 414. Data bus 414 is coupled to the input of a write encoder 416 and the input of a write encoder 418. Preferably, write encoder 416 encodes data from bus 414 in a low-density (i.e., ANSI) format; and write encoder 418 encodes data from data bus 414 in a higher density format. The Draft Proposal for 90MM Rewritable Optical Disk Cartridges for Information Interchange, dated 1 January 1991, which describes the ANSI format, is incorporated herein by reference. The outputs of write encoders 416 and 418 are coupled alternatively through a switch 422 to the write input of a magneto-optical read/write head 420. The read output of head 420 is coupled alternatively through a switch 424 to the inputs of a read decoder 426 and a read decoder 428. Read decoder 426 decodes data in the same format, i.e., ANSI, as write encoder 416; and read decoder 428 decodes data in the same format as write encoder 418. Preferably, the encoding and decoding technique disclosed above is employed to implement write encoder 418 and read decoder 428. The outputs of decoders 426 and 428 are connected to data bus 414.

Responsive to a mode-selection signal, switch-control electronics 430 set the states of switches 422 and 424 into either a first mode or a second mode. In the first mode, write encoder 418 and read decoder 428 are connected between data bus 414 and read/write head 420. In the second mode, write encoder 416 and read decoder 426 are

connected between data bus 414 and read/write head 420. Read/write head 420 reads encoded data from and writes encoded data to a 90 millimeter optical disk received by a replaceable optical disk drive 432, which is controlled by disk-drive electronics 434. Read/write head 420 is transported radially across the surface of the disk received by disk drive 432 by position-control electronics 436.

When a 90 millimeter disk in a high-density format is received by disk drive 432, a mode-selection signal sets the system in the first mode. As a result, data from host computer 410, to be stored on the disk, is organized by interface electronics 412 and encoded by write encoder 418; data read from the disk is decoded by read decoder 428, reorganized by interface electronics 412, and transmitted to host computer 410 for processing.

When a 90 millimeter disk in the low-density, ANSI format is received by disk drive 432, a mode-selection signal sets the system in the second mode. As a result, data from host computer 410, to be stored on the disk, is organized by interface electronics 412 and encoded by write encoder 416; data read from the disk is decoded by read decoder 426, reorganized by interface electronics 412, and transmitted to host computer 410 for processing.

Preferably, irrespective of the format used to store data, the mode-selection signal is stored on each and every disk in one format, e.g., the low-density, ANSI format, and the system defaults to the corresponding mode, e.g., the second mode. The mode-selection signal could be recorded in the control track zone in ANSI format. When a disk is installed in disk drive 432, disk-drive electronics 434 initially controls position-control electronics 436 to read the area of the disk on which the mode-selection signal is stored. Read decoder 426 reproduces the mode-selection signal, which is applied to switch-control electronics 430. If the installed disk has the low-density, ANSI format, then the system remains in

the second mode when the mode-selection signal is read. If the installed disk has the high-density format, then the system switches to the first mode when the mode-selection signal is read.

In certain cases, it may be desirable to modify the laser for the first and second modes. For example, different laser frequencies could be used or different laser-focussing lens systems could be used for the different modes. In such case, the mode-selection signal is also coupled to read/write head 420 to control the conversion between frequencies or optical-lens focussing systems, as the case may be.

It is preferable to organize the data stored in both formats to have the same number of bytes per sector, i.e., in the case of ANSI, 512 bytes. In such case, the same interface electronics 412 can be used to organize the data stored on and retrieved from the disks in both formats.

In accordance with the invention, the same read/write head 420, position-control electronics 436, optical disk drive 432, disk-drive electronics 434, interface electronics 412, and data bus 414 can be employed to store data on and retrieve data from optical disks in different formats. As a result, downward compatibility from higher-density formats that are being developed as the state of the art advances, to the industry standard ANSI format can be realized using the same equipment.

With reference to FIGS. 11, 12, and 14, the preferred format of the high-density optical disk will now be described. There are ten thousand tracks, namely tracks 0 to 9999, arranged in 21 zones. Each track is divided into a plurality of sectors. There are a different number of sectors in each zone, increasing in number moving outwardly on the disk. The frequency of the data recorded in each zone is also different, increasing in frequency moving outwardly on the disk. (See FIGS. 11 and 14 for a description of the number of tracks in each zone, the number of sectors in each zone, and the recording

frequency in each zone.) In contrast to the low-density disks, the format markings are erasably recorded on the disk using the same recording technique as is used for the data, preferably magneto-optical (MO). These format markings comprise sector fields, header fields for each sector, and control tracks. In contrast to the header fields and the data, the sector fields for all the zones are recorded at the same frequency. A description of the preferred embodiment of the sector format follows.

Sector Layout

A sector comprises a sector mark, a header, and a recording field in which 512 user data bytes can be recorded. The recording field can be empty or user-written. The total length of a sector is 721 bytes (one byte is equivalent to nine channel bits) of header and recording fields at a frequency that varies from zone to zone, plus 80 channel bits of sector mark at a fixed frequency, i.e., the same frequency for each zone. Tolerances are taken up by the buffer, i.e., the last field of the sector. The length of the header field is 48 bytes. The length of the recording field is 673 bytes.

Sector Mark (SM)

The sector mark consists of a pattern that does not occur in data, and is intended to enable the drive to identify the start of the sector without recourse to a phase-locked loop. The sector marks are recorded with a fixed frequency of 11.6 MHz for all zones. The length of the sector mark is 80 channel bits. The following diagram shows the pattern in the NRZI format.

1111 1111 1100 0000
1111 1100 0000 0000
0000 1111 1100 0000
1111 1100 0000 1111
1111 1100 1001 0010

VFO Fields

There are four fields designated either VFO_1, VFO_2, or VFO_3 to give the voltage-frequency-oscillator of the phase-locked loop of the read channel bit synchronization. The information in VFO_1 and VFO_3 is identical in pattern and has the same length of 108 bits. The two fields designated VFO_2 each have a length of 72 bits.

The continuous channel bit pattern for VFO fields is:

Standard - 101010101010...
Optional - 111111111111...

Address Mark (AM)

The address mark consists of a pattern that does not occur in data. The field is intended to give the disk drive the drive-byte synchronization for the following ID field. It has a length of 9 bits with the following pattern:

110000101

ID Fields

The three ID fields each contain the address of the sector, i.e., the track number and the sector number of the sector, and CRC bytes. Each field consists of five bytes with the following contents:

1st and 2nd byte		MSB, LSB of the track number
3rd byte bits 7 and 6	00	shall indicate field ID_1
	01	shall indicate field ID_2
	10	shall indicate field ID_3
bit 5		shall be set to ZERO
bits 4 to 0		shall number in binary notation
4th and 5th byte		CRC field containing the CRC bits computed over the first three bytes according to FIG. 15

Postambles (PA)

The postamble fields are equal in length, both having 9 bits. There is a postamble following ID_3 and a postamble following the data field. A postamble allows closure of the last byte of the preceding CRC or data field. The postambles (PA) have 9 bits of the following pattern:

Gaps

GAP 1 is a field with a nominal length of 9 channel bits, and GAP 2 is of 54 channel bits. GAP 1 shall be zeroes and GAP 2 not specified. GAP 2 is the first field of the recording field, and gives the disk drive some time for processing after it has finished reading the header and before it has to write or read the VFO_3 field.

Sync

The sync field allows the drive to obtain byte synchronization for the following data field. It has a length of 27 bits and is recorded with the bit pattern:

101000111 110110001 111000111

Data Field

The data field is used to record user data. It has a length of 639 bytes (one byte = 9 channel bits) and comprises:

512 bytes of user data
4 bytes the contents of which are not specified by this standard and shall be ignored in interchange
4 bytes of CRC parity
80 bytes of ECC parity and
39 bytes for resynchronization

User Data Bytes

The user data bytes are at the disposal of the user for recording information.

CRC and ECC Bytes

The Cyclic Redundancy Check (CRC) bytes and Error Correction Code (ECC) bytes are used by the error detection and correction system to rectify erroneous data. The ECC is a Reed-Solomon code of degree 16.

Resync Bytes

The resync bytes enable a drive to regain byte synchronization after a large defect in the data field. It has a length of 9 bits with the following pattern:

100010001

Their content and location in the data field is as follows: The resync field $R5_n$ is inserted between bytes A15n and A15n+1, where $1 \leq n \leq 39$.

Buffer Field

The buffer field has a length of 108 channel bits.

The 8-bit bytes in the three address fields and in the data field, except for the resync bytes, are converted to channel bits on the disk according to FIGS. 16a and 16b. All other fields in a sector are as defined above in terms of channel bits. The recording code used to record all data in the information regions on the disk is Group-Code (GCR 8/9) per ANSI Recorded Standard X3B5/86-123.

In FIG. 13, the write data is decoded by the RLL 2,7 encoder/decoder (ENDEC) 502 for the low-capacity, 128 Mbyte (low-density) mode. The GCR encoder/decoder (ENDEC) 504 is used in the high-capacity, 256 Mbyte (high-density) mode. The write pulse generator 506 produces a pulse width of 86 nsec with write power level varying from 7.0 mW to 8.5 mW from the inner to the outer zones for the low-capacity mode. For the high-capacity mode, the write pulse generator 507 decreases the pulse width to 28 nsec, but the write power is increased to a level that varies from 9.0 mW to 10.0 mW from the inner to the outer zones. The select circuit 509 alternatively couples pulse generator 506 or 507 to the laser diode driver of the magneto-optical read/write head, depending upon the state of an applied control bit HC. Control bit HC equals zero in the low-capacity mode and equals one in the high-capacity mode. The appropriate output is selected to drive the laser diode driver. The write clock is generated by the frequency synthesizer in the data

separator 508. The frequency is set to 11.6 Mhz for the low-capacity mode and 10.59 MHz to 15.95 MHz from inner to outer zones for the high-capacity mode.

During the playback, the preamplifier 510, which is fed by the photodiodes in the magneto-optical read/write head, can be selected for the sum mode (A+B) or the difference mode (A-B). For the sum mode, the preamplifier 510 reads the reflectance change due to the preformatted pits. These pits are stamped in the RLL 2,7 code and identify the sector mark, VFO fields, and track sector data. There are 512 bytes of data recorded in each preformatted sector. There are 10,000 tracks, segmented into 25 sectors, which totals 128 Mbytes of data for the low-capacity mode. In the high-capacity mode, the disk is formatted with GCR code. There are 40 sectors at the inner zone (i.e., zone 1), and the number of sectors gradually increases to 60 sectors at the outer zone (i.e., zone 21). Again, 512 bytes of data are recorded in each sector, which totals 256 Mbytes of data.

The writing of data in the RLL 2,7 mode is also pit-type recording. When these pits are read in the difference mode (A-B), the waveform appearing at the output of the preamplifier is identical to the preformatted pits when read in the sum mode (A+B). This signal only needs to be differentiated once by the dv/dt amplifier 512. A pulse corresponding to approximately the center of each pit is generated by digitizing the nominal output (VNOM P, VNOM N) from the programmable filter. The filter cutoff frequency is set to 5.4 MHz for the low-capacity mode responsive to the HC control bit. The filtered signal is digitized and passed through the deglitching logic circuit 518. The resulting signal called HYSTOUT (Hysterisis) is fed to the data separator 508. The signal is also coupled to the system controller to detect the sector marks. Responsive to the HC control bit, the PLO divider of the frequency synthesizer in data separator 508 is set to 3, and the synthesizer is set to

11.6 MHz. The sync data is identical to the original data decoded by the RLL ENDEC 502. This is coupled to the RLL ENDEC 502 for comparison purposes and then to the data bus to be utilized.

In the high-capacity mode, the difference mode of preamplifier 510 is selected. The playback signal appearing at the output of the preamplifier is in the NRZ (non-return-to-zero) form and requires detection of both edges. This is accomplished by double differentiation by the dv/dt amplifier and the differentiator in the programmable filter chip 514 after passage through the AGC amplifier 516. The differentiator, a high-frequency filter cutoff, and an equalizer on chip 514 are activated by the HC control bit. The filter cutoff is adjusted depending upon zone-identification bits applied to chip 514. (The differentiator and equalizer in chip 514 are not used in the low-capacity mode.) The output signal (VDIFF P, VDIFF N) from chip 514 is digitized and deglitched in the deglitching logic circuit 518. This circuit suppresses low signal level noise. The threshold level is set by a HYST control signal applied to deglitching logic circuit 518. The DATA P output is fed to the data separator. Responsive to the HC control bit, the PLO divider is set to 2, and the synthesizer is set to the appropriate frequency as determined by the applied zone number bits from the system controller. The cutoff frequency of the programmable filter is also dependent on the zone bits, but only in the high-capacity mode. The sync data is identical to the original GCR decoded data. This is coupled to the GCR ENDEC 504 for comparison purposes and then to the data bus to be utilized. The entire read function is shared between the low- and high-capacity modes.

The RLL 2,7 ENDEC 502 and write pulse generator 506 are represented by write encoder 416 and read decoder 426 in FIG. 10. The GCR ENDEC 504 and write pulse generator 507 are represented by write encoder 418 and read decoder

428 in FIG. 10. Select circuit 509 is represented by switch 422 in FIG. 10. The internal control of ENDECs 502 and 504, which alternately activates them depending on the HC control bit, is represented by switch 424 in FIG. 10. Preamplifier 510, amplifier 512, AGC amplifier 516, chip 514, deglitching logic circuit 518, and data separator 508 are employed in both the high-capacity and low-capacity modes. Thus, they are represented in part by both read decoder 426 and read decoder 428.

Claims:

1. An apparatus for recording data on an optical disk, said apparatus comprising:

a source of digital data arranged into data words having a given number of bits;

means for converting the data words to code words having one more bit than the given number using a group code recording (GCR) format, the code words including a binary signal having first and second binary values at a given clock interval determined by a bit rate of the code words;

an optical data storage disk having a recording surface;

means for rotatably driving the disk;

a laser having a focused laser beam;

means for directing the laser at the recording surface so that the laser beam accesses one of a plurality of concentric tracks on the recording surface;

means for providing a driving signal utilized for generating energizing pulses having a duration less than the clock interval when the binary signal has the first binary value, said driving signal being a non return to zero signal; and

means for applying the energizing pulses to activate the laser responsive to the energizing pulses so that the laser beam is turned on and off even when the binary signal does not change value from one bit to the next.

2. An optical data storage and retrieval system, comprising:

a source of digital data;

first means for encoding digital data in a first format higher in density than ANSI;

second means for encoding digital data in a second, ANSI format;

means for utilizing digital data;

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first means for decoding digital data from the first format;

second means for decoding digital data from the second format;

a disk drive for receiving a replaceable optical disk;

means for reading and writing encoded data, respectively, from and onto the optical disk received by the drive;

means in a first mode for connecting the first encoding means between the source and the reading and writing means and the first decoding means between the reading and writing means and the utilizing means;

means in a second mode for connecting the second encoding means between the source and the reading and writing means and the second decoding means between the reading and writing means and the utilizing means;

means for switching between the first and second modes;

means for sensing a mode-selection signal stored on a respective disk in the drive; and

means responsive to the mode-selection signal for actuating the switching means so that the switching means defaults to the first mode and switches to the second mode when the mode-selection signal designates said second mode.

3. The system according to claim 2 wherein said mode selection signal is stored in the low density format.

4. The system according to claim 3 wherein said disk includes a control track zone, and the mode selection signal is stored in said control track zone of the disk.

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5. The system according to claim 2 wherein said disk drive includes disk drive electronics, and the means for reading and writing encoded data include position-control electronics so that when a disk is installed in disk drive, the disk drive electronics initially control position-control electronics to read the area of the disk on which the mode-selection signal is stored.

6. The system according to claim 5 further including a read decoder reproducing the mode-selection signal which is applied to switch-control electronics of the means for switching between the first and second mode.

7. The system according to claim 2 wherein said first means for encoding digital data include an RLL 2,7 encoder connected to a write pulse generator.

8. The system according to claim 7 wherein said write pulse generator is able to produce pulses of approximately 86 nanoseconds.

9. The system according to claim 7 wherein said write pulse generator is able to produce pulses with write power level varying from approximately 7.0 to 8.5 milliWatt from the inner zone to the outer zone.

10. The system according to claim 2 wherein said second means for encoding digital data include an GCR 8/9 encoder connected to a write pulse generator.



11. The system according to claim 10 wherein said write pulse generator is able to produce pulses of approximately 28 nanoseconds.

12. The system according to claim 10 wherein said write pulse generator is able to produce pulses with write power level varying from approximately 9.0 to 10.0 milliWatt from the inner zone to the outer zone.

13. The system according to any one of claims 2, 7, or 10 wherein said means for switching between the two modes include a select circuit alternatively coupling first and second pulse generators to the laser diode driver of an optical read/write head of the writing means, said coupling depending upon the state of an applied control bit HC as indicated from the mode selection signal.

14. The system according to claim 2 wherein said means for reading and writing encoded data on the disk in the first mode uses a write clock having a frequency set to approximately 11.6 MegaHertz, and the means for reading and writing in the second mode uses a write clock having a frequency being variable from approximately 10.59 MHz to 15.95 MegaHertz from inner to outer zones of the disk.

15. The system according to claim 14 wherein said write clock is generated by a frequency synthesizer fed by the mode selection signal and a zone identification signal representative of the zone of the disk on which the data are written.

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16. The system according to claim 2 wherein said means for reading and writing encoded data includes an optical read/write head and a preamplifier which is fed by photodiodes.

17. The system according to claim 16 wherein said preamplifier is able to deliver a signal representative of the sum or the difference of the two signals provided by the photodiodes.

18. The system according to either claim 16 or 17 wherein said means for reading and writing encoded data includes a differentiator amplifier which is fed by the signal by the preamplifier.

19. The system according to claim 18 wherein said means for reading and writing encoded data includes an AGC amplifier which is fed by the signal provided by the differentiator amplifier.

20. The system according to claim 19 wherein said means for reading and writing encoded data includes a programmable filter which is fed by the AGC amplifier, and which receives the mode selection signal and a zone identification signal representative of the zone of the disk on which the data are written.

21. The system according to claim 20 wherein said means for reading and writing encoded data includes a digitizer and a deglitching logic circuit fed by a signal issued by the programmable filter.

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22. The system according to claim 21 wherein said means for reading and writing encoded data includes a data separator fed by the deglitching logic circuit.

23. The system according to claim 22 wherein said data separator is coupled with a frequency synthesizer fed by the mode selection signal and a zone identification signal representative of the zone of the disk on which the data is written.

24. The system according to claim 23 wherein said programmable filter is capable of being dynamically programmed to include a differentiator stage responsive to the combination of the mode selection signal and the zone identification signal.

25. The system according to claim 23 wherein said programmable filter is capable of being dynamically programmed to include a equalizer stage responsive to the combination of the mode selection signal and the zone identification signal.

26. The system according to claim 23 wherein said programmable filter has a cut-off frequency dynamically adjustable responsive to the combination of the mode selection signal and the zone identification signal.

27. The system according to claim 23 wherein said frequency synthesizer includes a PLO frequency divider which is set to two different values responsive to the mode selection signal.

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28. The system according to claim 23 wherein said frequency of the frequency synthesizer is dynamically adjusted responsive to the zone identification signal.

29. A high density optical disk including a plurality of tracks arranged in a predetermined number of zones, each track being divided into a plurality of sectors, the sector number being different in each zone, and increasing in number moving outwardly on the disk.

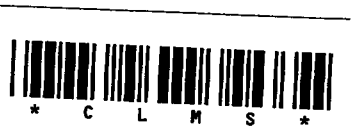
30. The high density optical disk according to claim 29 wherein said plurality of tracks includes ten thousand tracks.

31. The high density optical disk according to either claim 29 or 30 wherein said predetermined number of zones includes twenty-one zones.

32. The high density optical disk according to claim 29 including twenty first zones numbered consecutively from the center of the disk.

33. The high density optical disk according to claim 32 wherein each zone includes 480 tracks, and the outward zone includes 476 tracks.

34. The high density optical disk of claim 32 where the number of tracks per zone, the number of sectors per track in each zone, and the write frequency in each sector of each zone, are given for each zone numbered consecutively from the center of the disk according to the following table:



Zone Number	Number of Tracks per Zone	Number of Sectors per Track	Write Frequency in MegaHertz
1	476	40	10.591
2	480	41	10.852
3	480	42	11.117
4	480	43	11.368
5	480	44	11.636
6	480	45	11.963
7	480	46	12.180
8	480	47	12.459
9	480	48	12.705
10	480	49	12.992
11	480	50	13.757
12	480	51	13.533
13	480	52	13.831
14	480	53	14.086
15	480	54	14.362
16	480	55	14.624
17	480	56	14.914
18	480	57	15.130
19	480	58	15.467
20	480	59	15.694
21	480	60	15.950

1 35. The high density optical disk according to claim 32 further
2 including format markings erasably recorded on the disk using the same
3 recording technique as used for the data.

1 36. The high density optical disk according to claim 35 wherein said
2 recording technique is of a magneto-optical type.



37. The high density optical disk according to claim 35 wherein said format markings include sector fields, header fields for each sector, and control tracks.

38. The high density optical disk according to claim 35 wherein as contrasted with the header fields and the data, said sector fields for all the zones are recorded at the same frequency.

39. The high density optical disk according to claim 29 wherein each sector includes a sector mark, a header, and a recording field in which approximately 512 user data bytes can be recorded.

40. The high density optical disk according to claim 39 wherein a total length of a respective sector is the summation of approximately 721 bytes of header and recording fields at a frequency that varies from zone to zone, each byte being equivalent to nine channel bits, and approximately 80 channel bits of sector mark at a fixed frequency identical for each zone.

41. The high density optical disk according to claim 40 wherein the length of the header field is approximately 48 bytes, and the length of the recording field is approximately 673 bytes.

42. The high density optical disk according to claim 39 wherein the last field of each sector is used as buffer in order to take up tolerances.



43. The high density optical disk according to claim 42 wherein said last field of each sector has a length of approximately 108 channel bits.

44. The high density optical disk according to claim 39 wherein said sector mark consists of a pattern that does not occur in data, and is intended to enable the drive to identify the start of the sector without recourse to a phase-locked loop.

45. The high density optical disk according to claim 39 wherein said sector marks are recorded with a frequency fixed at approximately 11.6 MHz for all zones.

46. The high density optical disk according to claim 39 wherein said length of the sector mark is approximately 80 channel bits.

47. The high density optical disk according to claim 44 wherein the pattern of the sector mark in the NRZI format is:

1111	1111	1100	0000
1111	1100	0000	0000
0000	1111	1100	0000
1111	1100	0000	1111
1111	1100	1001	0010.

48. The high density optical disk according to claim 39 wherein each sector includes four voltage-frequency-oscillator fields intended to give the



voltage-frequency-oscillator of the phase-locked loop of the read channel bit synchronization.

49. The high density optical disk according to claim 48 wherein information in two of said four voltage-frequency-oscillator fields is identical in pattern.

50. The high density optical disk according to claim 48 wherein information in two of said four voltage-frequency-oscillator fields has the same length of approximately 108 bits.

51. The high density optical disk according to claim 48 wherein two of said four voltage-frequency-oscillator fields have a length of approximately 72 bits.

52. The high density optical disk according to claim 48 wherein a continuous channel bit pattern for the voltage-frequency-oscillator fields is 1 0 1 0 1 0 1 0 1 0 1 0

53. The high density optical disk according to claim 48 wherein a continuous channel bit pattern for the voltage-frequency-oscillator fields is 1 1 1 1 1 1 1 1 1 1 1 1.

54. The high density optical disk according to claim 39 wherein each sector includes an address mark field (AM) consisting of a pattern that does not

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occur in data, intended to give the disk drive the drive-byte synchronization for the following ID field.

55. The high density optical disk according to claim 54 wherein said address mark field (AM) has a length of 9 bits with the pattern 0 0 0 0 1 0 1.

56. The high density optical disk according to claim 54 wherein said address mark field (AM) has the pattern 0 0 0 0 1 0 1.

57. The high density optical disk according to claim 39 wherein each sector includes three ID fields each containing the address of the sector which includes the track number, the sector number, and any cyclic redundancy check (CRC) bytes.

58. The high density optical disk according to claim 57 wherein each ID field consists of five bytes.

59. The high density optical disk according to claim 58 wherein a first and a second byte of the ID field respectively consist in the MSB and the LSB of the track number.

60. The high density optical disk according to claim 58 wherein bits 6 and 7 of the third byte of the ID field indicate the number of the ID field.

61. The high density optical disk according to claim 58 wherein bit 5 of the third byte of the ID field is set to ZERO.

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62. The high density optical disk according to claim 58 wherein bits 0 to 4 of the third byte of the ID field is a number in binary notation.

63. The high density optical disk according to claim 58 wherein the fourth and fifth byte of the ID field consist in a CRC field containing the CRC bits computed over the first three bytes of the ID field.

64. The high density optical disk according to claim 63 wherein the 16 check bits of the CRC field of the ID field are computed using a generator polynomial of the form:

$$G(x) = x^{16} + x^{12} + x^5 + 1$$

including a residual polynomial of the form:

$$R(x) = \left(\sum_{i=8}^{i=23} \overline{b}_i \cdot x^i + \sum_{i=0}^{i=7} b_i \cdot x^i \right) \cdot x^{16} \bmod G(x)$$

where b_i denotes a bit of said first three bytes, $\overline{b}_i$ denotes an inverted bit, and b_{23} is the bit of highest order of the first byte.

65. The high density optical disk according to claim 64 wherein the 16 check bits (c_k) of the CRC field of the ID field are defined by:

$$R_c(x) = \sum_{k=0}^{k=15} c_k \cdot x^k$$

where c_{15} is the bit of highest order of the CRC field.

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66. The high density optical disk according to claim 39 wherein each sector includes two postamble fields including a first postamble following ID_3 and a second postamble following the data field, both postamble fields intended to allow closure of the last byte of the preceding CRC or data field.

67. The high density optical disk according to claim 66 wherein said two postamble fields are equal in length, both having 9 bits.

68. The high density optical disk according to claim 67 wherein said postamble fields have 9 bits of the following pattern 1 0 0 0 1 0 0 0 1.

69. The high density optical disk according to claim 39 wherein each sector includes one gap field (GAP1) localized in the beginning of the header.

70. The high density optical disk according to claim 69 wherein said gap field (GAP1) has a nominal length of 9-channel bits.

71. The high density optical disk according to claim 69 wherein bits of the gap field (GAP1) are zeroes.

72. The high density optical disk according to claim 39 wherein each sector includes a gap field (GAP2) being the first field of the recording field intended to give the disk drive a predetermined time for processing after it has finished reading the header and before it writes or reads the following fields.

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73. The high density optical disk according to claim 72 wherein said gap field (GAP2) has a nominal length of 54 channel bits.

74. The high density optical disk according to claim 39 wherein each sector includes a synchronization field (SYN) preceding the data field intended to allow the drive to obtain byte synchronization for the following data field.

75. The high density optical disk according to claim 74 wherein said synchronization field (SYN) has a length of 27 bits.

76. The high density optical disk according to claim 75 wherein said synchronization field (SYN) is recorded with the bit pattern 1 0 1 0 0 0 1 1 1 1 1 0 1 1 0 0 0 1 1 1 1 0 0 0 1 1 1.

77. The high density optical disk according to claim 75 wherein the recording field comprises:

a plurality of bytes of user data;

a plurality of bytes of cyclic redundance check (CRC) parity used by the error detection and correction system to rectify erroneous data;

a plurality of bytes for error correction code (ECC) parity used by the error detection and correction system to rectify erroneous data; and

a plurality of bytes for resynchronization for enabling a respective drive to regain byte synchronization after a large defect in the data field.

78. The high density optical disk according to claim 77 wherein the recording field has a length of approximately 639 bytes, each byte representing

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9 channel bits and including, 512 bytes of user data, 4 bytes of cyclic redundance check (CRC) parity, 80 bytes of error correction code (ECC) parity, 39 bytes for resynchronization, and 4 other bytes.

79. The high density optical disk according to claim 77 wherein said error correction code is a Reed-Solomon code of degree 16.

80. The high density optical disk according to claim 77 wherein said resynchronization bytes each have a length of 9 bits.

81. The high density optical disk according to claim 80 wherein said resynchronization bytes have the following pattern 1 0 0 0 1 0 0 0 1.

82. The high density optical disk according to claim 80 wherein said resynchronization bytes are located in the data field every 15 data byte.

83. An apparatus for recording data on an optical disk, said apparatus comprising:

a source of digital data arranged into data words having a given number of bits;

a converter that converts the data words to code words having one more bit than the given number using a group code recording (GCR) format, the code words including a binary signal having first and second binary values at a given clock interval determined by a bit rate of the code words;

an optical data storage disk having a recording surface;

a motor that rotatably drives the disk;



a laser having a focused laser beam;

a control assembly to direct the laser at the recording surface so that the laser beam accesses one of a plurality of concentric tracks on the recording surface;

a circuit assembly that provides a driving signal utilized for generating energizing pulses having a duration less than the clock interval when the binary signal has the first binary value, said driving signal being a non return to zero signal; and

a pulse generator that applies the energizing pulses to activate the laser responsive to the energizing pulses so that the laser beam is turned on and off even when the binary signal does not change value from one bit to the next.

84. An optical data storage and retrieval system, comprising:

a source of digital data;

an first encoder that encodes digital data in a first format higher in density than ANSI;

a second encoder that encodes digital data in a second, ANSI format;

a first decoder that decodes digital data from the first format;

a second decoder that decodes digital data from the second format;

a disk drive for receiving a replaceable optical disk;

a read/write head assembly that reads and writes encoded data on the optical disk received by the drive;

a first mode assembly for connecting the first encoder between the source and the read/write head assembly;



a second mode assembly for connecting the second encoder between the source and the read/write head assembly;

a switch to allow switching between the first and second modes;

a sensor permitting sensing of a mode-selection signal stored on a respective disk in the drive; and

an actuator responsive to the mode-selection signal for actuating the switch so that the switch defaults to the first mode and switches to the second mode when the mode-selection signal designates said second mode.

85. The system according to claim 84 further including a utilizing apparatus that utilized digital data.

86. The system according to claim 85 wherein said first mode assembly is further implemented to connect said first decoder between the read/write head assembly and the utilizing apparatus.

87. The system according to either claim 85 or 86 wherein said second mode assembly is further implemented to connect said second decoder between the read/write head assembly and the utilizing apparatus.

88. The system according to claim 84 wherein said mode selection signal is stored in the low density format.

89. The system according to claim 88 wherein said disk includes a control track zone, and the mode selection signal is stored in said control track zone of the disk.

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90. The system according to claim 84 wherein said disk drive includes disk drive electronics, and the read/write head assembly includes position-control electronics so that when a respective disk is installed in disk drive, the disk drive electronics initially control position-control electronics to read the area of the disk on which the mode-selection signal is stored.

91. The system according to claim 90 further including a read decoder reproducing the mode-selection signal which is applied to switch-control electronics of the switch that switches between the first and second mode.

92. The system according to claim 84 wherein said first encoder includes an RLL 2,7 encoder connected to a write pulse generator.

93. The system according to claim 92 wherein said write pulse generator produces pulses of approximately 86 nanoseconds.

94. The system according to claim 92 wherein said write pulse generator produces pulses with write power level varying from approximately 7.0 to 8.5 milliWatt from the inner zone to the outer zone.

95. The system according to claim 84 wherein said second encoder includes a GCR 8/9 encoder connected to a write pulse generator.

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96. The system according to claim 95 wherein said write pulse generator is able to produce pulses of approximately 28 nanoseconds.

97. The system according to claim 95 wherein said write pulse generator produces pulses with a write power level varying from approximately 9.0 to 10.0 milliWatt from the inner zone to the outer zone.

98. The system according to any one of claims 84, 92, or 95 wherein said switch between the two modes includes a select circuit alternatively coupling pulse generators to the laser diode driver of the read/write head assembly, said coupling depending upon the state of an applied control bit HC as indicated from the mode selection signal.

99. The system according to claim 84 wherein said first mode uses a write clock having a frequency set to approximately 11.6 MegaHertz, and said second mode uses a write clock having a frequency being variable from approximately 10.59 MHz to 15.95 MegaHertz from inner to outer zones of the disk.

100. The system according to claim 99 wherein said write clock is generated by a frequency synthesizer fed by the mode selection signal and a zone identification signal representative of the zone of the disk on which the data is written.

101. The system according to claim 84 wherein said read/write head assembly includes a preamplifier which is fed by photodiodes.

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102. The system according to claim 101 wherein said preamplifier delivers a signal representative of the sum or the difference of the two signals provided by the photodiodes.

103. The system according to either claim 101 or 102 wherein said read/write head assembly includes a differentiator amplifier which is fed by the signal from the preamplifier.

104. The system according to claim 103 wherein said read/write head assembly includes an AGC amplifier which is fed by the signal provided by the differentiator amplifier.

105. The system according to claim 104 wherein said read/write head assembly includes a programmable filter which is fed by the AGC amplifier, and which receives the mode selection signal and a zone identification signal representative of the zone of the disk on which the data are written.

106. The system according to claim 105 wherein said read/write head assembly includes a digitizer and a deglitching logic circuit fed by a signal issued by the programmable filter.

107. The system according to claim 106 wherein said read/write head assembly includes a data separator fed by the deglitching logic circuit.

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108. The system according to claim 107 wherein said data separator is coupled with a frequency synthesizer fed by the mode selection signal and a zone identification signal representative of the zone of the disk on which the data are written.

109. The system according to claim 108 wherein said programmable filter is capable of being dynamically programmed to include a differentiator stage responsive to the combination of the mode selection signal and the zone identification signal.

110. The system according to claim 108 wherein said programmable filter is capable of being dynamically programmed to include a equalizer stage responsive to the combination of the mode selection signal and the zone identification signal.

111. The system according to claim 108 wherein said programmable filter has a cut-off frequency dynamically adjustable responsive to the combination of the mode selection signal and the zone identification signal.

112. The system according to claim 108 wherein said frequency synthesizer includes a PLO frequency divider which is set to two different values responsive to the mode selection signal.

113. The system according to claim 108 wherein said frequency of the frequency synthesizer is dynamically adjusted responsive to the zone identification signal.

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