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(54) Title: APPARATUSES INCLUDING MULTI-LEVEL MEMORY CELLS AND METHODS OF OPERATION OF SAME

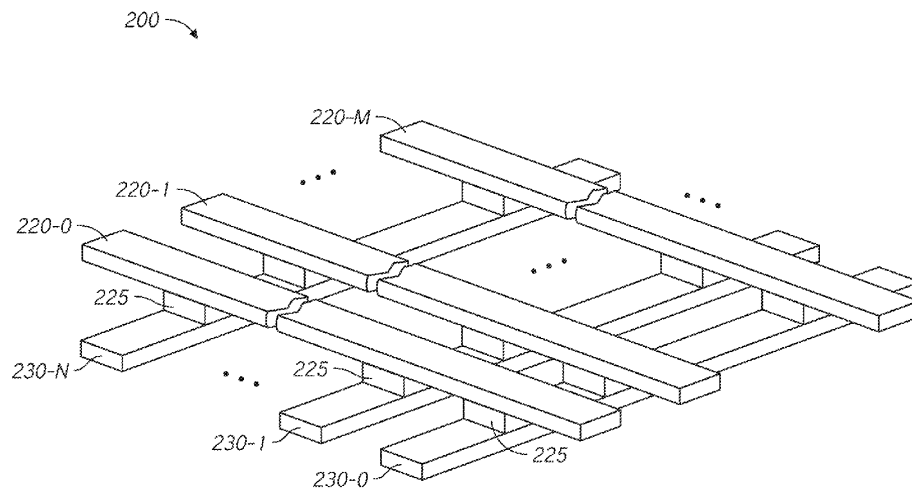


FIG. 2

(57) Abstract: Disclosed herein is a memory cell including a memory element and a selector device. Data may be stored in both the memory element and selector device. The memory cell may be programmed by applying write pulses having different polarities and magnitudes. Different polarities of the write pulses may program different logic states into the selector device. Different magnitudes of the write pulses may program different logic states into the memory element. The memory cell may be read by read pulses all having the same polarity. The logic state of the memory cell may be detected by observing different threshold voltages when the read pulses are applied. The different threshold voltages may be responsive to the different polarities and magnitudes of the write pulses.

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