STRAINED-CHANNEL MULTIPLE-GATE TRANSISTOR

ABSTRACT OF THE DISCLOSURE

A multiple-gate semiconductor structure is disclosed which includes a substrate, a fin formed of a semi-conducting material that has a top surface and two sidewall surfaces. The fin is subjected to a strain of at least 0.01% and is positioned vertically on the substrate; source and drain regions formed in the semi-conducting material of the fin; a gate dielectric layer overlying the fin; and a gate electrode wrapping around the fin on the top surface and the two sidewall surfaces of the fin overlying the gate dielectric layer. A method for forming the multiple-gate semiconductor structure is further disclosed.

FIG. 2