

THIS SHEET HAS BEEN
REPLACED

FIELD OF THE INVENTION

The present invention relates to a video processing apparatus used for a television game set or the like which can display not only a moving picture but also a background picture (or a still picture).

PRIOR ART

5 As techniques for rotating a moving picture, ones disclosed in Japanese Patent Publication No. 45,225/1980 and Japanese Patent Laid-Open Gazette No. 113,529/1976 (counterpart U.S. Patent No. 4,026,555) have been known. On the other hand, as techniques for rotating a background picture, a circuit shown in Fig. 17 has been known. In Fig. 17, a video RAM (referred to as "VRAM" hereinafter) 102
10 comprising a random access memory (referred to as "RAM" hereinafter) as well as a CPU 103 are connected to a picture processing unit 101. A main memory 104 storing, together with image data of a background picture and a moving picture, control data for displaying and controlling the image data is connected to the CPU 103. The image data stored in the main memory 104 are transferred to the VRAM 102 through the picture processing unit 101. On the basis of the control data from the CPU 103, the picture
15 processing unit 101 suitably reads data from the VRAM 102 and outputs the data to a display device 105 as a video signal to display an image on the display device 105 according to the data. Addresses of the VRAM 102 correspond to positions in the horizontal and vertical directions of the image displayed on the display device 105. The above described image data of the moving picture or the background picture (in some cases, a moving picture in addition thereto) is stored in the respective addresses of the VRAM 102.

20 In the above described conventional television game set, when a predetermined background picture is rotated or enlarged or reduced and displayed on the display device 105, during a vertical blanking period of the image data, the CPU 103 respectively calculates, on the basis of a position in the horizontal direction (referred to as "horizontal position" hereinafter) and a position in the vertical direction (referred to as "vertical position" hereinafter) on a display screen of the image data of the original background picture
25 stored in the VRAM 102, a horizontal position and a vertical position in a case where the background picture is rotated or enlarged or reduced and writes the image data of the original background picture in addresses of the VRAM 102 which correspond to the horizontal position and the vertical position as calculated. Thereafter, the picture processing unit 101 sequentially converts the data written in the VRAM 102 into a video signal and outputs the same to the display device 105 in the horizontal scanning periods.

30 On the other hand, as techniques for enlarging or reducing a background picture, one disclosed in Japanese Patent Laid-Open Gazette No. 172088/1985 (counterpart U.S. Patent No. 4,754,270) has been known.

However, the technique disclosed in Japanese Patent Publication No. 45225/1980 or Japanese Patent Laid-Open Gazette No. 113529/1976 cannot be used for the rotation of a background picture.

35 Furthermore, the prior art shown in Fig. 17 has the following disadvantage: When a background picture is rotated or enlarged or reduced and displayed, the CPU 103 must calculate the horizontal position and the vertical position in a case where the background picture is rotated or enlarged or reduced. Accordingly, the throughput of the CPU 103 is reduced so that the CPU 103 cannot perform another video processing, and the rotation processing or the enlargement or reduction processing of the background picture takes a
40 relatively long time.

Additionally, when the background picture is subjected to the rotation processing or the enlargement or reduction processing as described above, the image data of the background picture stored in the VRAM 102 is rewritten. Accordingly, the image data of the original background picture before the rotation processing or the enlargement or reduction processing cannot be preserved. Therefore, for example, when
45 the original background picture is repeatedly rotated through 30° at a time and consequently, the original background picture is rotated through a total of 360° (one rotation), computing errors at the time of respective rotations are accumulated so that a background picture is displayed in the coordinate positions different from that of the original background picture and displayed as a figure having a shape different from that of the original background picture. That is, since the original background picture cannot be preserved
50 as described above, the prior art has the disadvantage in that a background picture having the same shape as that of the original background picture cannot be displayed in the original exact position.

Furthermore, the technique disclosed in Japanese Patent Laid-Open Gazette No. 172088/1985 has the disadvantage in that a background picture cannot be enlarged or reduced while being rotated and rotation processing and enlargement or reduction processing cannot be achieved in a common circuit.



SUMMARY OF THE INVENTION

Therefore, a primary object of the present invention is to provide a video processing apparatus capable of displaying a background picture having the same shape as that of the original background picture without deformation before and after rotation.

Another object of the present invention is to provide a video processing apparatus capable of performing rotation processing and/or enlargement or reduction processing of a background picture at relatively high speed without imposing the burden on a CPU and reproducing the original background picture without deformation.

Still another object of the present invention is to provide a video processing apparatus capable of achieving enlargement or reduction processing while rotating a background picture.

The present invention is characterized by comprising storage means for storing image data of a background picture in an address corresponding to a display position of the background picture before rotation processing, operation means for operating, on the basis of control data for the rotation processing, an address of the storage means corresponding to a display position of the background picture after performing the rotation processing of the background picture, reading means for reading the image data stored in the address of the storage means which is operated by the operation means, and video signal generating means for generating a video signal on the basis of the image data read by the reading means.

In accordance with another aspect, the present invention is characterized by comprising storage means for storing image data of a background picture in an address corresponding to a display position of the background picture before rotation processing and enlargement or reduction processing, operation means for operating, on the basis of control data for the rotation processing and the enlargement or reduction processing, an address of the storage means corresponding to a display position of the background picture after performing at least one of the rotation processing and the enlargement or reduction processing of the background picture, reading means for reading the image data stored in the address of the storage means which is operated by the operation means, and video signal generating means for generating a video signal on the basis of the image data read by the reading means.

By the above described construction, the storage means stores, before rotation (and/or enlargement or reduction) processing of a picture, image data of the picture in an address corresponding to a display position of the picture before the rotation (and/or enlargement or reduction) processing.

Then, in the rotation (and/or enlargement or reduction) processing of a picture, the operation means operates an address of the storage means corresponding to a display position of the picture after performing the rotation (and/or enlargement or reduction) processing on the basis of the control data for the rotation (and/or enlargement or reduction) processing and then, the reading means reads the image data stored in the address of the storage means which is operated by the operation means, and the video signal generating means generates a video signal on the basis of the image data read by the reading means. Consequently, a video signal at the time of performing at least one of the rotation processing and the enlargement or reduction processing of the picture is obtained according to the image data stored in the storage means.

According to the present invention, a background picture having the same shape as that of the original background picture can be displayed without deformation before and after rotation. In addition, rotation and/or enlargement or reduction processing of the background picture can be achieved at high speed without imposing the burden on a CPU and the original background picture is not deformed.

The foregoing and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram showing a television gaming apparatus according to one embodiment of the present invention.

Fig. 2 is an illustrative view showing the relation between a VRAM area and a display screen area of background picture data stored in a VRAM 7.

Fig. 3 is a diagram showing a bit configuration of coordinates x and y indicating a position in the VRAM area shown in Fig. 2.

Fig. 4 is a diagram showing a memory map of the VRAM;

Fig. 5 is a diagram showing the storing conditions of color data of a background picture stored in the VRAM shown in Fig. 1.

Fig. 6 is a diagram showing bit configurations of addresses and data in a background picture character



area and a background picture screen area in the VRAM shown in Fig. 1.

Fig. 7 is a diagram for explaining the principle of rotation processing and enlargement or reduction processing of a background picture.

Fig. 8 is a detailed circuit diagram showing a background picture address control circuit.

5 Fig. 9 and 10 are timing charts showing an operation of the background picture address control circuit.

Fig. 11 is a diagram showing an example of the display of an original background picture, and Figs. 12 to 16 are diagrams respectively showing examples of the display of a background picture in a case where the original background picture is enlarged, rotated and reduced or processed in these combinations.

10 Fig. 17 is a block diagram showing a television gaming apparatus in the conventional example.

BEST MODE FOR CARRYING OUT THE INVENTION

Although in the following embodiment, a description will be made of a case where a video processing apparatus according to the present invention is applied to a television gaming machine, it should be noted
15 that the present invention is also applicable to various video processing apparatus such as a personal computer having as its object processing other than a game which is connected to a CRT display of a raster scan type or the like in the use.

Fig. 1 is a block diagram showing a television gaming apparatus according to one embodiment of the present invention.

20 Prior to describing this embodiment, a description is made of a display to which the embodiment is applied. In general, as a display applied to the television gaming apparatus, a raster scan type CRT display such as an RGB monitor or a standard television receiving set is used. One screen thereof is divided into 256 x 256 dots (pixels). However, since an image cannot be accurately displayed in portions of several lines on upper and lower sides due to a curved surface of a cathode-ray tube, 224 dots excluding the lines from
25 the number of dots in the vertical direction are actually utilized. Consequently, if one character which is the minimum unit of a background picture (and/or a moving picture) is composed of 8 x 8 dots, $32 \times 28 = 896$ characters can be simultaneously displayed on one screen.

This television gaming apparatus is so adapted that a background picture (or a still picture) forming a background which cannot be individually changed by an operation of a player and a moving picture which is
30 moved by an operation of the player or by the control of a CPU 2 are independently controlled, and comprises a picture processing unit 1 for outputting to a CRT display 8 a video signal in which the background picture and the moving picture are composed and displaying the same on the CRT display 8. Particularly the television gaming apparatus is characterized in that the picture processing unit 1 comprises a background picture address control circuit 24 and the circuit 24 evaluates a read address of a VRAM 7
35 storing image data of the background picture by operation processing at the time of rotation and/or enlargement or reduction processing of the background picture and only changes the read address without changing the image data to perform rotation and/or enlargement or reduction processing.

In Fig. 1, a read-only memory (ROM) 3, a RAM 4 and a keyboard 5 are connected to a CPU 2 for carrying out a variety of control of a television gaming machine through an address bus 11, a data bus 12
40 and a control bus 13.

The ROM 3 is used for storing program data for controlling the television gaming machine, data required to executing the program and character data and is contained in, for example, a cartridge (not shown) attachable to or detachable from the television gaming machine. This program data includes data for determining what type of moving character and/or background character is to be displayed, at which timing
45 the character is to be displayed and in which coordinate position on a screen the character is to be displayed, data for rotation, enlargement and reduction processing, and etc. As moving character data (moving picture attribute data), horizontal position data (Hc: 8 bits) for designating the horizontal position, vertical position data (Vc: 8 bits) for designating the vertical position, a character code (9 bits) for designating the type of character and a pallet code (3 bits) for designating a color pallet, a flip code (2 bits)
50 for designating the display of a character reversed in the vertical and horizontal direction, a size code (1 bit) for designating the dot size of a character and priority data (2 bits) for designating priority over a background picture are included for each character. As background character data, a character code (8 bits) for designating the type of character, color data (8 bits) for each of pixels constituting a character and etc. are included for each character. A lot of background characters are displayed in combination to constitute a
55 background picture (still picture), and a plurality of moving characters are displayed to constitute a moving picture. The background picture and the moving picture are composed on the same screen and displayed. However, as data for displaying one background picture, a background character code corresponding to each address of the background picture is designated so as to determine which background character is to



be written, in which address out of addresses in the vertical and horizontal directions in a VRAM area 40 as described later the background character is to be written and consequently, whether or not the background character is to be displayed in a desired position (coordinates) on a screen corresponding to the address.

The RAM 4 is used as a working area of the above described CPU 2. The keyboard 4 is used for a
5 player inputting information for controlling moving characters.

Furthermore, a CPU interface circuit 21 included in the picture processing unit 1 is connected to the CPU 2 through the address bus 11, the data bus 12 and the control bus 13. A reference signal generator 6, a VRAM 7 including two RAMs (7a, 7b), and a CRT display 8 such as an RGB monitor 8a or a standard television receiving set 8b are connected to the picture processing unit 1.

10 The picture processing unit 1 is used for, on the basis of control of the CPU 2, transferring image data of a moving picture and a background picture to the VRAM 7 during a vertical blanking period or at a forcedly transferring timing as well as reading the image data of the moving picture and/or the background picture stored in the VRAM 7 without any modification or outputting image data obtained by performing rotation, enlargement and reduction processing which characterized the present application, converting the
15 image data into an RGB signal and/or an NTSC color signal and outputting the same.

More specifically, the picture processing unit 1 comprises the CPU interface 21, and a moving picture address control circuit 22, a background picture address control circuit 24, a VRAM interface 27 and a color signal generating circuit 28 are connected to the CPU interface 21 through a data bus 14. An address bus 15 is connected to the moving address control circuit 22, and the address bus 15 and a data bus 16 are
20 connected to the background picture address control circuit 24 and the VRAM interface 27. The address bus 15 and the data bus 16 respectively comprise buses 15a and 15b and buses 16a and 16b respectively corresponding to the two VRAMs 7a and 7b. A moving picture data processing circuit 23 and a background picture data processing circuit 25 are together connected to the data bus 16. Video processing concerning the moving picture is performed by the moving picture address control circuit 22 and the moving picture
25 data processing circuit 23, and video processing concerning the background picture is performed by the background picture address control circuit 24 and the background picture data processing circuit 25. Outputs of the moving picture data processing circuit 23 and the background picture data processing circuit 25 are applied to a priority control circuit 26. An output of the priority control circuit 26 is converted into an RGB signal by the color signal generator 28 and directly applied to the RGB monitor 8a, and is converted
30 into an NTSC color television signal by an NTSC encoder 29 and outputted to the standard television receiving set 8b from an output terminal 9.

Furthermore, the picture processing unit 1 comprises a timing signal generator 30 and an HV counter 31. This timing signal generator 30 generates various timing signals on the basis of a clock of 21.447 MHz, a vertical synchronization signal and a horizontal synchronization signal which are outputted from the
35 reference signal generator 6. The HV counter 31 counts count data Hc and Vc for respectively designating the display positions in the horizontal and vertical directions within a display screen area 41 shown in Fig. 2 on the basis of the clock, the vertical synchronization signal and the horizontal synchronization signal from the reference signal generator 6.

Fig. 2 is a diagram showing the relation between a display screen area of the CRT display 8 and a
40 background picture storable area of the VRAM 7. A display screen area 41 of the CRT display 8 is constituted by, for example, a rectangle comprising 32 characters in the horizontal direction (breadth; x) and 28 characters in the vertical direction (length; y). On the other hand, if a background picture storable area (referred to as "VRAM area" hereinafter) 40 has no image data of a background picture in a portion which is not visible on a screen when the screen is reduced and displayed, a portion other than the background
45 picture which is actually visible is displayed in black so that a screen having no background appears. Furthermore, in a case where a background picture of the entire screen is scrolled up and down and displayed, if image data of a background picture is rewritten in real time, smooth scrolling cannot be achieved. Accordingly, the VRAM area 40 requires an area several times the display screen area 41 in the vertical and horizontal directions. In the embodiment shown, the VRAM area 40 has a storage area
50 comprising 128 characters in both the x and y directions ($128 \times 128 = 16384$) such that the horizontal position and the vertical position can be respectively designated by 7-bit address data. A background character code to be displayed is written in an address designated by respective coordinate data in the x and y directions. Herein, the origin of the VRAM area 40 is set in a left upper end of Fig. 2 and is represented by $x = 0$ and $y = 0$, and the display position of a certain dot on the VRAM area 40 is
55 represented by $P(x, y)$. Further, in order to indicate a position 53 in a left upper end of the display screen area 41, the distances in the x and y directions from the origin (referred to as offset hereinafter) are represented by H_p and V_p . Respective address data for designating the x and y coordinates are represented by x_c and y_c (7 bits each) indicating the position of a character in the VRAM area 40 and x_d and y_d (3 bits



each) indicating the position of a dot in one character 52, as shown in Fig. 3.

The VRAM 7 comprises two VRAMs 7a and 7b respectively having the same storage capacity, as shown in Fig. 4. Each of the VRAMs 7a and 7b has addresses 0 to 32K and can store 8-bit data for each of the addresses.

5 The VRAMs 7a and 7b are respectively divided into areas 51 to 54 for each 16K. The areas 51 and 52 having addresses 0 to 16K are used for storing data associated with a background picture, and the areas 53 and 54 having addresses $(16K + 1)$ to 32K are used for storing data associated with a moving picture (that is, a lot of moving character data to be displayed in a period during which the same background picture is stored in the VRAM area 40). More specifically, the area 51 in the VRAM 7a is used as a character area for
10 storing color data of a maximum of 256 background characters. As shown in Fig. 5, one character has bits corresponding to 8×8 (length $\times$ breadth) dots and includes 8-bit color data for each dot. Accordingly, one character has a storage capacity of 512 bits (64 bytes). A character code is determined for each character. The area 52 in the VRAM 7b has bytes corresponding to 128×128 (length $\times$ breadth) cells of the VRAM area 40 shown in Fig. 2 and is used as a screen area for storing a character code of a background picture
15 in an address designated by coordinates in the vertical and horizontal directions. An example of the formats of data written in the areas 51 and 52 is shown in Fig. 6.

Referring now to Figs. 1 to 6, a description is made of functions of portions shown in Fig. 1. On the basis of the control by the CPU 2, the CPU interface 21 transfers to the VRAM interface 27 data associated with a background character and a moving character by direct memory access during the vertical blanking
20 period or a forcedly transferring instruction and, at the same time, generates latch signals LA1 to LA4, LA11, LA12, LA14 and LA15 for transferring control data for rotation, enlargement and reduction to the background picture address control circuit 24. The data on the background character and the moving character are written in advance in the VRAM 7 by the VRAM interface 27.

The moving picture address control circuit 22 comprises a moving picture attribute memory, an in-range
25 detecting circuit and a moving picture address data generating circuit, the details thereof being known in, for example, Japanese Patent Laid-Open Gazette No. 118184/1984 filed by the applicant of the present application. Attribute data of 128 moving characters are transferred to the moving picture attribute memory from the CPU 2 through the CPU interface 21 and the data bus 14 and stored therein during a certain vertical blanking period. The in-range detecting circuit retrieves for each scanning line data to be displayed
30 in the next horizontal scanning from the data stored in the moving picture attribute memory. The moving picture address data generating circuit generates an address of the VRAM 7 indicating a reversed position in the display screen area 41 and outputs the same through the address bus 15 when V-flip data of the attribute data in-range detected is at the "H" level. On the other hand, it outputs an address of the VRAM 7 corresponding to the display screen area 41 of character data to the VRAM 7 through the address bus 15
35 without any modification when the V-flip data is at the "L" level. The VRAM 7 is responsive to the address so as to apply to the moving picture data processing circuit 23 through the data bus 16 the color data (4 bits per dot) of moving pictures stored in the moving picture character areas 53 and 54 which correspond to addresses outputted from the moving picture address data generating circuit in the moving picture address control circuit 22. Furthermore, the moving picture address data generating circuit directly applies to the
40 moving picture data processing circuit 23 the H-flip data (1 bit), the color pallet data (3 bits) and the priority data (2 bits) out of the attribute data of the moving characters in-range detected.

Consequently, data of 10 bits per dot comprising the color data read from the VRAM 7, the H-flip data, the color pallet data and the priority data directly applied from the moving picture address control circuit 22 is sequentially inputted to the moving picture data processing circuit 23 with respect to 256 dots of one
45 scanning line.

The moving picture data processing circuit 23 temporarily stores data of the next one scanning line which is inputted during the horizontal blanking period and then, temporarily stores data of 9 bits per dot excluding the H-flip data included in the data in the order reverse to the input order when the H-flip data is at the "H" level to perform H-flip processing. On the other hand, this circuit 23 temporarily stores the 9-bit
50 data in the input order when the H-flip data is at the "L" level. The moving picture data of one scanning line which is temporarily stored is outputted to the priority control circuit 26 in synchronization with horizontal scanning on the basis of the count data H_c outputted from the HV counter 31.

At the time of normal processing of a background picture, the background picture address control circuit 24 calculates a read address (16 bits) of a character code previously stored in the screen area 52 in
55 the VRAM 7b corresponding to a dot of the background picture on the basis of the offset data H_p and V_p on the screen and the control data including the H-flip data HF and the V-flip data VF which are applied from the CPU 2 and the count data H_c and V_c applied from the HV counter 31 and applies the address to the VRAM 7b through the address bus 15b. In addition, at the time of rotation processing and enlargement or



reduction processing of a background picture, the background picture address control circuit 24 calculates a read address of a character code corresponding to a dot of the background picture at the time of rotation and enlargement or reduction on the basis of the offset data H_p and V_p on the screen, the H-flip data HF, the V-flip data VF and parameter data including processing constants A, B, C and D at the time of rotation and enlargement or reduction which are applied from the CPU 2 and the count data H_c and V_c applied from the HV counter 31 and applies the address to the VRAM 7b. The principle of the operation processing for rotation, enlargement and reduction will be described with reference to Fig. 7 as described later.

In addition, the background picture address control circuit 24 calculates a read address of a character code corresponding to one dot of a background picture after performing scrolling processing of the screen on the basis of the offset data H_p and V_p on the screen applied from the CPU 2. At the same time, the background picture address control circuit 24 calculates a read address of a character code corresponding to one dot of the background picture after performing H-flip processing when the H-flip data HF is at the "H" level, while calculating a read address of a character name corresponding to one dot of the background picture after performing V-flip processing when the V-flip data VF is at the "H" level. The most significant two bits of the 16-bit read address data calculated by the background picture address control circuit 24 are "00" and the least significant 14 bits thereof are position data x_c and y_c (7 bits each) of a character corresponding to a display position of the background picture, as shown in Fig. 6.

The VRAM 7b applies a character code stored in the address applied from the background picture address control circuit 24 to the background picture address control circuit 24 through the data bus 15b. Responsively, the background picture address control circuit 24 applies to the VRAM 7a through the address bus 15a an address comprising the most significant two bits "00", a 8-bit character code and the position data y_d (3 bits) and x_d (3 bits) of a dot corresponding to a display position of the background picture. The VRAM 7a reads the 8-bit color data stored in the address applied from the background picture address control circuit 24 and applies the same to the background picture data processing circuit 25 through the data bus 16a.

Correspondingly, the background picture data processing circuit 25 latches the color data of 8 bits per dot as inputted and then, applies the 8-bit color data to the priority control circuit 26 on the basis of the count data H_c outputted from the HV counter 31.

The priority control circuit 26 determines the priority between the 7-bit moving picture data inputted from the moving picture data processing circuit 23 and the 8-bit background picture data inputted from the background picture data processing circuit 25 on the basis of priority data and outputs higher-priority data out of the moving picture data and the background picture data to the color signal generator 28. For example, the priority control circuit 26 outputs background picture data comprising the most significant three bits "000" and 8-bit color data to the color signal generator 28 when the priority data is "00", while outputting moving picture data of a total of 7 bits comprising 3-bit color pallet data and 4-bit color data to the color signal generator 28 when the priority data is "01".

The color signal generator 28 includes a color pallet table composed of a RAM having 8-bit addresses and stores color signal data applied from the CPU 2 in the color pallet table during the vertical blanking period. During the horizontal scanning period, the color signal generator 28 reads the color signal data stored in a corresponding address of the color pallet table on the basis of the 8-bit moving picture data or background picture data inputted from the priority control circuit 26 and then, converts the color signal data into an RGB signal of 5 bits for each color. Furthermore, the color signal generator 28 directly outputs the RGB signal to the RGB monitor 8a in synchronization with the count data H_c and V_c applied from the HV counter 31 and at the same time, outputs the same to the NTSC encoder 29. The NTSC encoder 29 carries out digital-to-analogue conversion of the RGB signal for each color and then, converts the RGB signal into an NTSC color television signal and outputs the same to the standard television receiving set 8b from the output terminal 9.

Fig. 7 is a diagram for explaining the principle of rotation processing and the enlargement or reduction processing of a background picture performed by the background picture address control circuit 24. In Fig. 7, it is assumed that x is a coordinate for each dot in the horizontal direction on the screen of the CRT display 8 and y is a coordinate for each dot in the vertical direction. However, the y direction is reverse to that shown in Fig. 2.

Let $P(X_1, Y_1)$ be coordinates of the original background picture before the background picture address control circuit 24 performs rotation processing and the enlargement or reduction processing, and let $Q'(X_2', Y_2')$ be coordinates of the background picture in a case where the original background picture is rotated around coordinates $R(X_0, Y_0)$ through an angle γ [rad]. Furthermore, let $Q(X_2, Y_2)$ be coordinates of the background picture in a case where the background picture having the coordinates $Q'(X_2', Y_2')$ is enlarged or reduced at scaling magnification α in the x direction and at scaling magnification β in the y direction



using as a basis the coordinates $R(X_0, Y_0)$. In this case, the relationship among the coordinates P, R and Q is expressed by the following equation (1):

$$\begin{bmatrix} X_2 \\ Y_2 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} X_1 - X_0 \\ Y_1 - Y_0 \end{bmatrix} + \begin{bmatrix} X_0 \\ Y_0 \end{bmatrix} \quad \dots (1)$$

Herein, constants (parameters) A, B, C and D are expressed by the following equations (2) to (5):

$$A = 1/\alpha \cdot \cos\gamma \quad (2)$$

$$B = 1/\alpha \cdot \sin\gamma \quad (3)$$

$$C = -1/\beta \cdot \sin\gamma \quad (4)$$

$$D = 1/\beta \cdot \cos\gamma \quad (5)$$

When not enlargement or reduction processing of a background picture but only rotation processing is performed, $\alpha = \beta = 1$. Consequently, the constants A, B, C and D in this case are expressed by the following equations (6) to (9):

$$A = \cos\gamma \quad (6)$$

$$B = \sin\gamma \quad (7)$$

$$C = -\sin\gamma \quad (8)$$

$$D = \cos\gamma \quad (9)$$

Furthermore, when not rotation processing of the background picture but only enlargement or reduction processing is performed, $\gamma = 0$. Accordingly, the constants A, B, C and D are expressed by the following equation (10) to (12):

$$A = 1/\alpha \quad (10)$$

$$B = C = 0 \quad (11)$$

$$D = 1/\beta \quad (12)$$

In the equation (1), the coordinates P (X_1, Y_1) of the original background picture are expressed by the following equations (13) and (14) if the above described offset data H_p and V_p in the VRAM area 40 shown in Fig. 2 and the count data H_c and V_c outputted from the VH counter 31 are used:

$$X_1 = H_p + H_c \quad (13)$$

$$Y_1 = V_p + V_c \quad (14)$$

Consequently, if x_2 and y_2 are developed by substituting the above described equations (13) and (14) in the equation (1), x_2 and y_2 are expressed by the following equations (15) and (16):

$$X_2 = [X_0 + (H_p - X_0) \cdot A + (V_p - Y_0) \cdot B + V_c \cdot B] + H_c \cdot A \quad (15)$$

$$Y_2 = [Y_0 + (V_p - Y_0) \cdot D + (H_p - X_0) \cdot C + V_c \cdot D] + H_c \cdot C \quad (16)$$

In the above described equation (15) and (16), terms $H_c \cdot A$ and $H_c \cdot C$ are terms which are changed for each dot on the screen, and terms other than $H_c \cdot A$ and $H_c \cdot C$ (that is, terms in parenthesis) are terms which are not changed during one scanning line. Consequently, the terms $H_c \cdot A$ and $H_c \cdot C$ must be calculated for each dot in the horizontal scanning period. On the other hand, the terms other than $H_c \cdot A$ and $H_c \cdot C$ need not be calculated during the horizontal scanning period, and it is rather difficult to calculate the terms at a time in a very short time for each dot of horizontal scanning. Accordingly, the terms are



collectively calculated before scanning of one line is started (preliminarily processed). Therefore, in order to calculate parts to be preliminarily processed of the equations (15) and (16) in simple circuits, the equations are replaced with the following equations (17) to (24) and operated in a step-by-step manner:

$$\begin{aligned}
 5 \quad E_1 &= H_p - X_0 & (17) \\
 E_2 &= V_p - Y_0 & (18) \\
 E_3 &= X_0 + E_1 \cdot A & (19) \\
 E_4 &= Y_0 + E_2 \cdot D & (20) \\
 E_5 &= E_3 - E_2 \cdot B & (21) \\
 10 \quad E_6 &= E_4 - E_1 \cdot C & (22) \\
 E_7 &= E_5 - V_c \cdot B & (23) \\
 E_8 &= E_6 - V_c \cdot D & (24)
 \end{aligned}$$

15 Fig. 8 is a detailed circuit diagram showing the background picture address control circuit 24. This background picture address control circuit 24 evaluates coordinates (X_2 , Y_2) at the time of rotation and enlargement or reduction of a background picture by a matrix operation using the above described equation (1) and then, outputs its coordinate data as a read address of the screen area 52 and a read address of the character area 51.

20 More specifically, the background picture address control circuit 24 includes registers FF1 to FF23 each composed of a plurality of delay-type (D-type) flip-flops. Each of the registers FF1 to FF23 latches data applied to its input terminal at a timing when a latch signal is applied, and outputs the data to its output terminal. In addition, reversed clocks obtained by reversing a clock 10MCK of 10.739 MHz outputted from the timing signal generator 30 are respectively inputted to the registers FF13 to FF19. Reversed clocks
25 obtained by reversing a clock 5MCK of 5.369 MHz outputted from the timing signal generator 30 are respectively inputted to the registers FF18, FF20, FF21, FF22 and FF23.

16-bit constant data A, B, C and D applied from the CPU 2 through the CPU interface circuit 21 and the data bus 14 are respectively latched in the registers FF1 to FF4 at timings when corresponding latch signals LA1 to LA4 are applied. Their latched data are applied to input terminals a, b, c and d of a switching device SW1. The switching device SW1 selects any one of the latched data inputted to the input terminals a, b, c and d and outputs the same to input terminals a of a multiplier MPY on the basis of an XS signal outputted from a timing signal generator 30.

Count data H_c outputted from the HV counter 31 is inputted to an exclusive OR circuit XOR1. The register FF5 latches the 8-bit count data V_c outputted from the HV counter 31 and outputs the same to an
35 exclusive OR circuit XOR2. The registers FF6 and FF7 respectively latch the 1-bit H-flip data HF and the 1-bit V-flip data VF applied from the CPU 2 on a leading edge of a machine clock of the CPU 2 and respectively output to the exclusive OR circuits XOR1 and XOR2 the H-flip data HF and data of 8 bits having the same level and the V-flip data VF and data of 8 bits having the same level.

The details of the exclusive OR circuits XOR1 and XOR2 will be described. Both the circuits
40 respectively include eight exclusive OR gates. Respective bits of the count data H_c are applied as respective one inputs of the eight exclusive OR gates included in the exclusive OR circuit XOR1, and corresponding bits of the data in the register FF6 are applied as the respective other inputs thereof. Respective bits of the count data V_c are applied as respective one inputs of the eight exclusive OR gates included in the exclusive OR circuit XOR2, and corresponding bits of the data in the register FF7 are
45 applied as the respective other inputs thereof. The respective eight exclusive OR gates included in the exclusive OR circuits XOR1 and XOR2 perform an exclusive OR operation of the respective two inputs and apply 8-bit data which are the results of the operation to input terminals a and input terminals b of the switching device SW2 directly or through the register FF8. This switching device SW2 has input terminals each 11 bits, and the most significant three bits of each of the input terminals a and b are connected to the
50 ground. In addition, the switching device SW2 includes input terminals c and d, and 11-bit data from the registers FF9 and FF10 are respectively inputted to the input terminals c and d.

The register FF9 latches data of the least significant 11 bits (E_1) of 18-bit data applied from an adder ADD on a leading edge of a latch signal LA9 outputted from the timing signal generator 30 and applies its latched data to the input terminals c of the switching device SW2. The register FF10 latches data of the
55 least significant 11 bits (E_2) of the 18-bit data applied from the adder ADD on the leading edge of a latch signal LA10 outputted from the timing signal generator 30 and applies its latched data to the input terminals d of the switching device SW2. The switching device SW2 selects any one of the data inputted to the input terminals a, b, c and d on the basis of a YS signal outputted from the timing signal generator 30 and applies



the same to input terminals b of the multiplier MPY.

The multiplier MPY multiplies any one of the data A to D inputted to the input terminals a by any one of the data E1, E2 and V_c inputted to the input terminals b to evaluate the second term in any one of the equations (19) to (24) and applies data which are the results of the multiplication to input terminals c of a switching device SW3 through the register FF13.

The register FF11 latches offset data H_p (10 bits) in the x direction applied from the CPU 2 on the leading edge of the machine clock and applies the same to input terminals a of the switching device SW3. In addition, the register FF12 latches offset data V_p (10 bits) in the y direction applied from the CPU 2 on the leading edge of the machine clock and applies the same to input terminals b of the switching device SW3. The most significant six bits and the least significant two bits of each of the input terminals a and b of the switching device SW3 are connected to the ground. The least significant two bits of the data inputted to each of the input terminals of the switching device SW3 correspond to data after the decimal point.

The switching device SW3 selects one of the data inputted to the input terminals a, b and c on the basis of an AS signal outputted from the timing signal generator 30 and applies the same to input terminals a of the adder ADD.

The register FF14 latches the position data x_0 in the x direction of the original background picture applied from the CPU 2 (the least significant eight bits of the data bus 14) on the leading edge of the machine clock and then, applies data of a total of 10 bits comprising the most significant two bits "00" and its latched data to input terminals a of a switching device SW4. In addition, the register FF15 latches the position data Y_0 in the y direction of the original background picture applied from the CPU 2 (the most significant two bits upper than the above described data x_0 of the data bus 14) on the leading edge of the machine clock and then, applies data of a total of 10 bits comprising the most significant eight bits "00000000" and its latched data to input terminals b of the switching device SW4. The most significant six bits and the least significant two bits of each of the input terminals a and b of the switching device SW4 are connected to the ground. The least significant two bits of the data inputted to each of the input terminals of the switching device SW4 correspond to data after the decimal point.

The register FF16 latches 18-bit data outputted from the adder ADD on a leading edge of a clock CK16 outputted from the timing signal generator 30 and applies the same to input terminals c of the switching device SW4. In addition, the register FF17 latches 18-bit data outputted from the adder ADD on a leading edge of a clock CK17 outputted from the timing signal generator 30 and applies the same to input terminals d of the switching device SW4. The switching device SW4 applies 18-bit data out of the data inputted to the input terminals a, b, c and d to an exclusive XOR circuit XOR3 on the basis of a BS signal outputted from the timing signal generator 30. The exclusive OR circuit XOR3 includes 18 exclusive OR gates. Corresponding bits of the data in the switching device SW4 are applied as respective one inputs of the exclusive OR gates, and an ADS signal outputted from the timing signal generator 30 is applied as the respective other inputs thereof.

Furthermore, certain one bit of the ADS signal is inputted to a carry-in terminal of the adder ADD. When one bit of the ADS signal inputted to the carry-in terminal of the adder ADD is at the "H" level, the ADS signal inputted to the respective other input terminals of the exclusive OR gates in the exclusive OR circuit XOR3 is a signal in which all 18 bits are at the "H" level. On the other hand, one bit of the ADS signal inputted to the carry-in terminal of the adder ADD is at the "L" level, the ADS signal inputted to the respective other input terminals of the exclusive OR gates in the exclusive OR circuit XOR3 is a signal in which all 18 bits are at the "L" level. The exclusive OR circuit XOR3 operates in the same manner as those of the exclusive OR circuits XOR1 and XOR2. That is, the exclusive OR circuit XOR3 performs an exclusive OR operation of data inputted to one input terminals and data inputted to the other input terminals with respect to each bit and applies the results of the operation to input terminals b of the adder ADD.

The adder ADD adds both the data inputted to the input terminals a and b and further adds one to the results of the addition only when the ADS signal at the "H" level is inputted to the carry-in terminal. Thereafter, out of the results of the addition, 18-bit data is stored in the registers FF16 and FF17, data of the least significant 11 bits is stored in the registers FF9 and FF10, 10-bit data is stored in the registers FF18 and FF19, and data of the least significant eight bits is stored in the register FF21.

Therefore, when the "H" signal is inputted to the carry-in terminal, an operation of subtracting the output data of the switching device SW4 from the output data of the switching device SW3 is performed by operations of the exclusive OR circuit XOR3 and the adder ADD. On the other hand, when the "L" signal is inputted to the carry-in terminal, a reversing operation by the exclusive OR circuit XOR3 and an operation of adding one by the adder ADD are not performed. Consequently, an operation of only adding the output data of the switching device SW3 to the output data of the switching device SW4 is performed. In this embodiment shown, the multiplier MPY and the adder ADD repeatedly perform a multiplication operation or



an addition operation of two data (coordinate data, constant data or data of the results of an operation obtained immediately before) applied by switching of the switching device SW1 to SW4 in a time shared manner to sequentially perform operations expressed by the equations (17) to (24) and finally perform operations expressed by the equations (15) and (16) by respective one circuits. Moreover, the rotation and/or the enlargement or reduction processing can be achieved using a common circuit by changing the constant data.

The register FF18 latches the 10-bit data as inputted and then, outputs data yc of the most significant seven bits as address data of the third to eighth bits from the most significant bit of the address bus 15b through a tri-state buffer amplifier (referred to as "buffer amplifier" hereinafter) BA2 and applies data yd of the least significant three bits to the register FF22. The register FF19 latches the 10-bit data as inputted and then, applies the same to the register FF20. The register FF20 latches the 10-bit data as inputted and then, outputs data xc of the most significant seven bits as address data of the least significant seven bits of the address bus 15b through a buffer amplifier BA3 and applies data xd of the least significant three bits to the register FF22.

The register FF21 latches the 8-bit character code inputted from the VRAM 7b through the data bus 16b and then, outputs the same as address data of the third to seventh bits from the most significant bit of the address bus 15b through a buffer amplifier BA5. The register FF22 latches the two 3-bit data yd and xd as inputted and then, outputs the data as address data of the least significant six bits of the address bus 15a through the register FF23 and a buffer amplifier BA6.

In addition, input terminals of two bits of the buffer amplifier BA1 are connected to the ground, and output terminals (2 bits) of the buffer amplifier BA1 are connected to the most significant two bits of the address bus 15b. Input terminals of two bits of the buffer amplifier BA4 are connected to the ground, and output terminals (2 bits) of the buffer amplifier BA4 are connected to the most significant two bits of the address bus 15a.

Figs. 9 and 10 are timing charts for explaining an operation of the enlargement or reduction and/or the rotation processing of a background picture which characterizes this embodiment. In particular, Fig. 9 shows one horizontal scanning period and horizontal blanking period, and Fig. 10 shows the periods of preliminary processing and a part of real-time processing in a case where an H count value is 9 to 17.5 by way of example.

Referring now to Figs. 1 to 10, the detailed operation of the enlargement or reduction and/or the rotation processing of a background picture which characterizes the present embodiment will be described. A description is made of an operation of the background picture address control circuit 24 for performing processing of one scanning line in a case where a background picture positioned in the display screen area 41 in the VRAM area 40 shown in Fig. 2 is rotated around the reference coordinates $R(X_0, Y_0)$ through an angle γ and is enlarged or reduced at scaling magnification α in the x direction and scaling magnification β in the y direction as described above with reference to Fig. 7.

Meanwhile, the constants A, B, C and D are previously calculated in the CPU 2 using the above described equations (2) to (5) on the basis of α , β and γ as described above, and data of the constants A, B, C and D are previously calculated in the CPU 2 and inputted to the flip-flops FF1 to FF4 from the CPU 2 through the CPU interface circuit 21 and the data bus 14 to be latched therein. In addition, the above described offset data H_p and V_p on the screen, the data x_0 and y_0 representing the above described reference coordinates, and the H-flip data HF and the V-flip data VF with respect to the background picture are respectively outputted from the CPU 2 and inputted to the flip-flops FF11, FF12, FF14, FF15, FF6 and FF7 through the CPU interface circuit 21 and the data bus 14 to be latched therein.

Now, the data H_c inputted from the HV counter 31 is reversed by the exclusive OR gate XOR1 and outputted to the input terminals a of the switching device SW2 when the H-flip data HF is at the "H" level. On the other hand, the data H_c inputted from the HV counter 31 is outputted to the input terminals a of the switching device SW2 through the exclusive OR gate XOR1 without any modification when the H-flip data HF is at the "L" level. Further, the data V_c inputted from the HV counter 31 and latched in the flip-flop FF5 during processing of one scanning line is reversed by the exclusive OR gate XOR2 and inputted to the flip-flop FF8 to be latched therein when the V-flip data VF is at the "H" level. On the other hand, the above data V_c is inputted to the flip-flop FF8 through the exclusive OR gate XOR2 without any modification to be latched therein when the V-flip data VF is at the "L" level. H-flip and V-flip operations of a background picture are respectively performed by reversing operations of the above described exclusive OR gates XOR1 and XOR2. The data outputted from the above described exclusive OR gates XOR1 and XOR2 are respectively referred to as data H_c and V_c irrespective of whether or not they are reversed, for convenience of description.

Additionally, the character name and the color data of the original background picture before rotation



processing and enlargement or reduction processing are previously stored in the background picture screen area 52 in the VRAM 7b and the background picture character area 51 in the VRAM 7a, respectively.

In Fig. 10, timings when a clock 10MCK of 10.739 MHz (it is given / in front of a symbol in place of a bar to be given above the symbol hereinafter) outputted from the timing signal generator 30 rise are represented by $t_1, t_2, t_3, \dots, t_{20}, \dots$ for convenience of description. In this case, processing from the time t_1 to the time t_9 is preliminary processing of calculating constants E_1 to E_8 which is performed in the vertical blanking period before the period of an image signal which is a video signal outputted from the picture processing unit 1. Processing after the time t_9 is real-time processing performed in synchronization with the generation and the display of an image signal which is a digital signal of RGB representative of a video signal, which is processing of evaluating coordinates $Q(X_2, Y_2)$ of the background picture at the time of the rotation and the enlargement or reduction on the basis of the constants calculated in the preliminary processing and the count data H_c and V_c , outputting an address of the background picture screen area 52 in the VRAM 7b and then, outputting an address of the background picture character area 51 in the VRAM 7a on the basis of a character code read from the area 52.

In a time period from the time t_1 to the time t_2 , both the switching devices SW3 and SW4 are switched to their input terminals a. The data H_p is inputted to the input terminals a of the adder ADD from the flip-flop FF11 through the switching device SW3. On the other hand, the data x_0 is inputted to the input terminals b of the adder ADD from the flip-flop FF14 through the switching device SW4 and the exclusive OR gate XOR3. At this time, the ADS signal is at the "H" level.

Accordingly, the exclusive OR gate XOR3 and the adder ADD perform subtraction processing in the above described manner and thus, perform an operation of data $E_1 = (H_p - x_0)$ and outputs the results of the operation. The data E_1 is inputted to the flip-flop FF9 to be latched therein on the leading edge of the latch signal LA9 at the time t_2 .

In a time period from the time t_2 to the time t_3 , the switching devices SW1 and SW2 are respectively switched to its input terminals a and its input terminals c. The data A is inputted to the input terminals a of the multiplier MPY from the flip-flop FF1 through the switching device SW1. On the other hand, the data E_1 is inputted to the input terminals b of the multiplier MPY from the flip-flop FF9 through the switching device SW2. The multiplier MPY performs an operation of data $A \cdot E_1$ and outputs the results of the operation. The data $A \cdot E_1$ is inputted to the flip-flop FF13 to be latched therein on the leading edge of the clock /10MCK at the time t_3 .

Furthermore, in the time period from the time t_2 to the time t_3 , both the switching devices SW3 and SW4 are switched to their input terminals b. The data V_p is inputted to the input terminals a of the adder ADD from the flip-flop FF11 through the switching device SW3. On the other hand, the data y_0 is inputted to the input terminals b of the adder ADD from the flip-flop FF15 through the switching device SW4 and the exclusive OR gate XOR3. At this time, the ADS signal is at the "H" level. Accordingly, the exclusive OR gate XOR3 and the adder ADD perform subtraction processing in the above described manner and thus, perform an operation of data $E_2 = (V_p - y_0)$ and output the results of the operation. The data E_2 is inputted to the flip-flop FF10 to be latched therein on the leading edge of the latch signal LA10 at the time t_3 .

In a time period from the next time t_3 to the time t_4 , both the switching devices SW1 and SW2 are switched to their input terminals d. The data D is inputted to the input terminals a of the multiplier MPY from the flip-flop FF4 through the switching device SW1. On the other hand, the data E_2 is inputted to the input terminals b of the multiplier MPY from the flip-flop FF10 through the switching device SW2. The multiplier MPY performs an operation of data $D \cdot E_2$ and outputs the results of the operation. The data $D \cdot E_2$ is inputted to the flip-flop FF13 to be latched therein on the leading edge of the clock /10MCK at the time t_4 .

Additionally, in the time period from the time t_3 to the time t_4 , the switching devices SW3 and SW4 are respectively switched to its input terminals c and its input terminals a. The data $A \cdot E_1$ is inputted to the input terminals a of the adder ADD from the flip-flop FF13 through the switching device SW3. On the other hand, the data x_0 is inputted to the input terminals b of the adder ADD from the flip-flop FF14 through the switching device SW4 and the exclusive OR gate XOR3. At this time, the ADS signal is at the "L" level. Accordingly, the exclusive OR gate XOR3 and the adder ADD perform addition processing in the above described manner and thus, performs an operation of data $E_3 = (A \cdot E_1) + x_0$ and output the results of the operation. The data E_3 is inputted to the flip-flop FF16 to be latched therein on the leading edge of the clock 16CK at the time t_4 .

In a time period from the next time t_4 to the time t_5 , the switching devices SW1 and SW2 are respectively switched to its input terminals b and its input terminals d. The data B is inputted to the input terminals a of the multiplier MPY from the flip-flop FF2 through the switching device SW1. On the other hand, the data E_2 is inputted to the input terminals b of the multiplier MPY from the flip-flop FF10 through the switching device SW2. The multiplier MPY performs an operation of data $B \cdot E_2$ and outputs the results



of the operation. The data $B \cdot E2$ is inputted to the flip-flop FF13 to be latched therein on the leading edge of the clock /10MCK at the time t5.

Furthermore, in the time period from the time t4 to the time t5, the switching devices SW3 and SW4 are respectively switched to its input terminals c and its input terminals b. The data $D \cdot E2$ is inputted to the input terminals a of the adder ADD from the flip-flop FF13 through the switching device SW3. On the other hand, the data y_0 is inputted to the input terminals b of the adder ADD from the flip-flop FF15 through the switching device SW4 and the exclusive OR gate XOR3. At this time, the ADS signal is at the "L" level. Accordingly, the exclusive OR gate XOR3 and the adder ADD perform addition processing in the above described manner and thus, perform an operation of data $E4 = (D \cdot E2) + y_0$ and output the results of the operation. The data E4 is inputted to the flip-flop FF17 to be latched therein on the leading edge of a clock 17CK at the time t5.

In a time period from the next time t5 to the time t6, both the switching devices SW1 and SW2 are switched to their input terminals c. The data C is inputted to the input terminals a of the multiplier MPY from the flip-flop FF3 through the switching device SW1. On the other hand, the data E1 is inputted to the input terminals b of the multiplier MPY from the flip-flop FF9 through the switching device SW2. The multiplier MPY performs an operation of data $C \cdot E1$ and outputs the results of the operation. The data $C \cdot E1$ is inputted to the flip-flop FF13 to be latched therein on the leading edge of the clock /10MCK at the time t6.

Furthermore, in the time period from the time t5 to the time t6, both the switching devices SW3 and SW4 are switched to their input terminals c. The data $B \cdot E2$ is inputted to the input terminals a of the adder ADD from the flip-flop 13 through the switching device SW3. On the other hand, the data E3 is inputted to the input terminals b of the adder ADD from the flip-flop FF16 through the switching device SW4 and the exclusive OR gate XOR3. At this time, the ADS signal is at the "L" level. Accordingly, the exclusive OR gate XOR3 and the adder ADD perform addition processing in the above described manner and thus, perform an operation of data $E5 = (B \cdot E2) + E3$ and output the results of the operation. The data E5 is inputted to the flip-flop FF16 to be latched therein on the leading edge of the clock 16CK at the time t6.

In a time period from the next time t6 to the time t7, both the switching devices SW1 and SW2 are switched to their input terminals b. The data B is inputted to the input terminals a of the multiplier MPY from the flip-flop FF2 through the switching device SW1. On the other hand, the data V_c is inputted to the input terminals b of the multiplier MPY from the flip-flop FF8 through the switching device SW2. The multiplier MPY performs an operation of data $B \cdot V_c$ and outputs the results of the operation. The data $B \cdot V_c$ is inputted to the flip-flop FF13 to be latched therein on the leading edge of the clock /10MCK at the time t7.

Furthermore, in the time period from the time t6 to the time t7, the switching devices SW3 and SW4 are respectively switched to its input terminals c and its input terminals d. The data $C \cdot E1$ is inputted to the input terminals a of the adder ADD from the flip-flop FF13 through the switching device SW3. On the other hand, the data E4 is inputted to the input terminals b of the adder ADD from the flip-flop FF17 through the switching device SW4 and the exclusive OR gate XOR3. At this time, the ADS signal is at the "L" level. Accordingly, the exclusive OR gate XOR3 and the adder ADD perform addition processing in the above described manner and thus, perform an operation of data $E6 = (C \cdot E1) + E4$ and output the results of the operation. The data E6 is inputted to the flip flop FF17 to be latched therein on the leading edge of the clock 17CK at the time t7.

In a time period from the next time t7 to the time t8, the switching device SW1 and SW2 are respectively switched to its input terminals d and its input terminals b. The data D is inputted to the input terminals a of the multiplier MPY from the flip-flop FF4 through the switching device SW1. On the other hand, the data V_c is inputted to the input terminals b of the multiplier MPY from the flip-flop FF8 through the switching device SW2. The multiplier MPY performs an operation of data $D \cdot V_c$ and outputs the results of the operation. The data $D \cdot V_c$ is inputted to the flip-flop FF13 to be latched therein on the leading edge of the clock /10MCK at the time t8.

Additionally, in the time period from the time t7 to the time t8, both the switching devices SW3 and SW4 are switched to their input terminals c. The data $B \cdot V_c$ is inputted to the input terminals a of the adder ADD from the flip-flop 13 through the switching device SW3. On the other hand, the data E5 is inputted to the input terminals b of the adder ADD from the flip-flop FF16 through the switching device SW4 and the exclusive OR gate XOR3. At this time, the ADS signal is at the "L" level. Accordingly, the exclusive OR gate XOR3 and the adder ADD perform addition processing in the above described manner and thus, perform an operation of data $E7 = (B \cdot V_c) + E5$ and output the results of the operation. The data E7 is inputted to the flip-flop FF16 to be latched therein on the leading edge of the clock 16CK at the time t8.

In a time period from the next time t8 to the time t9, both the switching devices SW1 and SW2 are switched to their input terminals a. The data A is inputted to the input terminals a of the multiplier MPY from the flip-flop FF1 through the switching device SW1. On the other hand, the data H_c is inputted to the input



terminals b of the multiplier MPY from the HV counter 31 through the exclusive OR gate XOR1 and the switching device SW2. The multiplier MPY performs an operation of data $A \cdot H_c$ and outputs the results of the operation. The data $A \cdot H_c$ is inputted to the flip-flop FF13 to be latched therein on the leading edge of the clock /10MCK at the time t9.

- 5 Furthermore, in the time period from the time t8 to the time t9, the switching devices SW3 and SW4 are respectively switched to its input terminals c and its input terminals d. The data $D \cdot V_c$ is inputted to the input terminals a of the adder ADD from the flip-flop FF13 through the switching device SW3. On the other hand, the data E6 is inputted to the input terminals b of the adder ADD from the flip-flop FF17 through the switching device SW4 and the exclusive OR gate XOR3. At this time, the ADS signal is at the "L" level.
- 10 Accordingly, the exclusive OR gate XOR3 and the adder ADD perform addition processing in the above described manner and thus, perform an operation of data $E8 = (D \cdot V_c) + E6$ and output the results of the operation. The data E8 is inputted to the flip-flop FF17 to be latched therein on the leading edge of the clock 17CK at the time t9.

The preliminary preprocessing is terminated by the foregoing operations. Consequently, the data E7 is latched by the flip-flop FF16, and the data E8 is latched in the flip-flop FF17.

- Furthermore, in a time period from the time t9 to the time t10, the switching devices SW1 and SW2 are respectively switched to its input terminals c and its input terminals a. The data C is inputted to the input terminals a of the multiplier MPY from the flip-flop FF3 through the switching device SW1. On the other hand, the data H_c is inputted to the input terminals b of the multiplier MPY from the HV counter 31 through the exclusive OR gate XOR1 and the switching device SW2. The multiplier MPY performs an operation of data $C \cdot H_c$ and outputs the results of the operation. The data $C \cdot H_c$ is inputted to the flip-flop FF13 to be latched therein on the leading edge of the clock /10MCK at the time t10.

- 20 Additionally, in the time period from the time t9 to the time t10, both the switching devices SW3 and SW4 are switched to their input terminals c. The data $A \cdot H_c$ is inputted to the input terminals a of the adder ADD from the flip-flop FF13 through the switching device SW3. On the other hand, the data E7 is inputted to the input terminals b of the adder ADD from the flip-flop FF16 through the switching device SW4 and the exclusive OR gate XOR3. At this time, the ADS signal is at the "L" level. Accordingly, the exclusive OR gate XOR3 and the adder ADD perform addition processing of $(A \cdot H_c) + E7$ and output the results of the operation as data x_2 . The data x_2 is inputted to the flip-flop FF19 to be latched therein on the leading edge of the clock /10MCK and then, inputted to the flip-flop FF20 to be latched therein on the leading edge of the clock /5MCK at the time t11.

- In a time period from the next time t10 to the time t11, both the switching devices SW1 and SW2 are switched to their input terminals a. The data A is inputted to the input terminals a of the multiplier MPY from the flip-flop FF1 through the switching device SW1. On the other hand, the data H_c is inputted to the input terminals b of the multiplier MPY from the HV counter 31 through the exclusive OR gate XOR1 and the switching device SW2. The multiplier MPY performs an operation of data $A \cdot H_c$ and outputs the results of the operation. The data $A \cdot H_c$ is inputted to the flip-flop FF13 to be latched therein on the leading edge of the clock /10MCK at the time t11.

- Furthermore, in the time period from the time t10 to the time t11, the switching devices SW3 and SW4 are respectively switched to its input terminals c and its input terminals d. The data $C \cdot H_c$ is inputted to the input terminals a of the adder ADD from the flip-flop FF13 through the switching device SW3. On the other hand, the data E8 is inputted to the input terminals b of the adder ADD from the flip-flop FF17 through the switching device SW4 and the exclusive OR gate XOR3. At this time, the ADS signal is at the "L" level. Accordingly, the exclusive OR gate XOR3 and the adder ADD perform addition processing of $(C \cdot H_c) + E8$ and outputs the results of the operation as data y_2 . The data y_2 is inputted to the flip-flop FF18 to be latched therein on the leading edge of the clock /5MCK at the time t11.

- The data x_2 in the case of $H_c = 0$ is calculated in the above described time period from the time t9 to the time t10, and the data y_2 in the case of $H_c = 0$ is calculated in the time period from the time t10 to the time t11. In a time period after the time t11, the data x_2 and y_2 in a case where the data H_c is 1 to 255 are calculated in the same manner, to calculate the data x_2 and y_2 of one scanning line.

- At the time t11, an AE signal outputted from the timing signal generator 30 falls. On this occasion, the tri-state buffer amplifiers BA1 to BA6 are enabled. Consequently, in a time period from the time t11 to the time t13, an address CAA0 of a total of 16 bits comprising data of the most significant two bits "00" outputted from the tri-state buffer amplifier BA1 and data y_c and x_c of the respective most significant seven bits of the data y_2 (10 bits) and the data x_2 (10 bits) in the case of $H_c = 0$ which are respectively latched in the flip-flops FF18 and FF20 is outputted to the VRAM 7b through the address bus 15b. The VRAM 7b inputs the address CAA0 at the time t13. The data y_d and x_d of the respective least significant three bits of the data y_2 and x_2 in the case of $H_c = 0$ which are respectively latched in the flip-flops FF18 and FF20 are



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latched in the flip-flop FF23 through the flip-flop FF22.

In a time period after the time t13, addresses CAA1 to CAA255 including the data y_c and x_c in a case where the data H_c is 1 to 255 are periodically repeated and outputted to the VRAM 7b through the address bus 15b for each period of the clock /5MCK. Furthermore, the data y_d and x_d corresponding to the
5 respective values of the data H_c are latched in the flip-flop FF23 through the flip-flop FF22 in the above described manner.

The VRAM 7b is responsive to the addresses CAA0 to CAA255 inputted from the background picture address control circuit 24 through the address bus 15b to output 8-bit character codes CA0 to CA255 stored in the respective addresses to the flip-flop FF21 in the background picture address control circuit 24
10 through the data bus 16b for each period of the clock /10MCK. The 8-bit character codes CA0 to CA255 are latched in the flip-flop FF21.

On the other hand, the data y_d and x_d (a total of six bits) corresponding to the character codes are latched in the flip-flop FF23 as described above. Consequently, in a time period from the time t15 to the time t17, a 16-bit address CCA0 comprising data of the most significant two bits "00", a 8-bit character
15 code latched in the flip-flop FF21, and the data y_d and x_d (a total of six bits) in the case of the data $H_c = 0$ is outputted to the VRAM 7a through the tri-state buffer amplifiers BA4 to BA6 and the address bus 15a. The address CCA0 is inputted to the VRAM 7a at the time t17.

In a time period from the time t17 on, the addresses CCA1 to CCA255 in a period during which the data H_c is 1 to 255 are outputted to the VRAM 7a from the background picture address control circuit 24 through
20 the address bus 15a in the same manner.

The VRAM 7a is responsive to the addresses CCA0 to CCA255 inputted from the background picture address control circuit 24 through the address bus 15a to output the 8-bit color data CD0 to CD255 stored in the respective addresses to the background picture data processing circuit 25 through the data bus 16b for each period of the clock /10MCK.

The foregoing rotation processing and enlargement or reduction processing of a background picture with respect to one scanning line are performed with respect to 244 scanning lines of 28 characters, as shown in Fig. 2, thereby to make it possible to achieve the rotation processing and the enlargement or
25 reduction processing of a background picture with respect to one display screen area 41.

As described in the foregoing, the background picture address control circuit 24 calculates the
30 addresses CAA0 to CAA255 in which character codes of a background picture at the time of rotation and enlargement or reduction are stored on the basis of the constant data A, B, C and D for rotation processing and enlargement or reduction processing which are inputted from the CPU2 and outputs the addresses, and outputs, in response to the addresses, the addresses CCA0 to CCA255 each comprising the character code (8 bits) outputted from the VRAM 7b and the data y_d and x_d , thereby to make it possible to output the color
35 data of 8 bits per dot at the time of rotation processing and enlargement or reduction processing to the background picture data processing circuit 25 from the VRAM 7a. Thereafter, the color data (8 bits) of the background picture is latched in the background picture data processing circuit 25 and then, inputted to the priority control circuit 26.

On the other hand, the 7-bit moving picture data is inputted from the moving picture data processing
40 circuit 23 to the priority control circuit 26. The priority control circuit 26 is responsive to the moving picture data so as to determine the priority between the moving picture data and the background picture data on the basis of the 2-bit priority data included in the moving picture data and outputting higher-priority data of the moving picture data and the background picture data to the color signal generator 28. The color generator 28 is responsive to the higher-priority data for converting the moving picture data or the
45 background picture data as inputted into a digital signal of RGB of 5 bits for each color and outputting the digital signal of RGB to the display device 8 and the NTSC encoder 29 on the basis of the count data H_c and V_c applied from the HV counter 31. Consequently, by the foregoing processing, a background picture obtained by rotating and enlarging or reducing the original background picture corresponding to the background picture data stored in the VRAM 7 on the basis of an angle of rotation γ and scaling
50 magnification α and β for the rotation processing and the enlargement or reduction processing which are inputted from the CPU 2 is displayed on the display device 8.

Consequently, in the present embodiment, a three-dimensional background or a background looking as if the road is curved as shown in each of Figs. 12 to 16 can be displayed on the basis of one background picture data for displaying a two-dimensional background picture as shown in, for example, Fig. 11. Further,
55 in a case where the present invention is applied to, for example, a simulation game, if the enlargement or reduction processing is performed while the rotating a background picture as a preferred embodiment, a background looking as if a map viewed from the runway and the air turns while getting away or near when an airplane takes off and lands by displaying the background screen in a three-dimensional manner can be



displayed, thereby to make it possible to further improve the representation of the background picture.

The foregoing will be described in detail. When the original background picture as shown in Fig. 11 is changed into a background picture as shown in Fig. 12, no rotation processing is performed. In this case, it is necessary that the scaling magnification α in the x direction of the parameter A in the equation (10) is increased with lower parts of the screen. In this case, however, no enlargement or reduction processing in the y direction is performed. Accordingly, the scaling magnification β in the y direction of the parameter D in the equation (12) may remain constant.

When the original background picture as shown in Fig. 11 is changed into a background picture as shown in Fig. 13, a scroll offset value H_p in the x direction is changed for each line and enlargement processing in the x direction is performed. In this case, it is necessary that the parameter x_1 in the equation (13) is sequentially altered and the scaling magnification α in the x direction of the parameters A and B in the equations (2) and (3) is increased with lower parts of the screen. In this case, however, no enlargement or reduction processing in the y direction is performed. Accordingly, the scaling magnification β in the y direction of the parameters C and D in the equations (4) and (5) may remain constant.

When the original background picture as shown in Fig. 11 is changed into a background picture as shown in Fig. 14, enlargement processing in the y direction is performed. In this case, it is necessary that the scaling magnification β in the y direction of the parameter D in the equation (12) is increased with lower parts of the screen. In this case, however, no enlargement or reduction processing in the x direction is performed. Accordingly, the scaling magnification α in the x direction of the parameter A in the equation (10) may remain constant.

When the two-dimensional original background picture as shown in Fig. 11 is changed into a three-dimensional background picture as shown in Fig. 15, processing shown in Fig. 13 and processing shown in Fig. 14 are combined. More specifically, in this case, it is necessary that the scaling magnification α in the x direction of the parameter A in the equation (10) is increased with lower parts of the screen and at the same time, the scroll offset value H_p is changed for each line to sequentially alter the parameter x_1 in the equation (13), and the scaling magnification β in the y direction of the parameters C and D in the equations (4) and (5) is increased with lower parts of the screen.

The rotation processing will be concretely described. If it is desired to divide one screen into a plurality of parts (three in Fig. 16) in the vertical direction in one frame period and alternately change to 45° the directions of rotation of parts of the original background picture shown in Fig. 11 as shown in, for example, Fig. 16, it is necessary to switch an angle γ of the parameter A in the equations (2) to (5) for each vertical coordinate position where the screen is to be divided.

Meanwhile, if it is desired to rotate the original background picture shown in Fig. 11 without any modification, the angle γ of the parameter A in the equation (2) and (5) may be gradually changed by a constant value for each frame. In this case, however, the illustration of this state is difficult and thus, is omitted.

As described in the foregoing, an address of the VRAM 7 in a case where the original background picture corresponding to the background picture data stored in the VRAM 7 is rotated and enlarged or reduced is calculated by the background picture address control circuit 24, the color data of the background picture at the time of the rotation processing and the enlargement or reduction processing is read from the VRAM 7 to generate a video signal, and the video signal is displayed on the display device 8. Accordingly, the CPU 2 must only set constants but need not calculate respective positions of a picture which is rotated and enlarged or reduced. Accordingly, the CPU 2 can perform processing of another image or picture. Consequently, the present invention has the advantage that the throughput of the CPU can be improved, as compared with the prior art for rotation processing or enlargement or reduction processing. In addition, an address of image data of a background picture in the VRAM 7 corresponding to the respective positions in the horizontal and vertical directions of the background picture which is rotated and enlarged or reduced is calculated by the background picture address control circuit 24 constituted by hardware such as the switching devices SW1 and SW4, the multiplier MPY and the adder ADD as described above. Accordingly, the rotation processing and the enlargement or reduction processing can be performed at higher speed, as compared with the prior art. Moreover, various circuits in one background picture address control circuit 24 achieve the rotation processing or the enlargement processing or the reduction processing in a time shared manner. Accordingly, the circuit configuration can be simplified and the cost is lowered, as compared with a case where a dedicated circuit is provided for each processing.

Furthermore, since in the picture processing unit 1, an address of image data of a background picture which is rotated and enlarged or reduced is calculated to find background picture data, the original background picture data can be preserved. Consequently, there are no possibilities that computing errors at the time of respective rotations are accumulated as in the conventional example when an image is rotated



once so that a background picture is displayed in a position different from that of the original background picture and the shape of the background picture is changed from that of the original background picture.

Although in the above described embodiments, description was made of the video processing unit 1 for rotating and enlarging or reducing a background picture and displaying the same, the present invention is not limited to the same. For example, the video processing unit may be constructed to perform at least one of rotation processing and enlargement or reduction processing. At this time, the construction of the background picture address control circuit 24 is not changed. The constants α and β calculated by the CPU 2 may be 0 if only the rotation processing is performed, and the constant γ calculated by the CPU 2 may be 0 if only the enlargement or reduction processing is performed.

Furthermore, although in the above embodiment, a description was made of a character type video processing apparatus, the present invention is not limited to the same. It should be noted that the present invention is applicable to a so-called dot map type video processing apparatus for designating an address for each dot to obtain color data using a VRAM having color data corresponding to the VRAM area 40.

Although the present invention has been described and illustrated in detail, it is clearly understood that the same is by way of illustration and example only and is not to be taken by way of limitation, the spirit and scope of the present invention being limited only by the terms of the appended claims.

Claims

1. A video processing apparatus comprising:

storage means for storing image data of a background picture in an address corresponding to a display position of the background picture before rotation processing;

operation means for operating, on the basis of control data for the rotation processing, the address of said storage means corresponding to a display position of the background picture after performing the rotation processing of the background picture;

reading means for reading the image data stored in the address of said storage means which is operated by said operation means; and

video signal generating means for generating a video signal on the basis of the image data read by said reading means.

2. A video processing apparatus comprising:

storage means for storing image data of a background picture in an address corresponding to a display position of the background picture before rotation processing and enlargement or reduction processing;

operation means for operating, on the basis of control data for the rotation processing and the enlargement or reduction processing, the address of said storage means corresponding to a display position of the background picture after performing at least one of the rotation processing and the enlargement or reduction processing of the background picture;

reading means for reading the image data stored in the address of said storage means which is operated by said operation means; and

video signal generating means for generating a video signal on the basis of the image data read by said reading means.

3. The video processing apparatus according to claim 2, wherein said operation means comprises

control data generating means for generating as control data parameter data (A, B, C, D) for rotation and/or enlargement or reduction, center coordinate data (X_0 , Y_0) for rotation and/or enlargement or reduction, and coordinate data (X_1 , Y_1) of the background picture; and

matrix operation means for performing, on the basis of the parameter data (A, B, C, D), the center coordinate data (x_0 , y_0) and the coordinate data (x_1 , y_1) from said control data generating means, a matrix operation expressed by the following equation (where $A = 1/\alpha \cdot \cos \gamma$, $B = 1/\alpha \cdot \sin \gamma$, $C = -1/\beta \cdot \sin \gamma$, and $D = 1/\beta \cdot \cos \gamma$ when α is taken as scaling magnification in the x direction, β is taken as scaling magnification in the y direction and is taken as an angle of rotation, $x_1 = H_p + H_c$ when H_p is taken as offset data in the horizontal direction and H_c is taken as display position data in the horizontal direction, and $y_1 = V_p + V_c$ when V_p is taken as offset data in the vertical direction and V_c is taken as display position data in the vertical direction):



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$$\begin{bmatrix} X_2 \\ Y_2 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} X_1 - X_0 \\ Y_1 - Y_0 \end{bmatrix} + \begin{bmatrix} X_0 \\ Y_0 \end{bmatrix}$$

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4. The video processing apparatus according to claim 3, wherein said video processing apparatus is used for displaying a background picture on a raster scan type display,

said operation means performing preliminary operation processing during the horizontal blanking period of the raster scan type display and performing the remaining operation processing during the horizontal scanning period.

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5. The video processing apparatus according to claim 4, wherein said video processing apparatus is used for displaying a background picture on a raster scan type display,

said storage means including a storage area larger than a storage area corresponding to the display size in the vertical and horizontal directions of the raster scan type display, and

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said control data generating means comprising means for generating data for designating an area to be displayed corresponding to the display size out of image data stored in the storage area larger than the display size.

- 25 6. The video processing apparatus according to claim 4, wherein said operation means comprises means for performing operations expressed by the following equations when parameter data for rotation and/or enlargement or reduction are represented by $A (= 1/\alpha \cdot \cos \gamma)$, $B (= 1/\alpha \cdot \sin \gamma)$, $C (= -1/\beta \cdot \sin \gamma)$ and $D (= 1/\beta \cdot \cos \gamma)$, center coordinate data for rotation and/or enlargement or reduction are represented by (X_0, Y_0) , coordinate data of the background picture are represented by (X_1, Y_1) , $X_1 =$

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$H_p + H_c$ (where H_p is offset data in the horizontal direction and H_c is display position data in the horizontal direction), and $y_1 = V_p + V_c$ (where V_p is offset data in the vertical direction and V_c is display position data in the vertical direction).

Amended Claims

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1. (Amended) A video processing apparatus which displays a still picture on display means having a display screen composed of a plurality of pixels in a horizontal direction and a vertical direction, respectively, comprising:

position data generating means for generating first position data representative of a position in said horizontal direction and said vertical direction on said display screen;

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parameter data applying means for applying parameter data for rotation of said still picture;

position data operation means for operating second position data after performing said rotation on said display screen on the basis of said first position data and said parameter data;

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first storage means for storing character data representative of a plurality of characters each composed of a plurality of pixels;

first reading means for reading said character data from said first storage means on the basis of said second position data operated by said position data operation means;

second storage means for storing color data of respective pixels constituting said character;

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second reading means for reading said color data from said second storage means on the basis of the character data read by said first reading means and said second position data; and

video signal generating means for generating a video signal on the basis of the color data read by said second reading means.

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2. (Amended) A video processing apparatus which displays a still picture on display means having a display screen composed of a plurality of pixels in a horizontal direction and a vertical direction, respectively, comprising:

position data generating means for generating first position data representative of a position in said horizontal direction and said vertical direction on said display screen;



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parameter data applying means for applying parameter data for at least one of rotation, enlargement and reduction of said still picture;

position data operation means for operating second position data after performing said at least one of said rotation, enlargement and reduction on said display screen on the basis of said first position data and said parameter data;

first storage means for storing character data representative of a plurality characters each composed of a plurality of pixels;

first reading means for reading said character data from said first storage means on the basis of said second position data operated by said position data operation means;

second storage means for storing color data of respective pixels constituting said character;

second reading means for reading said color data from said second storage means on the basis of the character data read by said first reading means and said second position data; and

video signal generating means for generating a video signal on the basis of the color data read by said second reading means.

3. (Added) A video processing apparatus in accordance with claim 1 or 2, wherein said first reading means accesses to said first storage means on the basis of a portion of said second position data, and said second reading means accesses to said second storage means on the basis of said character data and a remaining portion of said second position data.

4. (Amended) A video processing apparatus in accordance with claim 2, wherein said parameter data applying means generates parameter data (A, B, C, D), and said position data generating means generates said first position data (x_0, y_0), and

said position data operation means includes center coordinate data generating means for generating center coordinate data (x_0, y_0) for at least one of said rotation, enlargement and reduction, and matrix operation means for performing a matrix operation according to the following equation on the basis of said first position data (x_1, y_1) and said center coordinate data (x_0, y_0) to evaluate said second position data (x_2, y_2) of the pixels after performing at least one of said rotation, enlargement and reduction on said display screen:

$$\begin{bmatrix} X_2 \\ Y_2 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} X_1 - X_0 \\ Y_1 - Y_0 \end{bmatrix} + \begin{bmatrix} X_0 \\ Y_0 \end{bmatrix}$$

wherein, if a scaling factor in said horizontal direction for enlargement or reduction is α , a scaling factor in said vertical direction for enlargement or reduction is β , and an angle to be rotated is γ , said parameter data A, B, C and D are respectively given by the following equations:

$$A = 1/\alpha \cdot \cos \gamma$$

$$B = 1/\alpha \cdot \sin \gamma$$

$$C = -1/\beta \cdot \sin \gamma$$

$$D = 1/\beta \cdot \cos \gamma$$

5. (Added) A video processing apparatus in accordance with claim 3, wherein said first position data generating means generates said first position data (x_1, y_1) represented by $x_1 = H_p + H_c$ and $y_1 = V_p + V_c$ when offset data in said horizontal direction and said vertical direction are H_p and V_p and position data of said pixel in said horizontal direction and said vertical direction are H_c and V_c .

6. (Amended) A video processing apparatus in accordance with claim 4, wherein said display means includes a raster scan display, and said operation means performs a portion of said matrix operation necessary for a next horizontal scanning period of said raster scan display during a horizontal blanking period and performs a remaining portion of said matrix operation during said next horizontal



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scanning period for each pixel.

7. (Added) A video processing apparatus in accordance with claim 6, wherein said first storage means including a storage area larger than a size of said display screen of said raster scan display, and
5 said data generating means includes means for generating data for designating character data of a character to be displayed out of the characters stored in said first storage means.
8. (Added) A video processing apparatus in accordance with claim 5, wherein said operation means operates said second position data (x_2 , y_2) according to the following equations:
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- $$x_2 = A(H_p - x_0) + B(V_p - y_0) + x_0 + A \cdot H_c + B \cdot V_c$$
- $$y_2 = C(H_p - x_0) + D(V_p - y_0) + y_0 + C \cdot H_c + D \cdot V_c$$
9. (Added) A video processing apparatus in accordance with claim 8, wherein said display means includes
15 a raster scan display, said operation means performs terms " $+A \cdot H_c$ " and " $+C \cdot H_c$ " of said equations for each pixel during a horizontal scanning period of said raster scan display, and performs a remaining portion of said equations necessary for said horizontal scanning period during a horizontal blanking period before said horizontal scanning period.
- 20 10. (Added) A video processing apparatus which displays a still picture on a raster scan display having a display screen composed of a plurality of pixels in a horizontal direction and a vertical direction, respectively, comprising:
- storage means for storing an image data of said still picture in an address corresponding to a display position of said still picture;
- 25 matrix operation means for performing a matrix operation for at least one of rotation, enlargement and reduction of said still picture, said matrix operation means performing an operation of a portion of said matrix operation necessary for a next horizontal scanning period of said raster scan display during a horizontal scanning period and an operation of a remaining portion of said matrix operation for each pixel during said next horizontal scanning period;
- 30 reading means for reading said image data from said storage means on the basis of operation results by said matrix operation means; and
- video signal generating means for generating a video signal on the basis of the image data read by said reading means.

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