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PATENT SPECIFICATION

DRAWINGS ATTACHED

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Int. Cl.:—H 01 I 1/14

COMPLETE SPECIFICATION

Improvements in or relating to Semiconductor Devices

We, FAIRCHILD CAMERA AND INSTRUMENT CORPORATION, of 300 Robbins Lane, Syosset, Long Island, New York, United States of America, a corporation organized and existing under the laws of the State of Delaware, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to an integrated circuit and, in particular, to an improved integrated circuit arrangement and a method of forming such a circuit arrangement.

Silicon integrated circuits require external electrical connections to the monolithic chip for the purpose of supplying power, for the purpose of interconnecting a number of circuits together, and for other purposes. To provide for such connections, a number of areas of conductive material (e.g. aluminum film) referred to as pads are associated with each circuit. These pads are usually placed around the perimeter of the circuit components to allow maximum density and flexibility of interconnection of these components. Each pad provides sufficient area so that a conventional lead wire may be connected to it by a common bonding technique, such as ultrasonic bonding or thermocompression bonding.

In the prior art, as stated, the pads have been located outside the area of the circuit components (referred to hereinafter as the "integrated circuit component area"). Such location of the pads substantially increases the total area of the integrated circuit, limiting the maximum component density attainable. The number of circuits that may be batch processed in a single operation by such fabrication equipment as diffusion furnaces and photolithographic masking jigs is, in part, determined by the area of each integrated circuit. Thus, the increase in area of an integrated

circuit attributable to the pad area decidedly limits integrated circuit production output.

The subject invention reduces the area required for an integrated circuit. Briefly, the invention comprises a substrate having a surface; a circuit having a plurality of electrical components and their interconnections located adjacent a major portion of said surface of the substrate; a deposited insulating layer overlying at least a part of said components and said interconnections; and an electrically conductive pad overlying said insulating layer, and directly overlying a circuit component formed within said substrate said conductive pad being connected to at least one of said circuit components and being adapted to being connected to a conductor.

The method of the invention comprises forming a plurality of circuit components in cooperative relationship adjacent a major portion of the surface of a body of semiconductor material within a substrate; forming a first insulating layer over at least a part of said major portion of said surface; forming electrical interconnections upon said first insulating layer between at least two of the components; forming a second insulating layer over at least a portion of one of said interconnections; and forming a conductive pad over said second insulating layer adjacent (i.e., over or above) said major portion of said surface electrically connected to at least one of the circuit components and substantially within the topographical boundary formed by said components and interconnections.

The advantages and details of this invention will now be described in detail with reference to the drawings, wherein:

FIG. 1 is a simplified schematic plan view of a prior art integrated circuit;

FIG. 2 is a simplified plan view of the invented integrated circuit arrangement;

FIG. 3 is a sectional view along lines 3—3 of FIG. 2; and

FIG. 4 is a partial sectional view of a second embodiment of the invention.

Referring to FIG. 1, a prior art integrated circuit 10 is shown, having a plurality of circuit components (such as components 22 in FIG. 3) within the integrated circuit component area 12 defined by broken line 14. The integrated circuit area 12 is a major portion of the surface of substrate 13. The components within area 12 may be resistors, capacitors, transistors, diodes or other well-known electrical, electronic or solid-state components. Outside of the integrated circuit component area 12 and extending to the extremity of the integrated circuit is the pad area 15, wherein a plurality of electrically conductive pads 16 are located. The pads 16 are located around the perimeter of area 12 and are adaptable to being connected to a conductor such as a wire (e.g., aluminum or gold 1-mil diameter); such a pad has an area of about 10 to 20 sq. mils. The pads 16 are connected to various circuit components by thin-film interconnections within the integrated circuit. Typically, in such a prior art arrangement, the pads, along with the interconnections between the components of the circuit, are formed simultaneously atop the insulating layer with the interconnections passing through the insulating layer to electrically contact the various components and elements thereof. The method of forming such connections and interconnections is described in detail in U. S. Patent No. 2,981,877, issued April 25, 1961, to Robert N. Noyce. Such prior art arrangements have the decided disadvantage of requiring a considerable area of integrated circuit 10. As is noted from FIG. 1, the pad area 15 does not contain any underlying circuit components. This area is employed strictly as a support for the pads 16. In some arrangements, the pad area 15 may occupy as much as 40 per cent of integrated circuit 10.

The invented integrated circuit arrangement and method of placing pads minimizes the prior art limitations by arranging the pad area to be substantially overlying the integrated circuit component area. As shown in the integrated circuit 10 of FIG. 2, the pads 16 directly overlie the integrated circuit component area 12. Thus, the special area 15 previously devoted exclusively to pads 16 (FIG. 1) is eliminated and greater overall component density can be attained. In addition, the total surface area of substrate required for a given number of components may be substantially lowered.

A first embodiment of the invention shown in FIG. 3 employs a substrate 20 (e.g., monocrystalline semiconductor material, such as silicon) of a first conductivity type (e.g., n-type) with a component 22 formed therein. The component 22 is a transistor having a first monocrystalline semiconductor base region 24 of a conductivity type opposite that of substrate 20 (e.g., p-type), which serves as the

collector and a second monocrystalline semiconductor emitter region 26 having a conductivity type (e.g., n-type) opposite that of base region 24, whereby junctions 25 and 25a are formed. There is a plurality of such components as well as other components located adjacent a major portion of surface 28 of substrate 20. It is, of course, within the scope of the invention to employ components, such as diodes, field-effect transistors, metal-oxide-silicon devices, resistors, capacitors, inductors and other devices. Similarly, the invention is applicable to hybrid integrated circuits or integrated circuits of the thin-film type. The component 22 is formed by well-known double-diffusion and photo-engraving techniques, such as described in U. S. Patent No. 3,025,589, issued March 20, 1962, to J. A. Hoerni.

On surface 28 of substrate 20 is located a first insulating layer 30, which in the case of a silicon substrate may be a layer of silicon dioxide formed simultaneously or subsequent to the formation of regions 24 and 26. As is well known in the prior art, layer 30 is employed to passivate and protect the component formed in substrate 20 and is employed as an electrical insulating layer. Overlying first insulating layer 30 is a network of conductive material 32 that interconnects the various components of the circuit. This network 32 may be formed by well-known photoengraving and vacuum-deposition techniques, as described in the aforementioned U. S. Patent No. 2,981,877. (According to the prior art, the pads 16 would be formed simultaneously with the formation of the interconnection network 32 and over first insulating layer 30 exterior to the component 22. It is at this point that the invention departs from the prior art teaching.)

In accordance with the invention, a second insulating layer 34 is located over interconnections 32 and first insulating layer 30. The second insulating layer 34 covers the network 32 as well as component 22. The second insulating layer 34 may be fabricated by one of several well-known deposition techniques, from a variety of source materials. Among these are natural and synthetic silicates, refractory metal oxides, mixtures of silica and other metal-oxides (both natural and synthetic), and sintered glasses. These materials may be used as a source for thermal vacuum deposition, sputtering, vapor phase deposition or other well-known film deposition techniques. The resulting layers are suitable for use as insulation between the multi-level metallic conducting films such as pad 16 and interconnection 32. Films deposited from these sources are hard, chemically resistant, etchable, and electrically insulating. Effective deposition of the insulating layer is relatively easy to accomplish.

A hole 36 is formed in second insulating layer 34 and first insulating layer 30 to enable an electrical connection to be made to compo-

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5 nent 22. The forming of such hole may be accomplished by well-known photoengraving and etching techniques. The hole 36 may be formed by two etching operations or a single etching operation. For example, a portion 37 of hole 36 through first insulating layer 30 may be formed by etching prior to the forming of network 32; the portion of a contact 39 passing through first insulating layer 30 can be made at the same time as network 32 is deposited. Following the formation of second insulating layer 34, the remainder of hole 36 through second insulating layer 34 is formed by a second etching step. The contact 39 is then extended atop layer 34 and pad 16 is formed. The pad 16, along with the remaining portion of contact 39, may be formed by vacuum depositing a conductive metal (e.g., aluminum) over surface 38 of second insulating layer 34. Alternatively, hole 36 may be formed through both layers 30 and 34 by a single etching step. The vacuum deposition over surface 38 would then result in hole 36 being substantially filled with conductive material. The geometry of pad 16 is realized by appropriate photoengraving or other metal-forming techniques to remove the excess metal. The fabrication of such electrically ohmic contacts by vacuum-deposition techniques is described in the aforementioned U. S. Patent No. 2,981,877.

The integrated circuit may be connected to another circuit or to an external device by the connector 40 which is connected to pad 16 preferably by soldering, the thermocompression or ultrasonic bonding. Any forces applied to pad 16 should be limited in amount since the application of excessive forces may result in the cracking of insulating layer 34 and may possibly create a short circuit between pad 16 and network 32. It can be seen that pad 16 must have sufficient area to receive a connector wire 40. Typically, area 16 ranges from 10 to 20 sq. mils, while wire 40 has a diameter ranging from 0.5 mil to 2 mils.

As can be seen from FIGS. 2 and 3, an integrated circuit arrangement is provided wherein the special pad area usually associated with integrated circuits is eliminated and substantially all the substrate is employed for components.

An alternative embodiment of the invention is shown in FIG. 4. The substrate 20, components 22 and first insulating layer 30 of this embodiment are substantially the same as those shown in FIG. 3. This embodiment departs from the one shown in FIG. 3 in the manner in which pad 16 is formed. In this embodiment when network 32 is formed, a short section 52 of electroconductive material is simultaneously formed. The section 52 ohmically contacts region 26 and extends over protective layer 30. Insulating layer 34 is then formed as described in connection with the embodiment of FIG. 3 with the exception that a

portion 50 of section 52 remains exposed. Portion 50 may be exposed by depositing the insulating layer 34 through a temporary mask placed over the surface during the deposition or by lifting or etching techniques. Pad 16 may be formed by vacuum-deposition and photoengraving techniques as described above on contact with portion 50, as shown. This results in what may be described as a "folded-over pad" which is separated from network 32 by layer 34.

In summary, this invention eliminates space that was previously wasted (that is, not needed for the components), thereby substantially increasing overall circuit density and effecting a savings in processing costs by increasing the number of devices per wafer. For example, by eliminating 5-mil pads from the edges of a 40-mil square die, the die has reduced to a 30-mil square die. This increases the number of devices per square inch from 625 to 1,112, almost doubling the chip yield with little increase in processing cost.

Although this invention has been disclosed and illustrated with reference to particular applications, the principles involved are susceptible of numerous other applications which will be apparent to persons skilled in the art.

WHAT WE CLAIM IS:—

1. A semiconductor circuit wherein the total area required for a given circuit arrangement is reduced, comprising:

a substrate having a surface;
a circuit having a plurality of electrical components and their interconnections located adjacent a major portion of said surface of the substrate;

a deposited insulating layer overlying at least a part of said components and said interconnections; and

an electrically conductive pad overlying said insulating layer, and directly overlying a circuit component formed within said substrate, said conductive pad being connected to at least one of said circuit components and being adapted to being connected to a conductor.

2. A semiconductor circuit as claimed in Claim 1, wherein said circuit is an integrated circuit and said conductive pad has an area of a sufficient magnitude to have a wire bonded thereto.

3. A semiconductor circuit as claimed in Claim 1, wherein said circuit is a semiconductor integrated circuit and a plurality of pads are spaced around said integrated circuit.

4. A semiconductor circuit as claimed in Claim 3, wherein said plurality of pads are spaced substantially within the bounds of said integrated circuit.

5. A semiconductor circuit as claimed in any of the preceding claims, wherein said semiconductor circuit employs monocrystalline silicon and said insulating layer is silicon dioxide, and said conductive pad is aluminum.

6. A method for forming the integrated cir-



nent 22. The forming of such hole may be accomplished by well-known photoengraving and etching techniques. The hole 36 may be formed by two etching operations or a single etching operation. For example, a portion 37 of hole 36 through first insulating layer 30 may be formed by etching prior to the forming of network 32; the portion of a contact 39 passing through first insulating layer 30 can be made at the same time as network 32 is deposited. Following the formation of second insulating layer 34, the remainder of hole 36 through second insulating layer 34 is formed by a second etching step. The contact 39 is then extended atop layer 34 and pad 16 is formed. The pad 16, along with the remaining portion of contact 39, may be formed by vacuum depositing a conductive metal (e.g., aluminum) over surface 38 of second insulating layer 34. Alternatively, hole 36 may be formed through both layers 30 and 34 by a single etching step. The vacuum deposition over surface 38 would then result in hole 36 being substantially filled with conductive material. The geometry of pad 16 is realized by appropriate photoengraving or other metal-forming techniques to remove the excess metal. The fabrication of such electrically ohmic contacts by vacuum-deposition techniques is described in the aforementioned U. S. Patent No. 2,981,877.

The integrated circuit may be connected to another circuit or to an external device by the connector 40 which is connected to pad 16 preferably by soldering, the thermocompression or ultrasonic bonding. Any forces applied to pad 16 should be limited in amount since the application of excessive forces may result in the cracking of insulating layer 34 and may possibly create a short circuit between pad 16 and network 32. It can be seen that pad 16 must have sufficient area to receive a connector wire 40. Typically, area 16 ranges from 10 to 20 sq. mils, while wire 40 has a diameter ranging from 0.5 mil to 2 mils.

As can be seen from FIGS. 2 and 3, an integrated circuit arrangement is provided wherein the special pad area usually associated with integrated circuits is eliminated and substantially all the substrate is employed for components.

An alternative embodiment of the invention is shown in FIG. 4. The substrate 20, components 22 and first insulating layer 30 of this embodiment are substantially the same as those shown in FIG. 3. This embodiment departs from the one shown in FIG. 3 in the manner in which pad 16 is formed. In this embodiment when network 32 is formed, a short section 52 of electroconductive material is simultaneously formed. The section 52 ohmically contacts region 26 and extends over protective layer 30. Insulating layer 34 is then formed as described in connection with the embodiment of FIG. 3 with the exception that a

portion 50 of section 52 remains exposed. Portion 50 may be exposed by depositing the insulating layer 34 through a temporary mask placed over the surface during the deposition or by lifting or etching techniques. Pad 16 may be formed by vacuum-deposition and photoengraving techniques as described above on contact with portion 50, as shown. This results in what may be described as a "folded-over pad" which is separated from network 32 by layer 34.

In summary, this invention eliminates space that was previously wasted (that is, not needed for the components), thereby substantially increasing overall circuit density and effecting a savings in processing costs by increasing the number of devices per wafer. For example, by eliminating 5-mil pads from the edges of a 40-mil square die, the die has reduced to a 30-mil square die. This increases the number of devices per square inch from 625 to 1,112, almost doubling the chip yield with little increase in processing cost.

Although this invention has been disclosed and illustrated with reference to particular applications, the principles involved are susceptible of numerous other applications which will be apparent to persons skilled in the art.

WHAT WE CLAIM IS:—

1. A semiconductor circuit wherein the total area required for a given circuit arrangement is reduced, comprising:

a substrate having a surface;

a circuit having a plurality of electrical components and their interconnections located adjacent a major portion of said surface of the substrate;

a deposited insulating layer overlying at least a part of said components and said interconnections; and

an electrically conductive pad overlying said insulating layer, and directly overlying a circuit component formed within said substrate, said conductive pad being connected to at least one of said circuit components and being adapted to being connected to a conductor.

2. A semiconductor circuit as claimed in Claim 1, wherein said circuit is an integrated circuit and said conductive pad has an area of a sufficient magnitude to have a wire bonded thereto.

3. A semiconductor circuit as claimed in Claim 1, wherein said circuit is a semiconductor integrated circuit and a plurality of pads are spaced around said integrated circuit.

4. A semiconductor circuit as claimed in Claim 3, wherein said plurality of pads are spaced substantially within the bounds of said integrated circuit.

5. A semiconductor circuit as claimed in any of the preceding claims, wherein said semiconductor circuit employs monocrystalline silicon and said insulating layer is silicon dioxide, and said conductive pad is aluminum.

6. A method for forming the integrated cir-

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- 5 cuit of any of the above claims comprising:
 forming a plurality of circuit components
 in cooperative relationship adjacent a major
 portion of the surface of a body of semi-
10 conductor material within a substrate;
 forming a first insulating layer over at least
 a part of said major portion of said surface;
 forming electrical interconnections upon said
15 first insulating layer between at least two of
 the components;
 forming a second insulating layer over at
 least a portion of one of said interconnections;
 and
 forming a conductive pad over said second
15 insulating layer adjacent said major portion
 of said surface electrically connected to at least

one of the circuit components and substantially
within the topographical boundary formed by
said components and interconnections.

7. An integrated semiconductor circuit sub- 20
stantially as hereinbefore described with refer-
ence to Figs. 2 and 3 or Fig. 4 of the accom-
panying drawings.

8. A method of forming an integrated semi- 25
conductor circuit substantially as hereinbefore
described with reference to Figs. 2 and 3 or
Fig. 4 of the accompanying drawings.

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