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# PATENT SPECIFICATION

DRAWINGS ATTACHED

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## COMPLETE SPECIFICATION

### Electrical Circuits

We, RADIO CORPORATION OF AMERICA, a Corporation organized under the laws of the State of Delaware, United States of America, of 30, Rockefeller Plaza, City and State of New York, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to electrical circuits and in particular to integrated solid state structures, using thin film electrical devices as the active elements, and to electrical switching circuits incorporating such solid state structures.

Bistable multivibrators, or flip-flops, find wide use in digital computers and other apparatus as information storage elements in shift registers, counters and memories, and as control devices and the like. Generally speaking, a flip-flop may include two amplifying devices having their control and output electrodes cross-coupled by means of suitable coupling impedances, and bias means connected to the control electrodes for biasing one device in the "off" state while the other device is concurrently in the "on" state. It is desirable in the interests of reduced space, weight and power dissipation, as well as increased reliability and economy, to simplify the circuit as much as possible by reducing the number of component parts and by fabricating the circuit as an integrated solid state structure.

According to the present invention there is provided an integrated solid state structure comprising a pair of devices, each of said devices having a body portion of semiconductive material and three electrodes, said

electrodes including first and second spaced electrodes each having contact to the body portion and a third electrode connected to said body portion and extending over and insulated from at least a part of said body portion between said first and second spaced electrodes, and means conductively connecting each second electrode of one device to the third electrode of the other device.

According to the present invention there is also provided a switching circuit comprising a pair of semi-conductor devices each having a semiconductive body portion and a source electrode and a drain electrode comprising respectively spaced conductors extending in contact with the respective semiconductive body, and a gate electrode of each device comprising a conductor spaced from the source and drain electrodes thereof and extending over and insulated from a part of said semiconductive body between said source and drain electrodes, the drain electrodes of each device being conductively connected to the gate electrode of the other device and to first points of biasing potential, the source electrodes of said devices being connected to second points of biasing potential different from said first points, and means for changing the potential of each gate electrode to change the electrical conductivity of the respective semiconductor device.

According to the present invention there is further provided a switching circuit comprising a pair of semi-conductor devices each device having a semiconductive body of opposite type conductivity to the type of the body of the other device and each device having a source electrode and a drain electrode comprising respectively spaced conductors

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extending in contact with the respective semiconductor body, and a gate electrode of each device comprising a conductor spaced from the source and drain electrodes thereof and extending over and insulated from a portion of said semiconductor body between said respective source and drain electrodes, the gate electrodes of the devices being conductively connected together and to a first point of biasing potential, the drain and source electrodes of said devices being connected in a series combination across a source of biasing potential, and means for changing the potential of the gate electrodes to change the electrical conductivity of one of the pair of semiconductor devices.

In the accompanying drawing, like reference characters denote like components, and

FIGURE 1 is an energy level diagram useful in explaining the nature of an insulating film in a thin film triode;

FIGURES 2a and 2b are, respectively, a plan of one flip-flop structure according to the invention; and an equivalent circuit diagram of the flip-flop;

FIGURES 3 and 4 are sectional views taken along the lines 3—3 and 4—4, respectively, of FIGURE 2a;

FIGURE 5 is a set of typical characteristic curves for a thin film triode;

FIGURES 6a and 6b are, respectively, a plan and a circuit diagram of another flip-flop structure according to the invention, and an equivalent circuit diagram of the flip-flop;

FIGURE 7 is a cross-sectional view of the flip-flop taken along the line 7—7 of Figure 6a;

FIGURE 8 is a partial plan view of a shift register structure according to the invention;

FIGURE 9 is an equivalent circuit diagram of the shift register of FIGURE 8;

FIGURES 10—13 are views of certain electrical components which may be fabricated by thin film techniques;

FIGURE 14 is another shift register structure according to the invention;

FIGURES 15a and 15b are, respectively, a plan view of another flip-flop structure according to the invention, and an equivalent circuit diagram thereof;

FIGURES 16—18 are sectional views taken along the lines 16—16, 17—17 and 18—18 of Figure 15a;

Figure 19a is a plan of a flip-flop structure according to the invention and which employs four interconnected thin film triodes;

Figure 19b is an equivalent circuit diagram of the flip-flop structure of Figure 19a;

Figures 20—22 are sectional views taken along the lines 20—20, 21—21 and 22—22 of Figure 19a;

Figure 23 is a plan of a shift register

structure according to the invention which employs flip-flops of the type illustrated in Figure 19a; and

Figure 24 is an equivalent circuit diagram of the shift register of Figure 23.

For this invention, advantage is taken of the fact that, in a thin film triode as herein described, the control electrode is separated from the semi-conductive layer by an insulating material having a high resistivity between  $10^6$  and  $10^{18}$  ohm cm., for example, as compared to the semiconductor material having a typical resistivity between 0.1 and  $10^6$  ohm cm. The region of insulating material, which separates the control electrode from the layer of semiconductor material renders the control electrode substantially blocking in both directions. Hence, the control electrode conducts little or no current in either polarity direction. Two such thin film triodes may be cross-coupled with direct connections, preferably of negligible impedance, from the output electrode of the other triode. The flip-flop operates with the expenditure of substantially no current through the cross-coupling in either of its two stable states.

The insulating material may be completely insulating wide-gap semiconductor which exhibits high resistivity. Silicon dioxide, aluminium oxide and calcium fluoride are examples of suitable insulators. Zinc sulphide is an example of a high resistivity semiconductor suitable for use as the insulating material.

An advantage of the invention is that resistors, capacitors and diodes can be fabricated simultaneously with the thin film triodes by the same evaporation techniques. Since many components may be deposited simultaneously, the number of evaporation or deposition operations required for a complete circuit, such as a flip-flop, register, counter and the like increases very slowly or not at all with increasing complexity of the circuit.

A metal electrode insulated from the semiconductor, as may be utilized for the insulated control electrodes of the devices embodying the invention, is illustrated by the energy level diagram of FIGURE 1. Between the metal electrode 10 and the semiconductor 11 there is a region of insulating material 12, that is, a material which has a high resistivity relative to that of the semiconductor, as indicated above. The insulating material selected may have a band-gap which is sufficiently great that the barrier between the insulating material and the semiconductor is too high for charge carriers to be injected from the semiconductor into the conduction band of the insulating material. The insulating material then acts as a potential barrier, and blocks the flow of current from metal to semiconductor, and *vice versa*. No matter

what polarity of gate bias is applied, an insulating film of this type is blocking even though charge carriers may be present in the semiconductor.

5 Referring to FIGURES 2a, 3 and 4, the structure includes an insulating substrate 30, such as a plate of glass, ceramic, fused quartz, or the like, which serves as a support. On the top surface of substrate 30 are two spaced electrodes 32 and 34 which are substantially parallel to one another. One electrode 32 is shorter in extent than the other 34 and is located adjacent to, but spaced sideways from, approximately the lower half of the electrode 34, as viewed in Figure 2a. Electrodes 32 and 34 may consist of metals such as indium, gold or tin, and may be deposited on the substrate 30 as thin films by masking or evaporating techniques. Alternatively, the electrodes may be deposited by a paste containing metallic particles which may be painted or silk screened on the desired portions of the substrate 30. Other techniques, such as sputtering, also may be employed to deposit the electrodes 32, 34 as thin films.

A first thin film of insulating or wide gap material 36 (see FIGURE 4) is deposited on at least a portion of the substrate 30 and the upper half of the electrode 34. This film 36 may consist of one of the insulating materials described previously. For efficient operation, insulating film 36 preferably is less than about two microns thick.

35 A layer of semiconductive material 40 is deposited on the aforesaid top surface of the substrate 30 and covers a portion of the two spaced electrodes 32 and 34 and a portion of the insulating or wide-gap film 36. The upper portion (Figure 2a) of the electrode 34, which is separated from the semiconductor 40 by the insulating film 36 is thus insulated from the semiconductor 40. The insulating material 36 is chosen so that no appreciable current is conducted through the insulating film 36 in either direction between the electrode 34 and the semiconductor 40.

50 The semiconductive material is a crystalline substance which exhibits a periodic potential field, at least on an atomic scale, and may be either monocrystalline or polycrystalline. Suitable materials for the semiconductive layer 40 include elemental semiconductors such as germanium, silicon, and germanium-silicon alloys; group III—V compounds such as the phosphides, arsenides, and antimonides of aluminium, gallium and indium; and group II—VI compounds such as the sulphides, selenides and tellurides of zinc and cadmium. Zinc oxide also may be classed as a group II—VI compound. The electrical resistance of some of the group II—VI compounds is sufficiently high so that these materials may be regarded as in-

ulators rather than semiconductors, and may be used as the material for insulating electrodes from other semiconductors which have a lower resistivity. In particular, the semiconductive layer 40 preferably may be cadmium sulphide which exhibits a periodic potential field, at least on an atomic scale. The insulating film 36 may be silicon dioxide, by way of example, when polycrystalline cadmium sulphide is used as the semiconductor material 40.

A second insulating film 42 is deposited on a portion of the lower half of the semiconductor 40 and covers at least a portion of the gap of separation between the electrodes 32 and 34. A second pair of electrodes 44, 46 then is deposited on top of the structure thus far described. The electrode 46 is shorter than the electrode 44 and is adjacent to, and separated to the right from, approximately the upper half of the electrode 44. The electrode 46 is deposited on the top of the semiconductive layer 40. The upper portion of the electrode 44 also is deposited on the surface of the semiconductive layer 40 and the lower half of this electrode 44 is deposited on top of the second insulating film 42. The second insulating film 42 may be of the same material as the first insulating film 36. Also, the electrodes 44 and 46 may be the same in composition as the other two electrodes 32 and 34.

The insulating films 36 and 42 define regions of insulating material which separate the adjacent portions of electrodes 34 and 44, respectively, from the semiconductive material 40. The term "insulated film" is used herein to define the region of insulating material, however formed.

Electrode 32 and the adjacent spaced portion of the electrode 34, the insulated portion of electrode 44 which is opposite the gap between electrodes 32 and 34, and the semiconductive material 40 between these electrodes constitute a first thin film triode 50 (see FIGURE 3). The separation between the source and drain electrodes 32 and 34 preferably is less than about 100 microns. Advantageously, the gate electrode 44 spans the entire gap or separation between these electrodes 32 and 34, although this is not essential to satisfactory operation.

The upper portions of the electrodes 44 and 34 are the drain and gate electrodes, respectively, of a second thin film triode 52, of which electrode 46 is the source electrode, see FIGURE 4. Accordingly, the drain electrode of each triode is directly connected to the gate electrode of the other triode. The gate electrode of this triode 52 spans the entire gap between the source 42 and drain 44 electrodes thereof.

In the circuit diagram of FIGURE 2b, the same reference numerals as used in FIGURES

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2a, 3 and 4 are used to indicate the corresponding elements.

Although the source and drain electrodes of the triodes 50, 52 are on opposite sides of the semiconductor from the associated gate in FIGURES 2—4, it is also possible to deposit all four electrode strips on the same side of the semiconductor, with a narrow gap between electrodes if desired. The gate ends of the two long strips 34, 44 may be of the same or different metal as the drain ends, but a region of insulating material must be used to separate each gate portion from the semiconductor. An example of a flip-flop structure wherein all of the electrodes are on the same side of the semiconductive layer is illustrated in FIGURE 19a, and will be described later.

The substrate 30 of FIGURE 2a is shown broken away to indicate that the flip-flop, as described, may be a component part of a larger integrated structure, such as a shift register. In the latter event, the drain and source electrodes may be connected to electrodes of adjacent flip-flops by means of thin layer deposition techniques aforementioned. Leads for applying operating potentials to the electrodes may be connected to the electrodes by means of a metallic paste, such as silver paste. In particular, each of the drain electrodes may be connected through a separate resistor (not shown) to a source of biasing potential, and each of the source electrodes may be connected to a point of reference potential, such as circuit ground. The polarity of the operating potential applied to the drain electrodes depends upon whether the semiconductive material 40 is N-type, such as cadmium sulphide, or P-type, such as germanium.

FIGURE 5 is a set of typical operating characteristics for a thin film triode. Drain voltage, relative to source voltage, is plotted along the abscissa, and drain current is plotted along the ordinate. Each characteristic represents a different gate voltage. The set of characteristics in the first quadrant is for an N-type semiconductor, in which case the drain potential is positive relative to the source potential. The set of characteristics in the third quadrant is for the P-type material, in which case the drain potential is made negative relative to the source potential.

Consider by way of example that the semiconductor 40 is an N-type material and the source electrodes are grounded. Operation of the flip-flop may be determined by drawing a load line 56 which intersects the abscissa at a point  $+V_b$ , the drain energizing potential, and which has a slope equal to  $-1/R_l$ , where  $R_l$  is the load impedance. Assume that the voltage at the gate of the first triode 50 is  $+V_g$  volts. The voltage at the drain electrode of this triode 50 then is

$+V_b$  volts. This voltage is applied to the gate electrode of the second triode 52 by way of the direct connection to the drain electrode of triode 50. The characteristic for a gate bias of  $+V_b$  volts intersects the load line at a point corresponding to a drain voltage of  $+V_g$  volts, which is the voltage at the gate electrode of the first triode 50. In the other state of the flip-flop, the voltage at the drain electrode of the second triode 52 and the gate of the first triode 50 is  $+V_b$  volts, and the voltage at the gate of the second triode 52 and the drain of the first triode 50 is  $+V_g$ . Depending upon the type of semiconductive material, the operating potentials may be chosen so that one triode of the flip-flop is nonconductive while the other triode is conductive, relatively speaking, and *vice versa*.

A semiconductive material which has a large number of unfilled traps generally will have a high impedance, and little or no current will flow between source and drain until the voltage at the gate is made more positive than the source voltage for N-type material, or more negative than the source voltage for P-type material. Such a triode is operable only in the current enhancement, or carrier enrichment, mode. However, if the semiconductive material is doped so that the material has a high free charge density with zero gate bias, current will flow between source and drain at zero gate bias. Such a triode may be operated in the current enhancement mode by biasing the gate more positive than the source for N-type material and more negative than the source for P-type material. The triode may also be operated in the current depletion mode by applying gate bias potentials of the opposite polarities to those immediately aforementioned. Regardless of the mode of operation, the gate electrode draws little or no current, whereby direct coupling between stages is permitted, since the insulated gate electrode can be biased either positively or negatively with respect to its source electrode.

It will be understood that the electrodes insulating films and semiconductive material in the other devices to be described hereinafter may be deposited in the same manner as in the devices described above. Also, the materials of which the components are constructed may be the same as described previously.

Referring now to the flip-flop of FIGURES 6(a) and 7, it will be noted that all of the electrodes are shown deposited on the same surface of the layer of semiconductive material. A layer of semiconductive material 60 is deposited on the top surface of a substrate 62. Two strip electrodes 64 and 66 are deposited on top of the semiconductor layer 60, and spaced apart and parallel to one another. A thin film 68 of insulating

material, (not shown in FIGURE 6a in order to avoid confusion) is deposited on the top surface of the semiconductor layer 60 adjacent the electrode 64. The lower portion of a third electrode 70 is deposited on the insulating film parallel to, and spaced from, the lower half of electrode 64. The curved, central part and the upper portion of the electrode 70 are deposited on top of the semiconductor layer 60, with the upper portion parallel to, and spaced from, the electrode 66. A fourth electrode 72, of substantially the same shape as third electrode 70, has an upper or first portion deposited on the insulating film and spaced from electrode 64. The remainder of the fourth electrode 72 is deposited on the top surface of the semiconductor layer 60, with the exception of the point of cross-over with the third electrode 70. A relatively thick layer of insulating material may be interposed between the electrodes 70 and 72 at the cross-over point to provide electrical isolation.

Electrode 64 is a source electrode common to two thin film triodes, designated 76 and 78 in the equivalent circuit diagram of FIGURE 6b. The lower portions of the electrodes 70 and 72 are the gate and drain electrodes  $G_1$ ,  $D_1$ , respectively, of one of the triodes. The upper portions of the electrodes 72 and 70 are the gate and drain electrodes  $G_2$ ,  $D_2$ , respectively, of the other triode. Accordingly, the drain electrode of each triode is directly connected to the gate electrode of the other triode. Electrode 66 serves as a common B+ bus or supply line. The semiconductor material 60 between the B+ electrode 66 and the adjacent segments of electrodes 70 and 72 is resistive and is represented in the equivalent circuit of FIGURE 6b by resistors 80 and 82. For a given semiconductor, the values of these resistors 80 and 82 may be suitably fixed by properly spacing the electrode 66 relative to the adjacent segments of electrodes 70 and 72.

Flip-flop circuits of the present invention lend themselves readily to integration in a large system. For example, two and a half stages of a shift register which employs flip-flops of the FIGURE 6a type is illustrated in plan in FIGURE 8, and its equivalent circuit diagram is illustrated in FIGURE 9. This shift register may also employ components formed as illustrated in FIGURES 10a to 13.

FIGURES 10a and 10b illustrate two methods of forming a resistor by thin film techniques. In FIGURE 10a, a pair of ohmic contacts 90 and 92 are deposited on opposite surfaces of a layer of semiconductive material 94. The resistance of the element is determined by the thickness of the layer of semiconductive material and the areas of the opposed contacts 90, 92. Contacts 90 and 92 may be, for example, tin, indium or gold for a cad-

mium sulphide semiconductor. The resistor according to FIGURE 10b comprises two ohmic contact electrodes 96 and 98 deposited on the same surface of a layer of semiconductive material 100 and spaced apart from one another. The resistance provided thereby is determined by the spacing between the contacts 96, 98, the length of these contacts and the type of semiconductor. A substrate (not shown) may support the structures of FIGURES 10a and 10b. Another known form of thin film resistor (not illustrated) consists of an elongated strip of evaporated metal such as Nichrome (Registered Trade Mark).

FIGURE 11 is a cross-sectional view of thin film capacitor. The capacitor comprises a first ohmic contact 104 deposited on the top surface of a substrate or support 106. A thin, insulating film 108 separates the first ohmic contact 104 from a second ohmic contact 110. The capacitance of the element is determined by the areas of the opposed contacts 104 and 110, the thickness of the insulating film 108 and the dielectric constant of the insulating film.

An insulated cross-over for two contacts 114, 116 may be provided, as illustrated in FIGURE 12, by making the layer of insulating film thick enough so that there is negligible capacitance between the contacts 114 and 116.

A cross-sectional view of a diode is illustrated in FIGURE 13. The diode comprises an ohmic contact 120 deposited on the top surface of the substrate 122. A layer of semiconductive material 124 is deposited on the substrate 122 and covers a portion of the ohmic contact 120. A blocking contact 126 is deposited on top of the semiconductor 124 opposite the portion of the ohmic contact covered by the semiconductive material 124. The blocking contact 126 for a cadmium sulphide semiconductor may be, for example, tellurium.

In FIGURE 8 an interstage coupling resistor is designated by "R", a capacitor is designated by "C" and a diode is designated by "d". The thin film triodes and the drain resistors may be fabricated according to the method described previously in connection with FIGURE 6a. The resistors, capacitors and diodes may be fabricated according to the techniques described above in connection with FIGURES 10-13.

Information stored in the register stages may be read out at connections 140 . . . 144 to the drain electrode  $D_1$ ,  $D_2$  and  $D_3$ . These connections to the drain electrodes may be deposited at the same time as the corresponding drain electrodes. A film of insulating material (not shown) is deposited on top of the B+ bus and interposed between this bus and the electrodes 140 . . . 144. The horizontal portion of the shift pulse bus 145

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is deposited directly on the substrate. The vertical projections 146, 148 from the shift bus are separated from the common source electrode 147 by means of a layer of insulating material (not shown) of sufficient thickness so that there is no capacitive coupling therebetween. These vertical projections 146 and 148 are separated from the metallic electrodes which connect the resistors and associated diodes by a thin layer of insulating material (not shown) having a thickness to provide the desired capacitance.

The FIGURE 8 shift register has the feature that all of the components may be deposited either on the top surface of the semiconductive material (not shown) or on an exposed portion of the substrate, which is advantageous in some applications. For example, connections may be readily made to any of the components, which is not the case when some of the components are located between the substrate and the semiconducting material. One disadvantage of the circuit is that the cross-coupling connections between the drain of one triode and the gate of the other triode in the same flip-flop, and the connections between adjacent stages, are not along straight lines. Moreover, the spacing between adjacent output electrodes 140, 142, and 144 may be greater than desirable in some applications because of the circuit layout. If the shift registers is used, for example, as a scanner for television displayer, it would be desirable to have the output electrodes 140, 142 and 144 located more closely together.

Referring to Figure 14, each of the dashed boxes 160 . . . 164 includes a flip-flop of the type illustrated in FIGURE 2a and described previously. A modified form of this flip-flop also may be used wherein all of the electrodes are deposited on the same surface of the layer of semiconductive material. FIGURE 9 is the equivalent circuit diagram of this shift register, as well as the shift register of FIGURE 8, and components in FIGURE 14 are designated by the same reference characters.

The FIGURE 14 shift register has the advantage that all of the electrodes are strip type and are parallel to one another, admitting of ease in fabrication. Because the interconnecting circuitry comprising the resistors, diodes and input capacitors is located separately from the flip-flops themselves, the flip-flops may be located physically closer to one another than is possible in the embodiment of FIGURE 8. Accordingly, the output electrodes of the individual flip-flops may be spaced more closely together. In FIGURE 14, the circuitry outside the dashed boxes 160 . . . 164 may be deposited directly on the supporting substrate (not shown). Resistors, diodes, capacitors, and cross-overs are

fabricated according to the techniques illustrated in FIGURES 10—13.

FIGURE 15a is another embodiment of a flip-flop according to the present invention. The equivalent circuit of this flip-flop is illustrated in FIGURE 15b. The insulating films are not shown in FIGURE 15a in order to avoid confusion, although these films are illustrated in the cross-sectional views of FIGURES 16—18. In the fabrication of this flip-flop, four electrodes 180, 182, 184, and 186 are deposited on the top surface of a supporting substrate (not shown). The vertical segment of the electrode 186, as viewed in FIGURE 15a, is aligned with the short electrode 184, and the lower left corner of the electrode 180 overlaps the upper right portion of the electrode 184, making physical and electrical contact therewith (FIGURE 17).

An insulating film 190 (FIGURES 17 and 18) is deposited on the lower half of the substrate, as viewed in FIGURE 15a, and overlays the electrode 184 and most of the electrode 186. The free end of the horizontal segment of electrode 186 is not covered by the insulating film 190, in order that an electrical connection may be made between this electrode 186 and an external signal source. A long electrode 192, which extends the length of the structure, has its upper half deposited on the substrate and its lower half deposited on the insulating film 190. A layer of semiconductive material 194 next is deposited on top of the structure thus far described, with the outer ends of the electrodes 180, 182, 186 and 192 left exposed so that connections may be made thereto.

A second insulating film 198 (FIGURES 16 and 17) is deposited on the upper half of the layer of semiconductive material 194. Electrodes 200 and 202 are deposited on top of the second insulating film 198, the electrode 202 and the vertical leg of electrode 200 being aligned and spanning the gap or separation between underlying electrodes 180 and 182. Two other electrodes 204 and 206 are deposited on top of the semiconductive material 194 and positioned so that the underlying electrodes 184 and 186 span the gap between them. The upper left corner of electrode 204, as viewed in the drawing, makes contact with the lower right corner of electrode 202 (FIGURE 17).

The component parts of the thin film triodes shown in the cross-sectional views of FIGURES 16, 17 and 18 are designated by numerical reference characters corresponding to those used in FIGURE 15a, and also are designated by descriptive alphabetic reference characters corresponding to those used in the equivalent circuit of FIGURE 15b. It can be seen in FIGURES 15a and 17 that the drain electrode of each triode is directly connected with negligible resistance

to a gate electrode of the other triode. The resistance of the semiconductive material 194 between the drain electrodes 180, 204 and the common B+ line 192 is symbolized by the resistors 212 and 214, respectively, in FIGURE 15(b).

Note that each of the triodes has two gate electrodes. The first gate electrode  $G_1$  or  $G_2$  is directly connected to the drain electrode  $D_2$  or  $D_1$ , respectively, of the other triode. Input signals for switching the flip-flop from one stable state to the other may be applied at the other gate electrodes  $g_1$  and  $g_2$ .

Another embodiment of a flip-flop structure is illustrated in plan in FIGURES 19a, 20, 21 and 22; and its equivalent circuit is illustrated in FIGURE 19b. In the fabrication of this structure, a first layer of an N-type semiconductive material 250 is deposited on a portion of the lower half of a substrate 252. The semiconductive material may be cadmium sulphide by way of example. A second layer of P-type semiconductive material 254, is deposited on a portion of the upper half of the substrate 252 and separated from said first layer 250. Layer 254 may be, for example, suitably doped lead sulphide.

Two long, parallel strip electrodes 258 and 260 serve the functions of drain and gate electrodes for four thin film triodes 262, 264, 266 and 268. Those portions of the electrodes 258, 260 which serve as gate electrodes, and which are designated  $G_1$ ,  $G_2$ ,  $G_3$  and  $G_4$  in FIGURE 19a, are separated from the associated semiconductive material by an insulating layer 259 which underlies these portions and which may be wider in extent than the electrodes 258, 260 themselves (see FIGURES 20, 21 and 22). Remaining portions of these electrodes 258, 260 serve as drain electrodes and are deposited on the semiconductive materials 250 or 254. The ends of these electrodes 258 and 260 extend beyond the semiconductive material and may be deposited on the substrate 252.

Third and fourth short, metallic electrodes 272 and 274 are deposited on top of the layer of N-type material 250 adjacent those portions of electrodes 260 and 258 designated " $G_1$ " and " $G_2$ ", respectively. Fifth and sixth short, metallic electrodes 276 and 278 are deposited on top of the layer of P-type semiconductive material 254 adjacent the portions of electrodes 258 and 260 which are designated " $G_3$ " and " $G_4$ ", respectively. The latter four electrodes 272 . . . 278 are source electrodes for the thin film triodes 262, 264, 266 and 268, respectively (FIGURE 19b, and are designated  $S_1$ ,  $S_2$ ,  $S_3$  and  $S_4$ ).

Besides its ease of fabrication, a flip-flop of the type illustrated in FIGURE 19 has the advantage that it will remain in a quiescent steady state without any appreciable drawing current when the semiconductive materials

250 and 254 are doped so that the triodes 262, 264, 266 and 268 can operate only in the enhancement mode. Triodes 262 and 264 may be considered the cross-coupled active devices of the flip-flop. Triodes 266 and 268 operate as variable impedance elements serving the function of the load resistors, in the basic flip-flop circuits and enhance the operation of the flip-flop in a manner to be described.

It will be recalled from the description of FIGURE 5 that a semiconductive material which has a large number of unfilled traps at zero gate-to-source bias has a high impedance between source and drain. When the gate is made more positive in potential than the source, for N-type material, electrons are drawn into the semiconductive material, and the impedance between source and drain is lowered. If the semiconductor is P-type, holes are drawn into the material when the gate voltage is made negative with respect to the source of voltage. The gate-to-source voltage differential at which substantial filling of traps, and consequent lowering of impedance, occurs, is a function of the doping and can be controlled. Moreover, the impedance between source and drain for a given material is a function of the gate bias and does not depend upon continuous current flow between the source and drain electrodes. In this sense, the triode acts somewhat as a switch with the metallic electrode functioning to open and close the switch by controlling the conductivity of the path between source and drain.

Consider now the operation of the flip-flop and assume that the source electrodes of triodes 262 and 264 are grounded, and that the source of electrodes of triodes 266 and 268 are connected directly to a voltage supply of +5 volts. Assume further that the impedance between source and drain of a triode remains very high until the gate-to-source voltage differential exceeds one volt. Initially, the triode 262 may be in the low impedance state by virtue of having been so triggered from an external source. The impedance between source  $S_1$  and drain  $D_1$  then is low and the drain  $D_1$  voltage may be +1 volt. This voltage applied at the gate  $G_2$  of triode 264 is insufficient to lower the impedance appreciably between source  $S_2$  and drain  $D_2$ .

The impedance between the drain  $D_3$  and source  $S_3$  drops to the low value because the gate  $G_3$  is 4 volts negative relative to the source  $S_3$ . (The semiconductor material of triode 266 is P-type). Accordingly, the voltage drop between source  $S_3$  and drain  $D_3$  may be only about 1 volt, whereby the drain  $D_3$  voltage is +4 volts. This voltage applied at the gate  $G_1$  of triode 262 keeps this triode in a state of low impedance. The +4 volts

applied at the gate  $G_4$  of triode 268, however, results in a voltage differential of only one volt between source  $S_1$  and gate  $G_4$ . Accordingly, the impedance between source  $S_1$  and gate  $G_4$  is high.

In summary, triodes 262 and 266 are in their low impedance states, and the triodes 264 and 268 are in their high impedance states. The only paths for current flow through the triodes 262 and 266 are through the drain-source paths of triodes 268 and 264, respectively. Because of the high impedances of these paths, little or no current flows through the triodes 262 and 266, and the steady state power dissipation is very low. The flip-flop may be switched to its other stable state by applying a positive voltage signal at the gate  $G_3$  of triode 264, for example. All of the triodes 262, 264, 266 and 268 then reverse states.

FIGURE 23 is a plan of four stages of an evaporated, integrated shift register, each stage of which employs a flip-flop of the type illustrated in FIGURE 19. FIGURE 24 is an equivalent circuit diagram of the four stages. In FIGURE 23 resistors, capacitors and diodes are denoted by the letters "R", "C", and "D", respectively, with numerical subscripts corresponding to the reference characters of FIGURE 24. In both FIGURES 23 and 24 the 280 indicates a common B+ line, 282 a common ground line, and 284 a shift pulse bus. All of these components and the cross-overs of connecting lines may be fabricated in the manner illustrated in FIGURES 10—13 and described previously. The entire structure is supported on a substrate 290.

The semiconductive materials 292 and 294 of each flip-flop are deposited on the top surface of the substrate 290. The N-type semiconductor 292 and the P-type semiconductor for the left-most flip-flop only are outlined in FIGURE 23. The pattern of semiconductive materials is the same for the other flip-flops. It will be noted that the semiconductive material extends only a portion of the way across the width of the source S and drain D electrodes. This allows close spacing of the electrodes in a horizontal direction, while assuring that there is no coupling between the drain D electrode of one stage and the source S electrode of the next adjacent stage,  $D_1$  and  $S_2$  for example. A region of insulating material is interposed between each of the gate G electrodes and the semiconductive material, as shown in FIGURES 20—22.

It is to be noted that all critical gaps in the layout arrangement of FIGURE 23 are parallel to the output electrodes 296, 298, 300 and 302, thus permitting easy construction using a masking wire technique. Such a masking wire technique involves utilizing a stretched untwisted wire mounted on a frame

as an evaporation mask to form the gap between the two spaced electrodes. Imparting relative motion between the frame and the electrode supports transversely to the gap between the spaced electrodes and parallel to the plane of the major face for a distance less than the diameter of the wire. Repeating the evaporation of the metallic electrodes enables one to make the gaps between such electrodes less than the diameter of the wire and less than 100 microns. Geometrical layouts which permit at critical dimensions of the pattern to be determined by parallel masking wires in an evaporator yield a compact evaporated circuit. Extreme compactness is desirable in applications such as shift registers, memory arrays and scanning circuits for solid state television pickup and display pansl. The flip-flops of FIGURES 19a and 23 are particularly well adapted to thin film triode construction in which all of the electrodes are located on the same surface of the semiconductive material.

#### WHAT WE CLAIM IS:—

1. An integrated solid state structure comprising a pair of devices, each of said devices having a body portion of semiconductive material and three electrodes, said electrodes including first and second spaced electrodes each having contact to the body portion and a third electrode connected to said body portion and extending over and insulated from at least a part of said body portion between said first and second spaced electrodes, and means conductively connecting each second electrode of one device to the third electrode of the other device.

2. A structure according to Claim 1, wherein the second electrode of the one device and the third electrode of the other device are formed by a first continuous conductive strip extending over said body portions and closely spaced from the first electrodes of the pair of devices.

3. A structure according to Claim 2, wherein the third electrode of said one device and the second electrode of said other device are formed by a second continuous conductive strip extending over said body portions and closely spaced from the first continuous strip and said first electrodes.

4. A structure according to Claim 3, wherein the first electrodes of said pair of devices are each formed by a conductive strip portion extending over the respective body portion in substantially the same direction as and closely spaced respectively from said first and second continuous conductive strips.

5. A structure according to Claim 4, wherein the conductive strip portions forming respectively the first electrodes of said devices comprise a third continuous strip.

6. A structure according to Claim 4, wherein the first and second conductive strips comprising the second and third electrodes

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applied at the gate  $G_1$  of triode 268, however, results in a voltage differential of only one volt between source  $S_1$  and gate  $G_1$ . Accordingly, the impedance between source  $S_1$  and gate  $G_1$  is high.

In summary, triodes 262 and 266 are in their low impedance states, and the triodes 264 and 268 are in their high impedance states. The only paths for current flow through the triodes 262 and 266 are through the drain-source paths of triodes 268 and 264, respectively. Because of the high impedances of these paths, little or no current flows through the triodes 262 and 266, and the steady state power dissipation is very low. The flip-flop may be switched to its other stable state by applying a positive voltage signal at the gate  $G_2$  of triode 264, for example. All of the triodes 262, 264, 266 and 268 then reverse states.

FIGURE 23 is a plan of four stages of an evaporated, integrated shift register, each stage of which employs a flip-flop of the type illustrated in FIGURE 19. FIGURE 24 is an equivalent circuit diagram of the four stages. In FIGURE 23 resistors, capacitors and diodes are denoted by the letters "R", "C", and "D", respectively, with numerical subscripts corresponding to the reference characters of FIGURE 24. In both FIGURES 23 and 24 the 280 indicates a common B+ line, 282 a common ground line, and 284 a shift pulse bus. All of these components and the cross-overs of connecting lines may be fabricated in the manner illustrated in FIGURES 10-13 and described previously. The entire structure is supported on a substrate 290.

The semiconductive materials 292 and 294 of each flip-flop are deposited on the top surface of the substrate 290. The N-type semiconductor 292 and the P-type semiconductor for the left-most flip-flop only are outlined in FIGURE 23. The pattern of semiconductive materials is the same for the other flip-flops. It will be noted that the semiconductive material extends only a portion of the way across the width of the source S and drain D electrodes. This allows close spacing of the electrodes in a horizontal direction, while assuring that there is no coupling between the drain D electrode of one stage and the source S electrode of the next adjacent stage,  $D_1$  and  $S_2$  for example. A region of insulating material is interposed between each of the gate G electrodes and the semiconductive material, as shown in FIGURES 20-22.

It is to be noted that all critical gaps in the layout arrangement of FIGURE 23 are parallel to the output electrodes 296, 298, 300 and 302, thus permitting easy construction using a masking wire technique. Such a masking wire technique involves utilizing a stretched untwisted wire mounted on a frame

as an evaporation mask to form the gap between the two spaced electrodes. Imparting relative motion between the frame and the electrode supports transversely to the gap between the spaced electrodes and parallel to the plane of the major face for a distance less than the diameter of the wire. Repeating the evaporation of the metallic electrodes enables one to make the gaps between such electrodes less than the diameter of the wire and less than 100 microns. Geometrical layouts which permit all critical dimensions of the pattern to be determined by parallel masking wires in an evaporator yield a compact evaporated circuit. Extreme compactness is desirable in applications such as shift registers, memory arrays and scanning circuits for solid state television pickup and display panels. The flip-flops of FIGURES 19a and 23 are particularly well adapted to thin film triode construction in which all of the electrodes are located on the same surface of the semiconductive material.

#### WHAT WE CLAIM IS:—

1. An integrated solid state structure comprising a pair of devices, each of said devices having a body portion of semiconductive material and three electrodes, said electrodes including first and second spaced electrodes each having contact to the body portion and a third electrode connected to said body portion and extending over and insulated from at least a part of said body portion between said first and second spaced electrodes, and means conductively connecting each second electrode of one device to the third electrode of the other device.

2. A structure according to Claim 1, wherein the second electrode of the one device and the third electrode of the other device are formed by a first continuous conductive strip extending over said body portions and closely spaced from the first electrodes of the pair of devices.

3. A structure according to Claim 2, wherein the third electrode of said one device and the second electrode of said other device are formed by a second continuous conductive strip extending over said body portions and closely spaced from the first continuous strip and said first electrodes.

4. A structure according to Claim 3, wherein the first electrodes of said pair of devices are each formed by a conductive strip portion extending over the respective body portion in substantially the same direction as and closely spaced respectively from said first and second continuous conductive strips.

5. A structure according to Claim 4, wherein the conductive strip portions forming respectively the first electrodes of said devices comprise a third continuous strip.

6. A structure according to Claim 4, wherein the first and second conductive strips comprising the second and third electrodes





of said devices and the conductive strip portions comprising the first electrodes of the devices are formed on the same surface of said semiconductive body portions and extend in substantially parallel directions.

7. A structure according to Claim 6, wherein the first and second conductive strips extend across and are insulated from each other between the portions thereof comprising the second and third electrodes respectively of each device.

8. A structure according to Claim 4, wherein the body portions are formed as a single thin semiconductive film deposited on a supporting substrate and said first and second conductive strips are formed respectively on opposite surfaces of said thin semiconductive film and are separated from each other along their lengths by the semiconductive film and an electrically insulating film.

9. A switching circuit comprising a pair of semiconductor devices each having a semiconductive body portion and a source electrode and a drain electrode comprising respectively spaced conductors extending in contact with the respective semiconductive body portion, and a gate electrode of each device comprising a conductor spaced from the source and drain electrodes thereof and separated by insulation from a part of said semiconductive body portion between said source and drain electrodes, the drain electrode of each device being conductively connected to the gate electrode of the other device and to first points of biasing potential, the source electrodes of said devices being connected to second points of biasing potential different from said first points, and means for changing the potential of each gate electrode to change the electrical conductivity of the respective semiconductor device.

10. A switching circuit according to Claim 9, wherein the drain electrode of one device and the gate electrode of the other device are formed by a first continuous conductive strip extending across the body portions and the gate electrode of said one device and the drain electrode of said other device are formed by a second continuous conductive strip extending across the body portions and closely spaced from the first continuous strip, and the source electrodes of said pair of devices are each formed respectively by conductive strip portions extending in substantially the same direction as and closely spaced respectively from said first and second continuous conductive strips.

11. A switching circuit according to Claim 10, wherein said first or second continuous conductive strip is connected to a first point of biasing potential through a load resistor for the circuit comprising a resistive film portion.

12. A switching circuit according to Claim

11, wherein said load resistor comprises a resistive part of the semiconductive body portions.

13. A switching circuit according to Claim 10, wherein said semiconductive body portions of both devices constitute a single body and said first and second conductive strips are respectively connected through different load resistors to the first points of biasing potential which include a third conductive strip formed on said semiconductive body and having portions closely spaced by said semiconductive body respectively from said first and second conductive strips to form the respective load resistors.

14. A switching circuit according to Claim 10, wherein said semiconductive body portions of both devices constitute a single body and said first and second conductive strips extend along a surface of said body, and said means for changing the potential of each gate electrode includes another conductive strip on said semiconductive layer and having portions extending across said first and second strips and respectively separated therefrom by insulating material to form capacitive couplings respectively between said first and second strips and said potential changing means.

15. A switching circuit according to Claim 9, wherein the drain electrode of each device connected to the gate electrode of the other device is connected through a different load resistor to the first points of biasing potential, and wherein said devices comprise a first pair of semiconductor devices the semiconductive body portions whereof are of an N-type material, and wherein said load resistors comprise a second pair of semiconductor devices each formed of a P-type semiconductive body portion and each having a source electrode and a drain electrode comprising respectively spaced conductors in contact with the respective P-type semiconductive body portions, a gate electrode of each one of said second pair of devices comprising a conductor spaced respectively from the source and drain electrodes thereof and extending over and insulated from a part of said P-type semiconductive body portion between said respective source and drain electrodes, the drain electrode of each one of said second pair of semiconductive devices being conductively interconnected to the gate electrode of the other one of said second pair of devices and to the gate electrode of one of said first pair of devices, and the drain electrode of the other one of said first pair of devices, each device of said first pair of devices being connected in series with a different one of the devices of said second pair of devices across a source of biasing potential.

16. A switching circuit according to Claim 15, wherein the interconnected gate and drain electrodes of the first and second pair of

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semiconductive devices are formed respectively as a pair of continuous conductive strips each extending over the respective P- and N-type semiconductive body portions and are closely spaced from the respective source electrodes.

17. A switching circuit according to Claim 16, wherein the source electrodes of said first and second pair of devices are each formed respectively as a conductive film portion closely spaced from said pair of continuous conductive strips, with the conductive film portions forming the source electrodes of the first pair of devices connected to a terminal of said source of biasing potential and the conductive film portions forming the source electrodes of the second pair of devices connected to a second terminal of said source of biasing potential positive to said first terminal.

18. A switching circuit according to Claim 16 or Claim 17, wherein said first and second pairs of semiconductive devices constitute a first stage of said switching circuit and wherein a third pair of semiconductive devices identical to said first pair of devices and a fourth pair of semiconductive devices identical to said second pair of devices form a second stage of said circuit, the source electrodes of said first and third pairs of devices being connected to a first common source of biasing potential and the source electrodes of said second and fourth pairs of devices being connected to a second common source of potential positive to said first common source of potential, and wherein said continuous conductive strips form a first and second pair of conductive strips, wherein each one of the first pair of conductive strips constitutes the drain electrode of one of said first pair of semiconductor devices, the gate electrode of the other one of said first pair of devices, the gate electrode of one of said second pair of device and the drain electrode of the other one of said second pair of devices, and each one of the second pair of conductive strips constitutes the drain electrode of one of said third pair of semiconductor devices, the gate electrode of the other one of said third pair of devices, the gate electrode of one of said fourth pair of devices and the drain electrode of the other one of said fourth pair of devices.

19. A switching circuit according to Claim 9, wherein the drain electrode of each of the pair of devices and the gate electrode of the other one of the devices are connected together through load resistors respectively to a common point of biasing potential.

20. A switching circuit according to Claim 19, wherein at least one of the load resistors comprises a third semiconductor device having a semiconductive body of opposite type conductivity than that of the pair of devices and including a source and a drain electrode comprising spaced conductors in contact with the semiconductive body thereof and a gate electrode spaced from the source and drain electrodes and over and insulated from a portion of the semiconductive body of the third device between the source and drain electrodes thereof.

21. A switching circuit comprising a pair of semiconductor devices each device having a semiconductive body of opposite type conductivity to the type of the body of the other device and each device having a source electrode and a drain electrode comprising respectively spaced conductors extending in contact with the respective semiconductor body, and a gate electrode of each device comprising a conductor spaced from the source and drain electrodes thereof and extending over and insulated from a portion of said semiconductive body between said respective source and drain electrodes, the gate electrodes of the devices being conductively connected together and to a first point of biasing potential, the drain and source electrodes of said devices being connected in a series combination across a source of biasing potential, and means for changing the potential of the gate electrodes to change the electrical conductivity of one of the pair of semiconductor devices.

22. A switching circuit according to Claim 21, wherein said means for changing the potential of the gate electrodes includes a source of input signals, and output signals can be obtained from a point between the pair of devices upon the change in conductivity of one of the devices.

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