

LED driver and method for driving an LED

BACKGROUND

[0001] The present invention relates to an LED (Light Emitting Diode) driver, as well as to a method for operating the same.

[0002] LED light sources are more energy efficient than many other types of light sources, such as halogen or incandescent light sources. During recent years, sales of LED light sources have therefore seen an increase. Concurrently, many resources have been put into the further development of the LED light sources themselves, as well as development of various ways of providing electric energy to LED light sources.

[0003] Normally, an LED light source is driven using a low DC voltage, such as a 12 V or 24 V DC voltage, the voltage being provided by a so-called LED driver. In order to control the luminous intensity of the LED light source, LED drivers usually control the power delivered to the LED light source by either controlling the voltage while keeping the current constant, or by controlling the current while keeping the voltage constant.

[0004] LED light sources are generally dimmable across a relatively broad spectrum of light intensities. However, it has proved difficult to provide an LED driver being able to dim LED light sources across very broad dimming intervals, such as all the way to complete darkness.

[0005] In particular, it is difficult to dim LED light sources across broad dimming intervals without taking into consideration the individual dimming behavior of LED light sources to be dimmed. It would be desirable to provide an LED driver that provides adequate dimming across broad dimming intervals for many different types of LED light sources.

[0006] Allowing a conventional LED driver to dim across such broad dimming intervals, it has been found that one or more of the following problems can occur: flickering light; disturbing sounds; increased wear on electric components; noticeable dimming steps and/or color shifts at low dimming powers; cable crosstalk; uneven or unpredictable lighting levels at different dimming settings and along a strip of LEDs (a "LED strip"); and high peak current requirements.

[0007] Some of these problems may be partly or completely overcome by selecting expensive or short-lived components.

[0008] Hence, it would be desirable to provide a low-cost LED driver having a long useful life and that avoids one or more of the above-mentioned problems.

BRIEF SUMMARY

[0009] The invention relates to an LED, Light Emitting Diode, driver.

[0010] The LED driver can comprise a binary control signal source, arranged to provide a binary control signal as a square wave, the binary control signal having a control signal pattern that is repeated over time to form the binary control signal, the control signal pattern at each time having an instantaneous time-averaged value as time-averaged over the control signal pattern used at the time in question.

[0011] The LED driver can comprise a first-channel electric driver output, arranged to provide a drive current based on the binary control signal to drive an LED.

[0012] The LED driver can comprise a power transistor, having a power transistor control terminal and a pair of different terminals, one of the pair of different terminals being connected to the first-channel electric driver output.

[0013] The LED driver can comprise a drive circuitry, connected to the power transistor control terminal.

[0014] The drive circuitry can comprise a switch, arranged to provide an electric coupling between the power transistor control terminal to either a low voltage or a high voltage in dependence of an instantaneous low value or high value of the binary control signal.

[0015] The drive circuitry being arranged to receive or produce a level signal, the level signal being provided as an increasing or decreasing function of an increase in the instantaneous time-averaged value or as an increasing or decreasing function of an increase in a control signal in turn being correlated with the instantaneous time-averaged value.

[0016] The drive circuitry can further comprise a variable resistance part, arranged to provide a variable resistance along the electric coupling, the variable resistance varying as a function of the level signal, resulting in that an increase in the instantaneous time-averaged value results in an increase in an instantaneous current flowing to or from the power transistor control terminal.

[0017] In some embodiments, the drive circuitry comprises a signal averaging part, arranged to provide the level signal to be, or to correspond to, the instantaneous time-averaged value or to the inverse of the instantaneous time-averaged value.

[0018] In some embodiments, the signal averaging part comprises a low-pass filter or a digital to analog converting circuitry, arranged to provide the level signal as a smoothed and/or time-averaged version of the binary control signal, or to provide the level signal as a smoothed and/or time-averaged signal calculated based on the binary control signal, wherein a value of the level signal at a particular time is determined to correspond to a general level of the binary control signal at the same particular time.

[0019] In some embodiments, the level signal is a current or voltage corresponding to the instantaneous time-averaged value.

[0020] In some embodiments, the power transistor is a FET (Field-Effect Transistor).

[0021] In some embodiments, the switch comprises a switch transistor, having a gate/base terminal, a source/emitter terminal and a drain/collector terminal, the gate/base terminal of the switch transistor being connected to the binary control signal in the form of a voltage or current varying according to the value of the binary control signal.

[0022] In some embodiments, the switch comprises two switch transistors, a gate/base terminal of each being connected to the binary control signal in the form of a voltage or current varying according to the value of the binary control signal, the two switch transistors together providing a push/pull circuit.

[0023] In some embodiments, the two switch transistors are arranged between two different voltage potentials.

[0024] In some embodiments, the power transistor control terminal is coupled to a point between the two switch transistors.

[0025] In some embodiments, the switch transistor is a FET or a BJT (Bipolar Junction Transistor).

[0026] In some embodiments, the variable resistance part comprises a current-throttling part, arranged to throttle the current that can pass through the electric coupling and therefore limiting a rise-speed and/or fall-speed of an electric signal provided from the power transistor to the drive output as the switch switches the electric coupling between the low voltage and the high voltage.

[0027] In some embodiments, the variable resistance part comprises a current-controlling transistor, in turn comprising a current-controlling gate/base terminal, a current-controlling source/emitter terminal and a current-controlling drain/collector terminal.

[0028] In some embodiments, a current flowing through the electric coupling flows across the current-controlling transistor, via the current-controlling source/emitter terminal and the current-controlling drain/collector terminal.

[0029] In some embodiments, the level signal is coupled to the current-controlling gate/base terminal so that an increase in the instantaneous time-averaged value results in a higher instantaneous current across the current-controlling source/emitter terminal and the current-controlling drain/collector terminal.

[0030] In some embodiments, the current-controlling transistor is a BJT.

[0031] In some embodiments, the current-controlling transistor is series-connected to a first current-controlling resistor along the electric coupling.

[0032] In some embodiments, the variable resistance part comprises a first current-controlling transistor, connected so that a current flowing through the electric coupling between the first switch transistor and the power transistor control terminal passes through the first current-controlling transistor.

[0033] In some embodiments, the variable resistance part comprises a second current-controlling transistor, connected so that a current flowing through the electric coupling between the second switch transistor and the power transistor control terminal passes through the second current-controlling transistor.

[0034] In some embodiments, the binary control signal source is arranged to produce the binary control signal in response to an LED dimming value by varying both a pulse width and a number of pulses over the control signal pattern.

[0035] In some embodiments, the binary control signal source is arranged to produce the binary control signal in response to the LED dimming value by, when the LED dimming value increases, widening a pulse of the control signal pattern before increasing the number of pulses in the control signal pattern.

[0036] The invention also relates to a method for driving an LED, comprising providing, to a driver output of the LED driver being connected to the LED, electric power, in turn causing the binary control source to provide the binary control signal and the power transistor to provide the drive current to the driver output.

[0037] In some embodiments, the method further comprises adjusting the binary control signal, thereby modifying the instantaneous time-averaged value.

[0038] In some embodiments, the method further comprises adjusting a dimming state of the LED driver; and mapping the adjusting of the dimming state to a corresponding adjustment of the binary control signal.

[0039] The invention also relates to a method for configuring an LED, Light Emitting Diode, driver for dimming of an LED, the LED driver being arranged to provide a variable current to the LED, a time-average of the variable current corresponding to a dimming value, the variable current being modulated, using a transistor of the LED driver, based on a binary control signal, the binary control signal having a control signal pattern that is repeated over time to form the binary control signal, the control signal pattern at each time having an instantaneous time-averaged value as time-averaged over the control signal pattern; used at the time in question, the method comprising the steps providing, to a LED or a different load in turn being connected to the LED driver, the variable current with several different instantaneous time-averaged values for the binary control signal; obtaining, for each of the several different instantaneous time-averaged values, a respective measurement value of a quantity in turn being or being related to at least one of, firstly, an average current flowing through the LED or the load, and, secondly, an average light intensity emitted by the LED, thereby obtaining a measured first relationship of the absolute or relative current/light intensity as a function of the instantaneous time-averaged value; based on the first relationship, determining configuration information regarding a mapping of each of several different absolute or relative current/light intensity values to a corresponding value for the instantaneous time-averaged value; and storing the configuration information.

[0040] In some embodiments, the relative current and/or light intensity is relative to a maximum current or light intensity, respectively.

[0041] In some embodiments, the method further comprises identifying a second relationship between the instantaneous time-averaged value and the absolute or relative current/light

intensity; identifying a parametric model of the second relationship, the parametric model comprising one or several at least section-wise continuous functions determined by a set of parameters, the parametric model being useful for determining the mapping of each of the several different absolute or relative current/light intensity values to a corresponding instantaneous time-averaged value ; and determining values of the parameters that provide a fit of the at least one functions to the second relationship, the second relationship being evaluated for each of the measurement values and corresponding instantaneous time-averaged values.

[0042] In some embodiments, the configuration information comprises the parameter values.

[0043] In some embodiments, the second relationship comprises the quote or inverse quote of $\frac{g(x)}{g(y)}$, wherein g is a function that is non-constant with respect to x ; x is the instantaneous time-averaged value; and y is the absolute or relative current/light intensity.

[0044] In some embodiments, the one or several functions comprises at least one polynomial of degree 1 or higher.

[0045] In some embodiments, the one or several functions comprises one polynomial of degree 2 or higher.

[0046] In some embodiments, the one or several functions comprises two polynomials of degree 1 or higher that are interconnected by multiplication with a sigmoid function.

[0047] In some embodiments, the one or several functions are defined in terms of a function $f(y)$ where an absolute value of a first derivative of $f(y)$ with respect to y , in other words $|f'(y)|$, is decreasing, wherein y is the absolute or relative current/light intensity.

[0048] In some embodiments, the one or several functions comprises a function defined in terms of two different polynomials and a sigmoid function multiplying together the two polynomials.

[0049] In some embodiments, the two polynomials are selected to approximate, by selection of the parameter values, a general shape of the second relationship on either side of a local minimum or maximum thereof.

[0050] In some embodiments, the sigmoid function is defined in terms of two functions s' and s'' selected to yield a continuous function at an expected local maximum of the second relationship as a function of the absolute or relative current/light intensity, and so that a derivative of the continuous function does not change sign.

[0051] In some embodiments, the configuration information comprises respective determined and stored configuration information for at least one of firstly, at least two different number of pulses of the control signal pattern; secondly, at least two different temperatures of the LED driver when obtaining the measurement values; and thirdly, at least two different maximum allowed currents to be provided to the LED driver.

[0052] The invention also relates to a method for operating an LED driver to drive an LED, the method comprising configuring the LED driver using a method of the above type; and operating the LED driver by determining a binary control signal corresponding to a desired current/light intensity, the determining of the binary control signal being performed using the configuration information, and providing a variable current to a driver output of the LED driver based on the determined binary control signal.

[0053] In some embodiments, the determining of the binary control signal comprises adjusting one or several pulse widths within the binary signal pattern.

[0054] In some embodiments, the determining of the binary control signal comprises adjusting a number of pulses within the binary signal pattern.

[0055] In some embodiments, the pulses within the binary signal pattern are adjusted so as to be distributed over a predetermined set of available pulse positions across the binary signal pattern.

[0056] In some embodiments, the determining of the binary control signal comprises determining a number of pulses within the control signal pattern; and to select the binary control signal according to an interpolation between a first and a second respective expression for the binary control signal.

[0057] In some embodiments, the first expression for the binary control signal is determined based on the configuration parameters for a first number of pulses within the control signal pattern.

[0058] In some embodiments, the second expression for the binary control signal is determined based on the configuration parameters for a second number of pulses within the control signal pattern.

[0059] In some embodiments, the interpolation is performed for a current number of pulses within the control signal pattern between the first number of pulses and the second number of pulses.

[0060] In some embodiments, the first and second expressions for the binary control signal are determined based on a respective pulse width within the control signal pattern.

[0061] In some embodiments, the interpolation is performed using as a weight factor, for the first and second expressions for the binary control signal, a square root of a normalized value for the current number of pulses.

[0062] The method also relates to an LED driver, comprising a first-channel electric driver output, the LED driver being arranged to provide a current to the first-channel electric driver output according to a first-channel binary control signal; and a first-channel timer function, the first-channel timer function being configured to update a first-channel timer counter variable at a first-channel timer frequency, the first-channel timer function being configured to, for each update, compare the first-channel timer counter variable to a set first-channel compare value, and the first-channel timer function being configured to, in case the first-channel timer counter variable has reached or gone past the set first-channel compare value, cause the first-channel binary control signal to switch between a first binary state and a second, different, binary state.

[0063] In some embodiments, a duration of a repeated first-channel control signal pattern of the first-channel binary control signal is longer than the time it takes for the first-channel timer counter variable to complete a full cycle, the first-channel control signal pattern comprising one or several pulses.

[0064] In some embodiments, the LED driver is arranged to update the set first-channel compare value at least two times during each individual first-channel control signal pattern.

[0065] In some embodiments, the first-channel timer frequency is at least as high as, or higher than, a predetermined clock frequency of a CPU comprised in the LED driver.

[0066] In some embodiments, the first-channel timer function uses a DLL, Delay Locked Loop, function, configured to divide a timer input clock period into several fractional steps.

[0067] In some embodiments, the first-channel timer function is cyclic.

[0068] In some embodiments, the LED driver further comprises a RAM, Random Access Memory, area; and a compare value copying function, operable to update the first-channel timer function with an updated set first-channel compare value from the RAM area.

[0069] In some embodiments, the compare value copying function is a DMA, Direct Memory Access, channel or an ISR, Interrupt Service Routine being executed in response to an IRQ, Interrupt Request.

[0070] In some embodiments, the compare value copying function is configured to react to an interrupt produced in connection to the first-channel timer counter value reaching its full cycle value, the reaction comprising copying a new first-channel compare value from a next or subsequent memory position of the RAM area.

[0071] In some embodiments, the DMA channel is configured to be circular, such that after it has reached the end of the RAM area it continues copying from a beginning of the RAM area again.

[0072] In some embodiments, a size of the RAM area is at least 4 compare values, such as at least 8 compare values, such as at least 16 compare values.

[0073] In some embodiments, the CPU is configured to, in reaction to an updated dimmer setting received by the LED driver, update the RAM area with an updated set of first-channel compare values specifically selected to reflect said updated dimmer setting.

[0074] In some embodiments, an individual pulse of the binary control signal is longer than the time it takes for the first-channel timer counter variable to complete a full cycle.

[0075] In some embodiments, the LED driver is arranged to vary a number of pulses provided across the first-channel control signal pattern so as to achieve different desired instantaneous time-averaged values of the first-channel control signal pattern.

[0076] In some embodiments, the LED driver is arranged to vary a respective pulse width of one or several of a set of one or several pulses provided across the first-channel control signal pattern so as to achieve different desired time-averaged currents provided to the first-channel electric driver output.

[0077] In some embodiments, the LED driver is arranged to gradually increase the time-averaged applied current to the first-channel electric driver output by first increasing a pulse width of one or several pulses provided across the first-channel control signal pattern and to thereafter increase a number of pulses provided across the first-channel control signal pattern.

[0078] In some embodiments, the LED driver is arranged to distribute the at least one pulse across the first-channel control signal pattern over a set of predetermined and distributed time pulse positions across the first-channel control signal pattern.

[0079] In some embodiments, the distribution takes place according to a bit-reversal of a binary representation of a number, the number in turn describing or corresponding to the index of the pulse within the first-channel control signal pattern.

[0080] In some embodiments, a duration of the first-channel control signal pattern is constant across different desired time-averaged currents provided to the first-channel electric driver output.

[0081] In some embodiments, the LED driver comprises, in addition to said first-channel electric driver output, a second-channel electric driver output, the LED driver being arranged to provide a current to the second-channel driver output according to a second-channel binary control signal; and a second-channel timer function, the second-channel timer function being configured to update a second-channel timer counter variable at a second-channel timer frequency, the second-channel timer function being configured to, for each update, compare the second-channel timer counter variable to a set second-channel compare value, and the second-channel timer function being configured to, in case the second-channel timer counter variable has reached or gone past the set second-channel compare value, cause the second-channel binary control signal to switch between a third binary state and a fourth, different binary state.

[0082] In some embodiments, a duration of a repeated second-channel control signal pattern of the second-channel binary control signal is longer than the time it takes for the second-channel timer counter variable to complete a full cycle, the second-channel control signal pattern comprising one or several pulses.

[0083] In some embodiments, the LED driver is arranged to update the set second-channel compare value at least two times during each individual second-channel control signal pattern.

[0084] In some embodiments, a duration of the first-channel control signal pattern is an integer multiple of, such as the same as, a duration of the second-channel control signal pattern.

[0085] In some embodiments, the first-channel binary control signal is time-offset in relation to the second-channel binary control signal by an offset value that is smaller than the first-channel control signal pattern.

[0086] In some embodiments, the LED driver comprises three or more electric driver outputs, the LED driver being arranged to apply a respective current to each such driver output according to a respective binary control signal.

[0087] In some embodiments, each of the binary control signals has a respective repeated control signal pattern, the duration of which is an integer multiple or fraction of, such as the same as, each of the duration of repeated control signal patterns of the other binary control signals.

[0088] In some embodiments, the LED driver is arranged to time-offset each of the binary control signals by a value lower than the duration of the first-channel control signal pattern.

[0089] In some embodiments, the respective time-offsets of the at least three control signal patterns are distributed over a set of predetermined and distributed time offsets across the first-channel control signal pattern.

[0090] In some embodiments, the respective time-offsets of the at least three control signals are different.

[0091] In some embodiments, the time-offsets are computed according to a bit-reversal of a binary representation of a number, the number in turn describing or corresponding to the index of the respective electric driver outputs.

[0092] In some embodiments, the time-offsets are scaled over a duration of the first-channel control signal pattern.

[0093] In some embodiments, a clock frequency of the first-channel timer function is at least 50 MHz, such as at least 100 MHz, such as at least 150 MHz.

[0094] In some embodiments, the LED driver is a constant-voltage LED driver.

[0095] In some embodiments, the first-channel binary control signal is arranged to switch between the first binary state and the second binary state and back to the first binary state again at a frequency of at least 20 kHz, preferably at least 25 kHz.

[0096] In some embodiments, the LED driver further comprises a DC bus, the DC bus comprising a ceramic capacitor.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

[0097] Fig. 1a is a chart showing a current as a function of a voltage;

- [0098] Fig. 1b is a chart showing a log current as a function of a voltage, the current and voltage corresponding to those shown in Fig. 1a;
- [0099] Fig. 1c is a chart showing several different log currents as a function of a voltage;
- [0100] Fig. 2 is an overview of an LED driver;
- [0101] Fig. 3 is a flowchart showing an interrelationship between a first aspect, a second aspect and a third aspect;
- [0102] Fig. 4a is a chart showing a voltage-signal pulse train with straight flanks;
- [0103] Fig. 4b is a chart showing a voltage-signal pulse train with slanting flanks;
- [0104] Fig. 4c is a series of charts, going from the topmost chart to the lowermost chart, showing a progression of a pulse train design for an increasing PWM-like duty cycle;
- [0105] Fig. 4d is a principle graph of a pulse with definitions;
- [0106] Fig. 5 is an overview of an LED driver;
- [0107] Fig. 6 is a chart illustrating an order according to which different pulses are introduced in a pulse pattern;
- [0108] Fig. 7 is a flowchart illustrating how to introduce pulses in a pulse pattern;
- [0109] Fig. 8 is a chart showing a light intensity as a function of a PWM-like duty cycle;
- [0110] Fig. 9 is similar to Fig. 8, but shows the information in a log-log chart;
- [0111] Fig. 10 is a chart showing a curve fitting, together with a chart showing a sigmoid function;
- [0112] Fig. 11 is a flowchart for operating an LED driver;
- [0113] Fig. 12 is an overview chart illustrating an LED driver configuration setup;
- [0114] Fig. 13 is a chart showing an alternative sigmoid function;
- [0115] Fig. 14 is a flowchart for operating an LED driver;
- [0116] Fig. 15 is an overview of an LED driver connected to an LED load;
- [0117] Fig. 16 is an overview of an LED drivers;
- [0118] Fig. 17 is a circuit diagram showing a push-pull circuit;
- [0119] Fig. 18 is a circuit diagram of an LED driver;
- [0120] Figs. 19 and 20 are a series of circuit diagrams illustrating an analysis of part of the circuit diagram of Fig. 18;

[0121] Fig. 21 is a chart showing a curve set of voltages as a function of an output voltage and of a temperature;

[0122] Fig. 22 is a chart showing a curve set of voltages as a function of an output voltage and of a resistance;

[0123] Fig. 23 is an overview of an LED driver;

[0124] Fig. 24 is a circuit diagram of an LED driver;

[0125] Fig. 25 is a circuit diagram of an LED driver;

[0126] Figs. 26a and 26b shows the shape of a respective voltage pulse as a function of time; and

[0127] Fig. 27 is a flowchart for operating an LED driver.

[0128] The Figures share the same reference numerals for same or corresponding parts. Some reference numerals are used with or without one or several apostrophes, where the reference numeral without any apostrophe refers to the part in general whereas a number of apostrophes after the reference numeral denotes a particular channel. For instance, the LED drive switch is generally referred to as 180 whereas 180'' refers to the LED drive switch for a second channel.

DETAILED DESCRIPTION

[0129] The behavior of any particular LED light source may be difficult to foresee across a wide range of driving powers. In particular, dimming behavior may not be linear, or it may even be undefined.

[0130] To understand this, one can investigate the behavior in terms of light power as a function of voltage for an LED connected in series with a current-limiting resistor, which is a common setup.

The current through an LED is described by Shockley's diode equation:

$$I_D = I_s \left[\exp\left(\frac{V_D}{nV_T}\right) - 1 \right],$$

wherein I_D is the current through the diode, I_s is the current scale factor, V_D is the voltage, V_T is the thermal voltage and n is the ideality factor. For LEDs, I_s is normally in the order of nA, making the exponential term dominating for normally occurring currents I_D . The expression can therefore be simplified to

$$I_D = I_s \cdot \exp\left(\frac{V_D}{nV_T}\right),$$

And, solving for V_D :

$$V_D = nV_T \cdot \ln(I_D/I_S).$$

[0131] As an example of how the current varies through an LED that is connected in series with a resistor, a typical LED can be observed having a maximum forward current of 0.03 A. The LED used in this example is an NSPW500BS sold by Nichia. The parameter values can easily be read in the software program LTSpice, resulting in $I_S = 0.27$ nA and $n = 6.79$. The thermal voltage V_T is obtained by the expression $V_T = kT/q$, where k is the Boltzmann constant, T is the absolute temperature and q the elementary charge. In room temperature (300 K), this equation yields $V_T = 25.852$ mV.

[0132] This, in turn, results in

$$V_D = nV_T \cdot \ln(I_D/I_S) \approx 0.1755 \cdot \ln\left(\frac{I_D}{0.27 \cdot 10^{-9}}\right).$$

[0133] At 0.03 A, $V_D = 3.25$ V. If the series-connected LED and resistor are driven at 5 V, 1.75 V will be across the resistor at nominal current, which yields the resistance $R = U/I = 1.75/0.03 = 58.3 \Omega$. The equation for the voltage given the diode current therefore becomes

$$U = V_D + I_D \cdot R = 0.1755 \ln\left(\frac{I_D}{0.27 \cdot 10^{-9}}\right) + I_D \cdot 58.3.$$

[0134] A plot of this equation can be seen in Fig. 1a, and a version with log-scale current is shown in Fig. 1b. It can be seen that the graph has an approximately exponential region, because of the LED, and an approximately linear region, due to the resistor. The light power from an LED is proportional to the current, and the human eye has higher sensitivity at lower light levels.

[0135] In the calculations above, all the physical constants were approximations. Fluctuations during manufacturing will cause the parameter values to shift from diode to diode, causing the resulting LEDs to have not the exact same properties and characteristics. Fig. 1c shows the result after shifting the ingoing parameter values slightly. From this Fig. 1c, it is clear that the fluctuations become more noticeable at lower voltage levels. For an LED strip comprising many individual LEDs, this means that the LEDs will start to shine differently as the voltage drops, which is not desirable.

[0136] To solve this problem, one can measure the properties of each LED precisely during or after manufacturing and only use similar-properties LEDs together. This is called “binning” and is fairly expensive. Instead, one can avoid using the LEDs at lower voltage levels but instead always use higher voltage levels, such as full power.

[0137] In the latter case, conventional LED drivers use switching patterns to dim LED light sources, switching the LED light source in question on and off rapidly at high enough frequencies so that the human eye is incapable of noticing the resulting flickering. Such driving using a pulsed power provides a perceived more uniform dimming behavior for a wide range of LED light sources having different properties. Such LED drivers are called “constant voltage” drivers.

[0138] One way of providing such pulsed power to an LED light source is by the LED driver using pulse width modulation (PWM). A PWM signal can be described in terms of the pulse width and period time (both measured in seconds), or alternatively in terms of its frequency (measured in Hz) and duty cycle (the pulse width in relation to the period time, measured as a percentage).

[0139] In microcontroller based PWM drivers, a timer may be used that counts the number of clock cycles and that compares this number to a certain compare value. As long as the counter is below the compare value, the output signal is high (such as a predetermined full LED power); and when the timer exceeds the compare value, the output signal becomes low (such as zero LED power). The timer is then reset as the period time is reached. Hence, the time resolution of the PWM driver is determined by the clock frequency of the timer, and the PWM frequency is the clock frequency divided by the period length (measured in number of clock cycles). For instance, if a timer having a clock frequency of 25 MHz uses a period of 100,000 steps (clock cycles), a PWM signal is generated having a period frequency (PWM frequency) of $25 \cdot 10^6 / 10^5 = 250 \text{ Hz}$. The time resolution is $1 / (25 \cdot 10^6) = 40 \text{ ns}$. In this case, the smallest duty cycle achievable is for compare value = 1, and the duty cycle is then $1/1e5 = 0.001\%$.

[0140] The human eye has higher sensitivity at low lighting levels, meaning that it is the relative change of the light intensity which is important to the sensation of light. A change from 100% light intensity to 10% light intensity is experienced as roughly equally large as a change from 10% to 1% light intensity. In other words, an LED driver dimming from 100% to 1% time-averaged light intensity is perceived to dim the LED light source twice as “far” as an LED driver dimming from 100% to 10%.

[0141] At the same time, the human eye can perceive light in very small quantities. For instance, it has been found that light emitted from an LED light source of nominal current at 200 mA can be perceived when the LED light source is driven with as little as 5 μA total current, which is 40,000 times less than the nominal current.

[0142] In order to dim such an LED light source down to such low emitted powers using PWM, a duty cycle of 0.0025% would be required. If this number is rounded down to 0.001%, this then means that a microcontroller with a clock frequency of 25 MHz using a PWM frequency of 250 Hz would barely be able to achieve such low dimming levels.

[0143] However, even if such low dimming would be possible, the step from the lowest dimming level to the second-lowest dimming level would be 100%, which would be a very noticeable step in light intensity to the human eye. In particular, this would be visible when using color-settable lighting (such as an RGB-controlled lighting), since the color would change significantly by dimming one of the color channels up or down close to the lowest possible dimmer setting.

[0144] It has been shown that the human eye is incapable of sensing a light intensity change of less than about 1.5%. Therefore, if an LED driver is to be able to dim all the way down to darkness and be perceived as dimming continuously over the whole dimming intensity interval, all dimming steps across the whole intensity interval must be less than 1.5%. If the maximum step size is set to 1% for margin, such 1% steps need to be taken at 0.001% light intensity close to the lower-most dimming levels. This means that the light intensity resolution needs to be at the most 0.00001% at these levels.

[0145] Producing short PWM pulses furthermore results in wavelengths that risk being of the same magnitude as an LED strip in which the controlled LED is used. LED strips tend to be at the most 5 m – 10 m long, in order to avoid intolerable voltage drops across the LED strip. The speed of light in copper is about half of that in vacuum, meaning that a pulse of 40 ns into an LED strip will have a pulse length of roughly 6 m:

$$(s = vt = 150 \cdot 10^6 \cdot 40 \cdot 10^{-9} = 6 \text{ m}).$$

[0146] 6 m is the same order of magnitude as the length of a typical LED strip. Since the pulse length is comparable to the length of the LED strip, this means that the load must be modelled using microwave theory rather than traditional voltage equations. In other words, the generated pulse will to some extent be reflected at the end of the LED strip, and the pulse together with its reflection will risk creating standing wave patterns along the LED strip. This, in turn, means that the applied voltage will not be uniform along the LED strip and the individual LEDs will shine with different power depending on the applied voltage pulse characteristics.

[0147] At the same time, it is also necessary to avoid visible flickering as well as sounds accruing from the driver or any power source used. Since PWM by definition involves flickering, the flickering needs to be kept at frequencies not perceived as disturbing. This is done by using sufficiently high PWM frequencies.

[0148] The standard IEEE PAR1789 (“IEEE Recommended Practices for Modulating Current in High-Brightness LEDs for Mitigating Health Risks to Viewers”) defines “flicker-safe” driving of a load alternating between 0% and 100% as using a driving frequency of at least 3 kHz. The disturbing effect of flickering as perceived by humans decreases with decreasing average light intensity. The present inventors have noted that it is not as critical to stay above 3 kHz frequencies when operating close to the lowest dimming intensities for drivers capable of dimming to complete darkness.

[0149] At 3 kHz PWM frequency and 0.001% duty cycle, the pulse width becomes very short; 0.001% of a period time of 333 μ s is 3.33 ns. This is equivalent to a PWM frequency of 300 MHz, and for a square wave preserving its first overtones this implies frequencies in the GHz range. At such high frequencies, the wavelengths become so short so that the voltage supply cable starts acting as an antenna, potentially resulting in crosstalk with nearby cables. Problems with standing waves in the voltage supply cable may also accrue, resulting for instance in an LED light strip supplying different light intensities along different parts thereof.

[0150] To mitigate these problems, it is possible to remove the sharp current derivatives of the PWM signal, resulting in that the highest frequencies are decreased or eliminated. However, this means that the LED light source will spend more time in total in the voltage interval between 0 V and nominal voltage (for instance, 12 V or 24 V). As the behavior of the LED light source may be undefined in this interval, uneven light may result during dimming. Therefore, for an LED light source to work acceptably at a PWM signal of 3 kHz and a duty cycle of 0.001%, the light intensity emitted by different LEDs in the same LED light source (or “LED load”) should preferably have the same behavior in terms of light output as a function of time-averaged current in the interval from 0 V up to its nominal voltage. This is possible, but then conventionally requires careful binning of the LED light sources to use with one and the same LED driver, in order to minimize the differences of their forward voltages.

[0151] For higher light intensities, however, the current derivatives will only contribute to a very small share of the total light, why any differences between individual LED light sources become unnoticeable far from the lowest dimming intensities.

[0152] For many LED drivers, unwanted noise becomes a problem as the delivered power varies. For instance, a constant voltage LED driver will draw a varying current as the delivered power varies, resulting in that any capacitors and inductors in a power supply used may start emitting sound. If the PWM frequency is within the human-hearable sound frequency spectrum, such sounds may become noticeable when the current requirements are high enough.

[0153] By using a PWM frequency exceeding about 25 kHz, any resulting noise will not be noticeable to the human ear. Such high PWM frequencies also make it possible to use chip capacitors while still providing sufficient capacitance to draw relatively smooth currents, in turn resulting in smaller current and voltage variations for the power supply. Smaller voltage variations means that any electrolyte condensers in the power supply are not loaded as heavily during operation, effectively prolonging their useful life.

[0154] For these reasons, a PWM frequency of at least 25 kHz is advantageous so long as the LED light source draws a non-negligible current. Instead, ceramic capacitors, typically associated with a long useful life, can then be used if high PWM frequencies are selected.

[0155] The LED driver embodiments described herein may be constant-voltage LED drivers. They can be used to drive individual LEDs and/or LED strips, for instance at 12 V or 24 V constant voltage. An LED strip is typically up to a maximum of 5 m or 10 m, and can comprise a plurality of individual LEDs that in turn can be connected in series to one or several resistors. Groups of one or more individual LEDs in an LED strip can be connected in parallel, allowing a user to adapt the total length of the LED strip by cutting it at predetermined points along the length of the LED strip.

[0156] Fig. 2 illustrates an exemplary LED driver 100 having N channels. That the LED driver has N channels means that it can concurrently drive N LED loads, such as N different LEDs and/or LED strips. The drive of the channels can take place in an independent manner, so that each channel can be dimmed independently of the other channels. For multi-color LEDs, different colors can be controlled over different channels, with an RGB (Red Green Blue) LED as an example. As an example, the LED driver 100 can have twelve channels, but it is realized that the number of channels in various embodiments can be at least one, at least two, at least four, or at least ten;

and/or that the number of channels can be at the most one hundred, at the most fifty, or at the most twenty.

[0157] The LED driver 100 comprises a microcontroller 130, arranged to accept a respective control input 110', 110'', 110''' for each of the N channels. Each such control input 110', 110'', 110''' can be in the form of a digitally coded number or an analog signal representing a desired dimming value for the channel in question.

[0158] The microcontroller 130 comprises a CPU 131 and/or other hardware computational logic circuitry component, such as a GPU. The microcontroller 130 can further comprise a respective timer function 132', 132'', 132''' for each of the channels. Each such timer function 132', 132'', 132''' can in turn comprise a respective DLL (Delay Locked Loop) function 133', 133'', 133'''. The microcontroller 130 can further comprise a RAM (Random Access Memory) area 134 and/or a compare value copying function 135. For each of the channels, the microcontroller 130 can comprise a respective binary control signal generator 136', 136'', 136''' and/or a respective pulse compensator 137', 137'', 137'''. These components will be described in closer detail below.

[0159] The LED driver 100, and in particular the microcontroller 130 can comprise a piece of control software, arranged to execute on the CPU 131 and/or any other computational hardware component of the microcontroller 130 and when executed perform the steps described herein performed by the microcontroller 130. One or several of the steps described herein can also be performed using purely hardware-based logic, as the case may be. Each of the components 132, 135, 136 and 137 can be implemented as discrete hardware components; as software modules; or a combination. The LED driver 100 can also comprise a communication bus for communication between the various hardware and software components of the LED driver 100 described herein.

[0160] The LED driver 100 furthermore comprises, or is connected to, an internal or external power supply 120. The LED driver 100 can further comprise a DC bus 121, that in turn can provide a constant voltage of at least eight volts and/or at the most 48 volts. The power supply 120 can be arranged to, via the LED bus 121, power the microcontroller (such as using 3.2 V) and/or an LED drive switch 180', 180'', 180''' of the LED driver 100 (such as at 5.0 V). One such LED drive switch 180', 180'', 180''' for each channel is arranged to provide a variable current to a respective driver output corresponding to the channel in question. The time-average of the variable current

corresponds to the desired dimming value for that channel. The DC bus can comprise a ceramic capacitor.

[0161] The LED driver 100 can also comprise a respective drive circuitry 140', 140'', 140''' for each channel. The drive circuitry 140 is arranged to provide an analog switch control signal to the LED drive switch 180 to control the LED drive switch 180 to in turn provide the drive current to the LED driver output. The drive circuitry 140 can comprise software-implemented functionality, but in examples the functionality of the drive circuitry 140 is entirely or at least partly implemented in hardware.

[0162] The LED driver 100 also comprises functionality for overcurrent and overtemperature protection. Such functionality is conventional as such and will not be described in detail herein.

[0163] The present inventors have developed the LED drivers described herein according to three aspects, that can be used independently or combined freely.

[0164] In a first aspect, pulses generated by the microcontroller 130 have a dynamic frequency such that low frequencies are used for low intensities and high frequencies are used for higher intensities.

[0165] In a second aspect, a model is formulated allowing a mismatch to be decreased between expected light intensity and actual light intensity.

[0166] In a third aspect, the drive circuit 140 is devised having a dynamic rise and fall time, such that smooth pulses with long rise and fall times are used for low intensities while faster pulses with shorter rise and fall times are used for higher intensities.

[0167] The interrelationship between these aspects is illustrated by means of a simplified overview shown in Fig. 3.

[0168] Starting from the top of Fig. 3 and moving downwards, a control input is generated, identified or received by the microcontroller 130. The control input can be an analog or digital signal on any suitable format that can be interpreted by the microcontroller 130. Generally, the input signal can be significative of a desired dimming level, such as on a scale from 0% (no light emitted from the LED) to 100% (full light). In the example shown, the control value received by the microcontroller 130 signifies "10% dimming level".

[0169] Functionality according to the first aspect then produces a pulsed signal corresponding to the control input. More particularly, the pulsed signal is a periodic binary signal generated by one or several timer functions 132 of the microcontroller 130. The periodicity of the periodic binary signal can coincide with a lowest supported frequency of the microcontroller 130, and a highest supported frequency of the microcontroller 130 can be a multiple of this lowest supported frequency. In examples, the lowest supported frequency is 250 Hz and the highest supported frequency is 32 kHz.

[0170] Herein, such a produced periodic binary signal is generally denoted “binary control signal”. A binary control signal can be in the form of a square wave comprised of an alternating low and high value, such as 0 and 1. The binary control signal can have a control signal pattern, in other words a binary pattern that is repeated over time to form the binary control signal. At each given point in time, the control signal pattern has an instantaneous time-averaged value. This instantaneous time-averaged value is a value determined as the time-averaged value over the control signal pattern used to form the binary control signal at the time of determination. The control signal pattern can change over time, for instance in reaction to a changed control input. In some embodiments, the (potentially over time changing) repeated control signal pattern fully defines the binary control signal over time, such that the binary control signal does not comprise any additional waveforms in addition to the repeated control signal pattern. At any rate, the control signal pattern can be arranged to completely determine an instantaneous time-averaged value of the binary control signal at all times.

[0171] As is shown in Fig. 3, the generated binary control signal can comprise pulses of different pulse widths. Generally, the control signal pattern can comprise one or several pulses, each having the same or different pulse widths, and/or the time between individual pulses can be the same or different. This way, the produced binary control signal has similarities to a PWM signal, but can be more complex than a conventional PWM signal. In some embodiments, the binary control signal has a duration of at least 0.1 ms, such as at least 0.5 ms, such as at least 1 ms, or even at least 2 ms. In some embodiments, the binary control signal has a duration of at the most 1000 ms, such as at the most 500 ms, such as at the most 100 ms, such as at the most 50 ms, such as at the most 20 ms, or even at the most 10 ms.

[0172] Functionality according to the second aspect, and in particular a pulse compensator 137 of the microcontroller 130, can then produce, based on the binary control signal, a compensated binary control signal. This compensation can then take into consideration a determined model of properties of at least one of the drive circuitry 140, the LED drive switch 180, the LED load 10 actually powered by the LED driver 100, and a predetermined typical LED load to be powered by the LED driver 100.

[0173] More particularly, as any pulse rise or fall time has a non-zero width for any drive circuitry, the actual relative current drawn from an LED load will not perfectly match the average duty cycle of the binary control signal. If the instantaneous pulse frequency of the binary control signal is increased while the average PWM-like duty cycle is kept constant, the pulse widths become narrower and the rise and fall times will have a larger impact on the overall match between average duty cycle and average relative current drawn from the LED load 10. The model can therefore be devised to approximate an inverse model of the drive circuitry 140 such that the compensated signal compensates for the particular behavior of the drive circuitry 140 (and correspondingly for the LED drive switch and the LED load 10 or typical LED load).

[0174] As is shown in Fig. 3, the compensated binary control signal can have a format that corresponds to the uncompensated binary control signal, such as having straight flanks (it can be a purely binary signal), but the pulse configuration can be altered for instance in terms of individual pulse widths in the control signal pattern.

[0175] Maintaining even light intensity over the whole length of an LED strip at low light intensities requires that the pulses are physically much longer than the LED strip itself. Thus, too short pulse widths cannot be used and so the pulses must be longer while at the same time not contributing to too much light. If the rise and fall times are longer, the pulses get wider while not contributing to maximum power output. However, for higher currents and higher frequencies, this results in more power dissipations than necessary. Functionality according to the third aspect, and more particularly the drive circuitry 140, provides the analog control signal as a (not purely binary) signal having dynamic rise and fall times that depend on the instantaneous time averaged value of the binary control signal.

[0176] The analog control signal is then provided to the LED driver switch 180, the latter producing the current at the LED driver output 182 (see Fig. 5 and Fig. 15) to be provided to the LED load 10.

The current is provided using the power supply 120. The average current provided to the LED load 10, relative to a maximum current, can be the input to the control input 110 to the LED driver 100.

[0177] It is realized that each of the first, second and third aspects provide different advantages in terms of a final pulsed current provided to the LED load 10, but that all three aspects are not necessary in all embodiments. In particular, the first, second and third aspects can be used individually or be combined in pairs of two, or all three, to provide various advantages as described herein and as is desired or needed in the particular use case considered. For instance, the control input can be in the form of a PWM-like signal provided directly to the functionality according to the second aspect. The binary control signal can be used as it is and provided directly to the functionality according to the second aspect. The compensated control signal can be provided directly to the LED driver switch 180. And so on.

[0178] Fig. 4a shows an exemplary binary control signal, in the form of a square voltage (Y axis) wave shape as a function of time (X axis), the wave shape alternating between a low value (in this case 0 V) and a high value (24 V). The binary control signal is arranged to control an on/off or high/low state of an LED load, such as an individual LED light or an LED strip as described above. It is realized that the binary control signal can alternatively be an electric current signal.

Furthermore, the signal shown in Fig. 4a is an analogue signal, but it is realized that the binary control signal in some embodiments can be a coded signal, such as a digitally coded signal conveying the corresponding wave shape information. The binary control signal can also be digitally generated by a timer 132 of the microcontroller 130, and output as an analog signal of the type shown in Fig. 4a.

[0179] For a binary control signal in the form of a repeated square wave shape having only one pulse, the pulse width divided by the period width is the percentage time that the binary control signal is active. As discussed above, this is called the duty cycle, for instance in PWM. In the example provided in Fig. 4a, the pulse width is 60 clock cycles and the period time is 200 clock cycles, yielding a duty cycle of $60/200 = 30\%$. The frequency is provided as the inverse of the period time. Timers that are integrated in conventional microcontrollers typically use an internal clock to count the number of clock cycles until a desired maximal counter value is achieved, after which the counter is restarted. The counter value is compared to a compare value and the microcontroller

generates a signal which is high if the counter is under the compare value but low if the counter is over the value, resulting in a PWM signal.

[0180] The time resolution of this signal is determined by the speed of the internal clock: the faster the clock counts, the more frequent the possibility of changing the signal from low to high or vice versa. Most conventional microcontrollers use a main clock that can be scaled down to generate the timer clock. Recent microcontrollers, however, sometimes have timers that use delay locked loops (DLLs), in effect providing the same effect as scaling up the main clock.

[0181] In embodiments of the present invention, the LED driver 100 can be a constant-voltage LED driver, arranged to drive an LED load 10 at a constant voltage. Instead of varying a current smoothly to achieve various dimming levels, the LED driver 100 can be arranged to provide a voltage signal switching from zero to the notional constant voltage (such as 12 V or 24 V), or from some other low value above zero to said notional constant voltage. The switching can then take place according to a square wave signal such as the one shown in Fig. 4a, or according to such a square wave signal that has been compensated and/or modified as described in connection to the various embodiments described herein. It is realized that this also means that a drive current provided to the LED load 10 will be a varying (pulsed) current, as a result of the voltage switching between its low value and its high value.

[0182] As mentioned above, there is a problem generating very low light levels in an LED load 10 using a PWM approach, both since the dimming step size at very low light levels becomes relatively large even with a fast microcontroller, and also because very short pulses yield problems with standing waves along a driven LED strip.

[0183] Another thing to consider is how the voltage supplied to the LED load 10 changes over time, in other words the voltage derivative when switching from the low value to the high value and vice versa. This is illustrated in Fig. 4b, which corresponds to the wave shape shown in Fig. 4a but shows a varying voltage applied to an LED load 10 by the LED driver 100.

[0184] As is clear from Fig. 4b, the voltage takes a while to change from the low value to the high value and vice versa, causing the LED load 10 to emit light before the rising voltage has reached its maximum level, and correspondingly before the sinking voltage has reached its minimum level. The properties of this voltage derivatives at the flanks of the voltage provided to the LED load 10 affects the behavior of the LED load 10 in terms of light emitted at low dimming values. The

challenge is to cause the LED driver to achieve even and smooth lighting at low dimming values both in terms of the dimming behavior of each individual LED light and light emitted along the LED strip.

[0185] The present invention solves this problem by defining a lowest acceptable PWM frequency to use at low light levels allowing a sufficiently wide pulse width to achieve a particular defined low average light power over time without noticeable pulse flank effects due to the voltage derivatives. Dimming up the light power from a low or lowest dimming value, the pulse width can first be increased up to a certain pulse width at which the flank effects are negligible in relation to the duty cycle, and at that point another pulse can be introduced in the repeated pulse pattern. The newly added pulse can have a pulse width which is narrower than the already-existing pulse. It is understood that this signal is then no longer a PWM signal, but a more complex signal.

[0186] The pulse width of the newly added pulse can then be increased as the dimming value is increased, up until the certain pulse width, whereupon an additional pulse can be added, and so on.

[0187] Once a desired maximum number of pulses has been reached in the repeated control signal pattern, the pulse widths of all the pulses can be grown in concert to further increase the dimming value up until a full-light point where the pulses completely fill the signal and the signal de facto is at its high value 100%, or close to 100%, of the time.

[0188] Fig. 4c illustrates an example of how this can be achieved. Each row in Fig. 4c illustrates two full cycles (each 4,000 μ s long) of the repeated waveform signal provided to the LED load 10, where the dimming value is increased from the top to the bottom row. The voltage derivatives are slightly exaggerated for reasons of clarity. Each row in Fig. 4c is denoted using an instantaneous time-averaged control signal pattern value of the row in question, as marked to the left in the chart. The X axis in Fig. 4c represents clock cycles.

[0189] In the first waveform, a 250 Hz signal is introduced. Since the derivative is limited and the pulse is short, the pulse does not have the time to reach the high value of 24 V before the pulse ends. However, as the dimming value increases, the voltage at the pulse peak increases. Once the pulse has reached said certain pulse width that is sufficiently broad so that flank behavior is negligible, an additional pulse is introduced (see the third row). This added pulse is then pulse width-increased up to the certain pulse width. Thereafter, new pulses are introduced between the

existing pulses until a maximum number of pulses has been reached. Lastly (row seven forward), the pulse width of all pulses is increased simultaneously up to maximum light.

[0190] An alternative way of achieving this would be to increase the pulse width until the certain pulse width and to thereafter decrease the period time of the repeated signal. As will be seen below, however, this is sometimes not a feasible solution in embodiments (such as for multi-channel LED drivers) where a fixed total time for a repeated signal pattern is desired.

[0191] Fig. 5 is another view showing an exemplary LED driver 100 having three channels, for instance for driving an RGB LED or LED strip 10. Three different dimming values (such as red, green blue) are received by the LED driver 100 and specifically by the microcontroller 130. The microcontroller 130 outputs one corresponding binary control signal to each of three analog drive circuits 140', 140'', 140'''. The drive circuits 140', 140'', 140''' each produce a corresponding analog control signal, which is fed to a corresponding switch 180', 180'', 180''', each in turn having a driver output terminal 182', 182'', 182''' providing a respective varying (pulsed) voltage signal to each of three respective inputs on the LED load 10, the voltage signals providing the desired set dimming and color settings.

First aspect of the invention

[0192] Turning now specifically to the first aspect, and with reference to Fig. 2 and Fig. 5, the LED driver 100 comprises the first-channel electric driver output 182' to which the LED driver 100 is arranged to provide a current according to the first-channel binary control signal provided by the binary control signal generator 136.

[0193] The first-channel timer function 132' can be configured to update a first-channel timer counter variable at a first-channel timer frequency, the first-channel timer function 132' being configured to, for each such update, compare the first-channel timer counter variable to a set first-channel compare value, and the first-channel timer function 132' being further configured to, in case the first-channel timer counter variable has reached or gone past the set first-channel compare value, cause the first-channel binary control signal to switch between a first binary state and a second, different, binary state. The corresponding can also be true for any second-channel or further-channel timer function 132.

[0194] In some embodiments, a clock frequency of the timer function 132 is at least 50 MHz, such as at least 100 MHz, such as at least 150 MHz. In some embodiments, the binary control signal is arranged to switch between a first binary state and a second binary state and back to the first binary state again at a frequency of at least 20 kHz, such as at least 25 kHz. Such switching can be an average switching frequency over time for at least some ingoing dimming values.

[0195] As described above, dimming smoothly down to complete darkness is difficult without a high-resolution duty cycle using conventional PWM. To make matters worse, calibration would be rather coarse, resulting in poor intra-channel matching.

[0196] In practice, the present inventors have used a microcontroller STM32G484, available from ST Microelectronics, as the microcontroller 130. This microcontroller comprises a CPU 131 capable of performing floating point calculations at a clock frequency of 170 MHz, and it also features Direct Memory Access (DMA) functionality, making it possible to copy data from one memory area to another without directly involving the CPU 131. The STM32G484 also features six “high resolution timers”, also known as “HRTIMers”, used as the respective timer function 132 for each of the supported channels. The HRTIMers are based on DLL technology and are capable of splitting each clock pulse into 32 parts. This provides a lowest time resolution of the microcontroller of $\frac{1}{(32 \cdot 170 \cdot 10^6)} \approx 184 \text{ ps}$. The STM32G484 furthermore has two output channels per timer, making it possible to construct an LED driver 10 having a total of twelve channels, using the principles described herein, and is based on 16 bits counters. If the PWM period time is set to $65535 - 32 = 65503$, which is the longest possible period time using this counter, a PWM frequency of $\frac{32 \cdot 170 \cdot 10^6}{65503} \approx 83 \text{ kHz}$ is achieved. Therefore, using one and the same compare value is not a possible way to generate a high-resolution but low-frequency binary control signal.

[0197] However, the compare value can be updated before each HRTIM period, as will be explained in the following.

[0198] If, for example, a 32 kHz PWM signal is desired, the required number of HR (High Resolution) clock cycles can first be calculated: $\frac{32 \cdot 170 \cdot 10^6}{32000} = 170000$. Since this value is higher than 65503, it is split in three: $\frac{170000}{3} \approx 56666.67$. The period time is set to the lower nearest integer, in this case 56666, resulting in a total repeated control signal pattern period time of three periods of 56666, or a total of 169998 HR cycles and a PWM frequency of about 32000.38 Hz.

[0199] As an example, assume that the desired duty cycle for a corresponding PWM signal is 84.31393%. This then yields a total compare value of $169998 \cdot 0.8431393 = 143332$ HR cycles. It is noted that this is both more than 56666 and more than $56666 \cdot 2 = 113332$. Therefore, the two first compare values are each set to 56666, yielding an output control signal remaining at the high level for the two first run-throughs of the HRTIM period. The third compare value is set to the remaining value $143332 - 56666 \cdot 2 = 30000$.

[0200] In other words, at HR clock cycle 0, the compare value is set to 56666 and the counter variable starts from 0. The produced control signal is at the logical high value (such as being or corresponding to 3.3 V or “full light”). At HR clock cycle 56666, the counter variable reaches the end of the HRTIM period, and is reset to 0. The compare value is again set to 56666. The control signal remains at the high value. At HR clock cycle 113332, the counter variable is again reset to 0, and the compare value is set to 3000. The control signal remains at the high value. At HR clock cycle 143332, the counter variable reaches the compare value of 3000 and triggers a switch of the produced control from the high value to the logical low value (such as being or corresponding to 0 V or “no light”). The counter variable continues to increase until it reaches the end of the HRTIM period. Then, a switch of the output control signal is again triggered, now back to the high value, and the procedure restarts from the beginning using a counter variable reset to 0.

[0201] By updating the compare values after each HRTIM period, arbitrarily low frequencies can be generated while maintaining the required high time resolution. Again using the period time of the above example, a PWM frequency of 250 Hz can be generated by combining 128 times more the number of periods: $\frac{32 \cdot 170 \cdot 10^6}{56666 \cdot 3 \cdot 128} \approx 250 \text{ Hz}$. This means that $3 \cdot 128 = 384$ defined compare values can be used to generate a repeated binary control signal pattern that varies between 250 Hz and 32 kHz.

[0202] In general, a duration of the repeated control signal pattern of the binary control signal can be longer than the time it takes for the timer counter variable to complete a full cycle. This was illustrated in the example above, in which the counter variable reached the end of the HRTIM period several times before reaching the full length of the control signal pattern. Further generally, the repeated control signal pattern can comprise one or several pulses.

[0203] The LED driver 100 can be arranged to update the set compare value at least two times, or even, as seen in the example above, at least three times, or even more than three times, during each individual control signal pattern.

[0204] The timer function 132 can in principle have a clock frequency that is independent of a used clock frequency of the CPU 131 of the microcontroller 130. However, in some embodiments the CPU 131 can be arranged to run at a predetermined clock frequency and a clock frequency of the timer function 132' (the timer frequency) can be at least as high as, or higher than, the predetermined clock frequency of the CPU 131.

[0205] As mentioned in the example above, the timer function 132 can use the DLL 133, that in turn may be configured to divide a timer function 132 clock (a timer input clock period, "input" referring to the fact that the clock enters into the timer peripheral) into several fractional steps. This is equivalent to increasing the timer resolution of timer function 132 but without the need to increase the clock frequency of the same.

[0206] As also mentioned in the example above, the timer function 132 can be cyclic, meaning that the counter variable restarts from an initial value repeatedly, in the example above after the end of each HRTIM period has been reached, and is compared to the current compare value when stepping through the timer function 132 period. Herein, the terms "HRTIM period" and "timer period" are used interchangeably, but it is understood that the more general term "timer period" is equally applicable as "HRTIM period". In the concrete example discussed herein, the HRTIM timer divides the clock cycles using DLL, but in the more general case other concrete mechanisms can be used to define a suitable timer period.

[0207] As described, the exemplary HRTIM period of 56666 clock cycles means that the compare value needs to be changed after this time has passed, meaning in the example above 96000 times per second. If this task was for the CPU 131 to perform, it would need to devote a large share of its capacity to this task. Instead, the present inventors propose to perform the compare value update in the background, such as using a DMA channel.

[0208] Namely, in the above example the HRTIM units are controlled by a master clock that is reset after 56666 HR clock cycles. Each time it resets, all currently used compare values (for each

channel) are consumed, and new ones are needed. A DMA channel is configured so that each time new values are needed they are read directly from a circular RAM buffer, provided as or in the RAM area 134 and holding 384 values for each channel. Since the buffer is circular, the fetching of values is restarted from the beginning after all 384 values have been copied, and if the incoming dimming value has not changed the contents of the RAM buffer also needs not change. This offloads the updating work from the CPU 131. Once the dimming value is updated, a different algorithm is configured to update, if needed, data in the RAM buffer. In this example, this needs then be done at most every time the RAM buffer has been reached, namely 250 times per second. This updating can then be performed by the CPU 131 at substantially lower computational cost. The longest repeated control signal pattern possible without changing the values in the RAM buffer is then defined in terms of the number of clock cycles in each HRTIM period times the number of compare values that fit in the RAM buffer. In various embodiments, the RAM buffer can be dimensioned to hold at least 2, such as at least 4, such as at least 8, at least 16 or even at least 32 compare values at any given time. It is realized that the compare values can generally be integers.

[0209] Hence, the compare values in the RAM buffer can be configured to together define the repeated control signal pattern, in turn forming the binary control signal as the control signal pattern is repeated. As the dimmer setting is changed, the RAM buffer needs to be updated with a correspondingly updated set of compare values that together define a new repeated control signal pattern reflecting the updated dimmer setting. To this end, the CPU 131 can be configured to, in reaction to an updated dimmer setting received by the LED driver 100, update the RAM area 134 with an updated set of compare values specifically selected to reflect the updated dimmer setting.

[0210] Generally, the compare value copying function 135 can be configured to update the timer function 132 with an updated set compare value from the RAM area 134, such as one such compare value for each channel supported by the LED driver 100.

[0211] For microcontroller units in general, there are a number of different ways for a non-CPU component, or peripheral component, of the microcontroller in question, such as the timer function 132, to receive and process updated information. As a first example, using a polling interface the updated value is fed to the component by the CPU, and the CPU waits for the value to be consumed before feeding the next value. This is not a very efficient way to use CPU resources

since the CPU will then be locked during the time it takes for the component to consume the value. As a second example, an interrupt-controlled interface can be used. Then, a value or a buffer is fed to the component, whereupon the component consumes the values in the background. Once the values are fully consumed, an interrupt is generated that can be caught by the CPU and used to trigger a buffer data update. As a third example, a DMA controlled interface can be used. Then, the component is connected to the RAM area 134 and a DMA channel is configured to perform the specific use of the data that is specific to the application. Once the component requires a next value it signals this to the DMA channel, which in turn is responsible for providing the next value to the component. The value is copied by the DMA channel from the RAM buffer, and an interrupt can be configured to be generated automatically at a certain point, such as when the RAM buffer has been read fully or halfway through. For instance, a first interrupt can be triggered after a first share (such as half) of the RAM buffer compare values have been consumed, indicating that the first share can be updated, and a second interrupt can be triggered after a second share (such as the other half) of the RAM buffer compare values have been consumed, indicating that the second share can be updated, and so forth. This interrupt can then be caught by the CPU 131 and acted upon accordingly, such as by updating the values in the RAM buffer. As the CPU 131 knows where in the read cycle the process currently is, it can update the RAM buffer values that are currently not read.

[0212] In exemplary embodiments of the present invention, the second or third examples can be used for consumption and/or updating of the RAM buffer in the RAM area 134. Hence, the compare value copying function 135 can be or comprise a DMA channel, that can be a circular or cyclic DMA channel such that after it has reached the end of the RAM area 134 it continues copying from a beginning of the RAM area 134 again. The DMA channel can be arranged to notify the CPU 131, such as using an interrupt, when a certain point, such as half or full consumption of the values, has been reached, providing information to the CPU 131 about the current read state of the RAM area 134 so that the CPU 131 can act accordingly and update different parts of the RAM area 134 accordingly.

[0213] Alternatively, the compare value copying function 135 can be or comprise an ISR (Interrupt Service Routine) being executed in response to an IRQ, Interrupt Request, the ISR being arranged to signal, via an interrupt, to the CPU 131 that a new compare value is needed from the RAM

buffer. When the IRQ signal is emitted, the CPU 131 executes the ISR, which is arranged to update the timer function 132 with a new compare value from the RAM buffer. Hence, the compare value copying function 135 can be configured to react to an interrupt produced by the IRQ in connection or reaction to the timer counter value reaching its full cycle value, the reaction then comprising copying a new compare value from a next or subsequent memory position of the RAM area 134. Further alternatively, an IRQ can be used to alert, via an interrupt, the CPU 131 that the RAM buffer has been fully consumed and that it is time for the CPU to update the RAM buffer compare values.

[0214] As is illustrated by the above example, the repeated control signal pattern can be defined to be longer than the HRTIM period, in other words the time it takes for the timer counter variable to complete a full cycle. Moreover, one or several individual pulses forming part of the repeated control signal pattern can be longer than the HRTIM period, meaning that at least one compare value will be equal to or more than the number of HR clock cycles in one HRTIM period. This way, the repeated control signal pattern is in a sense independent of the HRTIM period, since both individual pulses and the entire control signal pattern can extend in time beyond the boundaries of a single HRTIM period.

[0215] In the following, the mechanisms for defining the repeated control signal will be explained and exemplified in closer detail. In general, the LED driver 100 can be arranged to vary at least one, such as both, of firstly, a number of pulses provided across the repeated control signal pattern, and secondly, a respective pulse width of one or several of a set of one or several pulses provided across the repeated control signal pattern, in way so that different desired time-averaged currents (or voltages) can be provided to the driver output 182.

[0216] As will be seen from the below, the LED driver 100 can generally be arranged to gradually increase the time-averaged applied voltage or current to the driver output 182, as the dimming value is gradually increased from a low level to a high level, by first increasing a pulse width of one or several pulses provided across the repeated control signal pattern and to thereafter, to further increase the light intensity, increase a number of pulses provided across the repeated control signal pattern. As we will see, this can then be repeated by growing a respective pulse width of one or several such added pulses, thereafter adding one or several additional pulses, and so forth.

[0217] Continuing on the example discussed above, a “pulse period”, in the PWM sense, can be defined to be a concatenation of three compare values, so that 128 individual such PWM pulse periods are used together to define the repeated control signal pattern and hence the instantaneous shape of the binary control signal. It is realized that the repeated control signal pattern can have any arbitrary shape, for instance so that individual pulses are distributed in a less regular manner than forming trains of such “PWM pulses”, but for the present example this is the case. It is particularly noted that one or several parts of the general methodology described regarding how individual pulses are introduced and grown can be applied for other pulse patterns across the repeated control signal pattern. When a particular part of a pulse pattern can be analyzed in terms of a PWM pulse, it is herein denoted “PWM like”. It is realized that this terminology is used to facilitate understanding of the invention, and is not intended to limit the described embodiments to PWM in its conventional meaning (having a single repeated pulse the duty cycle of which is varied over time).

[0218] Using such three-compare-value PWM pulse periods, a threshold pulse width (the threshold width being defined as a width reached before a new pulse is introduced) is set to a value under 169998, such as 10000. For the lowest light powers, only one PWM pulse will be non-zero across the repeated control signal pattern, but as the dimming value is increased the pulse width of this single PWM pulse will be increased until it reaches the threshold pulse width in question. At this point, a second PWM pulse is introduced and starts to grow with increasing dimming values. Once the second PWM pulse has reached the threshold pulse width, a third pulse is introduced and starts to grow, and so forth. When all 128 pulses have reached the threshold pulse width, the compare values are adjusted so that the respective pulse widths of all PWM pulses are widened simultaneously. It is noted that the compare values can be set so that all PWM pulses are treated in the identical same manner as described, but alternatively so that different PWM pulses have slightly different properties, such as being associated with different threshold pulse widths before the next pulse is introduced or where in the repeated control signal pattern the pulse in question is placed. This provides a way to tailor the pulse-defining algorithm to achieve very precise dimming even for hardware platforms with various hardware constraints, such as a minimum or maximum number of clock cycles for the compare value and similar. If the pulse widths are controlled individually, degradation of bit resolution can be avoided and as a result the

effective number of bits for the control signal can be caused to be constant and given as an expression of the total number of clock cycles in the repeated control signal pattern, which in this example results in:

$$nBits = \frac{\log(128 \cdot 3 \cdot 56666)}{\log(2)} \approx 24.375 \text{ bits.}$$

The time spent in the high level (instead of the low level), in relation to the total time of the repeated control signal pattern defines a sort of PWM-like “duty cycle”.

[0219] Generally speaking, the LED driver 100 can be arranged to distribute the at least one pulse of the repeated control signal pattern across the repeated control signal pattern over a set of predetermined and/or evenly distributed, or substantially evenly distributed (such as to a precision allowed by the distribution mechanism), time pulse positions across the repeated control signal pattern. In some embodiments, this distribution can take place according to a bit-reversal of a binary representation of a number, the number in turn describing or corresponding to the index of the pulse within the first-channel control signal pattern. This will now be exemplified.

[0220] Hence, let $\{P_{I_0}, P_{I_1}, P_{I_2}, \dots, P_{I_{127}}\}$ be the determined (desired) pulse widths of the 128 individual PWM pulses comprised in the repeated control signal pattern, where $I_k \in [0, 127]$. Furthermore, let M be the threshold pulse width before an additional PWM pulse is introduced. Before the highest frequency is reached, this results in a sequence according to $\{M, M, \dots, M, x, 0, 0, \dots, 0\}$, where $x \in [0, M)$ and N is the number of PWM pulses having a pulse width of M . If T is the total HR clock cycle length $T = 56666 \cdot 3 \cdot 128 = 21759744$ of the three-compare-value PWM pulse periods and the desired average PWM-like duty cycle (instantaneous intensity I), the sequence will fulfill the equation $M \cdot N + x = T \cdot I$.

[0221] Now the mapping I_k can be determined. If $I_k = k$, all pulses would fall after each other followed by a long break, resulting in a large 250 Hz component, in turn risking the result of flickering and disturbing sounds. To solve this, the mapping I_k can be designed to maximize the resulting PWM frequency. One way to achieve this is to represent k as a binary number, such as a 7-bit number, and then reverse or swap the bits and use the mapping $I_k = k_{swap}$. For the first values, the following is achieved:

<u>k</u>	<u>0</u>	<u>1</u>	<u>2</u>	<u>3</u>	<u>4</u>	<u>5</u>
<i>k_{bin}</i>	0000000	0000001	0000010	0000011	0000100	0000101
<i>k_{swap}</i>	0000000	1000000	0100000	1100000	0010000	1010000
<i>k_{swap}</i> (dec)	0	64	32	96	16	80

<u>k</u>	<u>6</u>	<u>7</u>	<u>8</u>	<u>9</u>	<u>10</u>
<i>k_{bin}</i>	0000110	0000111	0001000	0001001	0001010
<i>k_{swap}</i>	0110000	1110000	0001000	1001000	0101000
<i>k_{swap}</i> (dec)	48	112	8	72	40

[0222] This is visually illustrated in Fig. 6, in the form of a graph wherein the height of each bar symbolizes the order in which the corresponding PWM pulse is introduced, higher bars being introduced earlier (the first bar is introduced for $k = 0$). This way of introducing pulses across the repeated control signal pattern guarantees that the pulses are as spread-out as possible while not drawing too much compute resources. It is realized that this distribution mechanism can be used also for less regular pulse distributions, so that the introduction of pulses is distributed using bit binary swapping or a similar mapping mechanism even if the pulses themselves are not perfectly evenly distributed across the repeated control signal pattern.

[0223] Hence, for the binary system, where numbers are represented in a series of 0s and 1s, the bit reversal process is as described above. However, this concept of reversal isn't confined to the binary realm. It extends to more complex systems. In a more general case, for instance, a mixed-radix base of primes is used. Unlike the binary system, wherein each digit has a base of 2, mixed radix systems involve numbers with different bases at different positions. In a mixed-radix base of primes, the primes are sorted from a highest to a lowest number (the lowest prime is the least significant position). Then the order is reversed to be lowest-to-highest (highest prime is least

significant position). Then, given a starting frequency, say 250 Hz, the higher end of the interval (which is 32 kHz in the example above) can instead be selected arbitrarily, to be for instance 24 kHz. Furthermore, if the ratio between the highest frequency and lowest frequency would not be a power of 2, a mixed radix base could instead be used. This could then potentially result in an even better dimming performance. As a specific example, assume the ratio is $24000/250 = 96 = 3 \cdot 2^5$. Since 96 can be factored as $3 \cdot 2^5$, a mixed radix base having bases $\{3, 2, 2, 2, 2\}$ can be used to represent the number. The bases are ordered from highest to lowest such that the lowest base has the least significant value. The representation becomes $\{s_5, s_4, s_3, s_2, s_1, s_0\}$. Now, if a number is expressed in this base, the possible values ranges from 0 to 95 and are described by a sequence $\{s_5, s_4, s_3, s_2, s_1, s_0\}$. Then, the representation is reversed to $\{s_0, s_1, s_2, s_3, s_4, s_5\}$ and is observed using the mixed radix base $\{2, 2, 2, 2, 3\}$. Hence, the process of "bit-reversal" described above is here generalized to "digit-reversal" and then consists of reversing the sequence into $\{s_0, s_1, s_2, s_3, s_4, s_5\}$ and computing the new index using the base $(2, 2, 2, 2, 3)$, where the base is now ordered from lowest to highest. Based thereupon, the index is calculated, whereby the sequence $(0, 1, 2, 3, \dots)$ would be mapped to $(0, 48, 24, 72, 12, 60, 36, 84, 6, \dots)$

[0224] In this and in other embodiments, a duration of the repeated control signal pattern can be constant across different desired time-averaged currents provided to the driver output 182. In other words, in some embodiments the duration does not change with the dimming value but instead the concentration of high-value clock cycles across the control signal pattern is instead changed by altering the pulse pattern.

[0225] As another alternative, it would be possible to allow, by way of example, a 250 Hz pulse signal to grow, as the dimming value increases, in pulse width until a certain threshold pulse width was reached. Thereafter, as the dimming value increases further, the period time could be decreased continuously to introduce the pulses more and more often over time. Once the frequency reaches a certain maximum value, such as 32 kHz, the pulse width can again be increased until 100% duty cycle is achieved. This type of modulation works particularly well with single-channel LED drivers 100 and can also be achieved using the multi-HTRIM-period pulse structures generally described above.

[0226] However, for a multi-channel LED driver 100, the fact that the duration of the respective repeated control signal pattern is not the same for different channels means that there will be a drift in terms of instantaneous current requirements across the different channels. To clarify the consequences of this, one can assume two channels with PWM duty cycles $D_1 > 0$ and $D_2 > 0$, $D_1 \neq D_2$, meaning in the latter example that the corresponding PWM frequencies f_1 and f_2 are not equal, $f_1 \neq f_2$. When the respective channel is leading (high value for the binary control signal), an increased current requirement arises, in turn causing the voltage on the DC bus 121 to decrease temporarily. The size of this sinking depends, inter alia, on the size of the LED load 10 and the amount of capacitance on the DC bus 121. This means that, if the channels are active at the same time, a certain current requirement will arise, but if they are active at different times a different current requirement will arise. Interference will then arise on sums and differences of the respective frequencies, meaning that the frequency $f_1 - f_2$ will have a non-zero amplitude. If, for example, $f_1 \approx f_2$, a low-frequency flickering may occur, which is not desirable. Hence, using $f_1 = f_2$ configurations, for instance according to the above example, is often more suitable for multi-channel LED drivers 100 than $f_1 \approx f_2$ configurations.

[0227] Generally, the relative current requirement across different channels can be arranged to be stable, and not drift. To this end, one respective periodic signal (such as the repeated control channel pattern) can be generated on each channel, where the periodicity is the same for all channels, and where the periodicity can be as long as the longest PWM period of PWM pulses together forming the periodic signal. In other words, the signal can be constructed from a sequence that is repeated, and the sequence is generated as a concatenation of individual PWM-like pulses. Since the sequence is periodic, the voltage on the DC bus 121 will also be periodic with the same period, resulting in a constant light contribution from a pulse so long as it is not moved in the sequence. If a pulse is moved to a different position, there is a risk that a notch results in the dimming curve. Once a pulse has been introduced at a certain point in the sequence as the dimming value is increased, the LED driver 100 can be configured to keep that introduced pulse in that location in the sequence as long as the dimming value is increased.

[0228] Generally, the LED driver 100 can comprise, in addition to the first-channel electric driver output 182', a second-channel electric driver output 182'' and any third-channel 182''' or further electric driver output. Like for the first-channel electric driver output 182', the LED driver 100 can

be arranged to provide a current to the second-channel driver output 182'' and any further driver output 182''', etc., according to a corresponding binary control signal, such as a second-channel binary control signal. The LED driver 100 can also correspondingly comprise a second-channel timer function 132'' and any third-channel 132''' or further timer function, being configured to update a corresponding second, third or further-channel timer counter variable at a second, third or further-channel timer frequency. The second 132'', third 132''' or further-channel timer function can be configured to, for each update, compare the second, third or further-channel timer counter variable to a set second, third or further-channel compare value. The second 132'', third 132''' or further-channel timer function can be configured to, in case the timer counter variable in question has reached or gone past the set compare value in question, cause the binary control signal in question to switch between a corresponding set of binary states, such as for the second-channel binary control signal between a third binary state and a fourth, different binary state. This functionality can hence correspond to what has been generally described above in relation to the binary control signal and specifically to the first-channel binary control signal.

[0229] Then, a duration of a repeated second, third and/or further-channel control signal pattern of the second, third and/or further-channel binary control signal can be longer than the time it takes for the second, third and/or further-channel timer counter variable to complete a full cycle. As is the case for the first-channel control signal pattern, the second, third or further-channel control signal pattern can each comprise one or several pulses.

[0230] Moreover, the LED driver 100 can then be arranged to update the set second, third and/or further-channel compare value at least two times during each individual second, third and/or further-channel control signal pattern, respectively.

[0231] In such cases, a duration of the first-channel control signal pattern can be an integer multiple of, such as the same as, a duration of the second, third and/or further-channel control signal pattern. This will result in no intra-channel drift. It is noted that the same effect is achieved if the first-channel control signal pattern is an even fraction of a duration of the second, third and/or further-channel control signal pattern, in case the duration of the first-channel control signal pattern is the shorter duration.

[0232] To achieve as stable DC voltage as possible, it is desired for the LED driver 100 to draw as smooth a current as possible. If it is assumed that the corresponding PWM duty cycle is, for instance, 10% across all channels, and that the activated binary control signal sequence activates all channels at the same time in the sequence, the current requirement would be unnecessarily high, followed by an unnecessarily long pause before the next current requirement would arise.

[0233] If instead an offset is introduced on the channel level, the offset being different for each channel, the current requirement would not arise simultaneously on each channel, in turn resulting in a smoother overall current requirement. As the frequency contents in the current requirement increases, the capacitance on the LED driver 100 does not need to supply the circuitry with current during as long a time, yielding a lower capacitance requirement and by consequence lower manufacturing costs.

[0234] Generally, the first-channel binary control signal can be time-offset in relation to the second, third and/or further-channel binary control signal by a respective offset value that is smaller than the first-channel control signal pattern duration.

[0235] For LED drivers 100 having three or more electric driver outputs 182', 182'', 182''', each of the respective binary control signals for the different channels can be offset by a value lower than the duration of the first-channel control signal pattern, and the respective time-offsets of the at least three control signal patterns can be distributed over a set of predetermined and distributed time offsets across the first-channel control signal pattern. The distribution of the at least three control signal patterns can be even, or substantially even (given available granularity on the hardware used, for instance), across the repeated control signal pattern duration.

[0236] For instance, bit reversal similar or corresponding to the above-described manner of distributing pulses across the repeated control signal pattern can be used to distribute the offsets for the respective binary control signal of different channels. If M_i is the offset for channel i , the offset values $M = \{0, 64, 32, 96, 16, 80, 48, 112, 8, 72, 40, 104\}$ for a twelve-channel LED driver 100. This yields a distribution across the channels that generally provides a smooth current requirement and therefore smoother voltage and lower capacitance requirements. For multi-channel LED strips, this yields even less flickering, since the instantaneous light intensity decreases at the same time as the frequency increases.

[0237] In general, the distribution of offsets across different channels can take place according to a bit-reversal of a binary representation of a number, the number in turn describing or corresponding to a channel index of electric driver outputs $182'$, $182''$, $182'''$. The distribution can be across the first-channel control signal pattern duration used.

[0238] The following is an illustration of a procedure of the type generally described above, designed to use a variadic frequency for driving a constant voltage LED load 10 and to avoid stutter, flicker and interference patterns.

[0239] N is the maximum number of pulses in a periodic signal (the repeated control signal pattern). All pulses have one and the same threshold pulse width W_{max} measured in clock cycles, equal to one N th of the total number of clock cycles in the periodic signal, T_{total} .

[0240] $W[0], W[1], \dots, W[N-1]$ are the N slots that hold the counter values for each respective pulse width.

[0241] The desired intensity I_{avg} is a value in the range $[0,1]$.

[0242] The task at hand is now to fill all slots such that $I_{avg} = \frac{1}{N \cdot W_{max}} (\sum_{i=0}^{N-1} W[i])$. The slots can be filled using the flow diagram shown in Fig. 7.

[0243] Left to do now is to decide in which order new slots should be chosen. If $W[0]$ would be filled first, followed by $W[1]$, $W[2]$ and so on, a large low-frequency component would be present in the signal. To minimise flicker as much as possible, after the first slot has been filled, the next slot to be filled should be at the furthest distance from the first slot. This will make sure that low-frequency content of the signal is always minimized. So if the first slot that was filled was $W[0]$, then the next one should be $W[N/2]$. After that it would proceed in a binary fashion, inserting new pulses at the furthest distance away from the existing pulses. If N can be written as $N = 2^m$ for some integer m , this type of indexing can be computed by doing an m -bit reversal of a linearly increasing index i .

[0244] Given the constraints of the microcontroller that was used in the setup used by the inventor, the high resolution timer was limited to 16 bits. This is hence merely an example. With a highest equivalent clock frequency of $32 \cdot 170 \text{ MHz} = 5.44 \text{ GHz}$, the lowest possible PWM

frequency is then achieved when the timer period is at its maximum value, being equal to $65535 - 96 = 65439$. Dividing the equivalent clock frequency by this number, one gets about 83 kHz , which is too high for the task at hand. By letting each slot $W[i]$ consist of three counter periods of 56666 clock cycles each, the maximum frequency is instead $\frac{5.44e9}{3 \cdot 56666} = 32 \text{ kHz}$. By letting $N = 128$, the lowest frequency is then 250 Hz .

[0245] For any other set of minimum and maximum frequencies, the following procedure can be used:

- Given is the clock frequency f_{TIM} of a timer peripheral, for example $f_{TIM} = 170 \text{ MHz}$ · $32 = 5.44 \text{ GHz}$
- Define a ratio N between the highest and lowest PWM frequency $N = f_{max}/f_{min}$, for example $N = 128$.
- Define a target frequency $f_{minTarget}$ of the lowest frequency content of the signal, for example $f_{minTarget} = 250 \text{ Hz}$.
- In the formula $T_{approx} = f_{TIM}/(f_{max} \cdot b)$, find the lowest integer b such that the result is below the maximum counter value. This gives both T_{approx} and b , for example $T_{approx} = \frac{f_{TIM}}{f_{max} \cdot b} = \frac{5.44e9}{32000 \cdot 3} \approx 56666.667$ and $b = 3$.
- Truncate T_{approx} to an integer, for example $T = 56666$.
- The example values gives

$$f_{max} = f_{HRTIM}/(b \cdot T) = 5.44e9/(3 \cdot 56666) \approx 32000.376475 \text{ Hz} \quad f_{min} = f_{max}/N \approx 250.002941 \text{ Hz}.$$

[0246] N defines the number of different pulse widths that are to be generated before the sequence starts over. Each pulse has a maximum length of $b \cdot T$ clock cycles, for example $3 \cdot 56666 = 169998$ clock pulses. Define $W[i]$ to be the pulse width of pulse i , where i is an index ranging from 0 to $N - 1$. The total on-time is $W[0] + W[1] + \dots + W[N - 1]$ and the total time is $T \cdot b \cdot N$ clock cycles, for example $56666 \cdot 3 \cdot 128 = 21759744$. If the controller input signal is equal to the average light intensity to be generated with range $[0,1]$, the quantity can be defined as

$$I_{avg} = \frac{\langle \text{total on-time} \rangle}{\langle \text{total time} \rangle} = \frac{W[0] + W[1] + \dots + W[N-1]}{T \cdot b \cdot N}.$$

[0247] If all $W[i]$ would be the same value, the control signal being generated would be a pure PWM signal with frequency f_{max} and the duty cycle would be $D = I_{avg} = W[i]/(b \cdot T)$. If all $W[i]$ -values would be zero except for one index i , the control signal being generated would be a pure PWM signal with frequency f_{min} and with duty cycle $D = I_{avg} = W[i]/(N \cdot b \cdot T)$. In the general case, the frequency content of the signal is mixed, dependent on which bins are filled. However, the number of pulses per second is $f_{min} \cdot \langle \text{number of nonzero } W[i] \rangle$ and the minimum frequency component of the signal being generated will not be lower than f_{min} .

[0248] The algorithm can be summarized as follows:

- Configure a timer peripheral such that a periodic signal of N pulses can be generated with the desired f_{min} and f_{max} . N is selected such that $N = 2^m$, for some m .
- Decide a minimum pulse width M that is going to be used. The lower the value, the faster the frequency will go from f_{min} to f_{max} when increasing intensity.
- Define n to be the number of slots that can be filled at least with the pulse width M . n is computed by $n = \frac{T_{total} \cdot I_{avg}}{M}$ and then truncated to its integer part.
- Define an array that is to be filled up sequentially, $Z[0], Z[1], \dots, Z[N-1]$.
- If $n < N$, fill up the first n slots in Z with the value M and set the next slot to the residual, $Z[n] = T_{total} \cdot I_{avg} - n \cdot M$. All other slots are set to zero.
- Otherwise if $n \geq N$, fill all slots as equally as possible: First, set all values to $Z[i] = T_{total} \cdot I_{avg}/N$, where all values are truncated to their integer parts. Then compute the residual $R = T_{total} \cdot I_{avg} - Z[0] \cdot N$. This is a value in the range $[0, N-1]$. Increase the first R slots with one to minimise the residual.
- Scramble the indices by setting $W[rev(i)] = Z[i]$, where rev is the m -bit reversal function.

Second aspect of the invention

[0249] Turning now instead specifically to the second aspect of the present invention, it has been understood from the above that the binary control signal is, or is an analog representation of, a digital control signal in turn used to switch the LED load 10 on and off. However, the drive circuitry 140, the drive switch 180 and the LED load 10 itself all have dynamic electrical properties that will

alter the resulting signal actually delivered to the LED load 10. If, for instance, a PWM signal with duty cycle D is used as the control signal based on which the LED load 10 is driven, the actual average current through the LED load 10 will differ from i_{max} times D , where i_{max} is the current through the LED load 10 when $D = 1$.

[0250] As an example, in case the raw or compensated binary control signal is provided to a MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor) that in turn is used to output the drive current to the LED load 10, the relationship between the gate voltage V_{gs} and its internal resistance R_{ds} is complex and depends on several factors. When the drive circuitry 140 takes a non-zero time $t > 0$ to charge V_{gs} this complex relationship will give rise to a deterministic (but normally unknown) change of R_{ds} during the charge and discharge process. As the time t becomes so long so that a visible amount of light is emitted before the charging is completed, this will result in such light being emitted before the current through the LED load 10 has reached its maximum. Again, how much such light is emitted is determined by a complex and normally unknown relationship that is determined both by the transistor itself and also the drive circuitry 140. It is noted that the drive circuitry 140 can be as described below in connection to the third aspect, but that any drive circuitry 140, such as using a simple series-connected resistor, will give rise to complex dynamic behavior to some degree. For example, a resistor will be associated with a certain precision and manufacturing variability, so that every resistor of the same type does not have the exact same properties. Even if resistors with higher quality are selected, any transistors used in the drive circuitry 140 will have dynamic properties, and so forth.

[0251] The amount of light emitted from a light source, such as an LED, is directly proportional to the current. Hence, if the current is integrated over time, a measurement of the total amount of emitted light can be achieved. The intensity of the light can be defined as

$$I = \frac{\int_0^T i(t) dt}{i_{max} T},$$

Where T is the period time for the signal (the period of the repeated control signal pattern), $i(t)$ is the varying current through the LED load 10 and i_{max} is the current reached at 100% duty cycle (binary control signal at constant high value).

[0252] Now, the duty cycle D can be defined as the amount of time that the currently used repeated control signal pattern is in the high value divided by the period of the currently used repeated control signal pattern. In the ideal case, $I = D$. However, due to the above-described complex relationship this equation will not hold. But the relationship between I and D can be measured, such as by connecting a typical LED load 10 or another electric load to the LED driver 100 and then measure $I(D)$.

[0253] In the following, an example will be presented to illustrate this. Since the frequency change on the output signal of the LED driver 100 typically adds extra complexity, the frequency was first fixed to 250 Hz for all intensities. $I(D)$ was then measured and the results are presented in Fig. 8. The dotted line is $I = D$.

[0254] The present inventors propose to find the inverse of the measured function $I(D)$, that is $D(I)$, and then to use $D(I)$ to find a certain duty cycle of the binary control signal to use, given a desired light intensity.

[0255] To better understand how each PWM-like pulse is altered by the LED driver 100, let H be the system consisting of the drive circuitry 140, drive switch 180, and a typical LED load 10. Furthermore, let s be a binary control signal going into this system and let x be any single PWM-like pulse in s . Let $y = H(x, e)$ be the equation that describes how x gets modified by the system H . In the equation, x and y are pulse widths measured in seconds, where y can be computed by taking the time integral of the pulse and dividing with its maximum value (yielding an effective pulse width for a constant maximum-value pulse). e is any set of external variables that may affect the system, which could be ambient temperature, average value of s , maximum current i_{max} , drive supply voltage, etc. Depending on the scope of H , x and y could represent pulses of voltages and/or currents.

[0256] Fig. 4d illustrates a non-square pulse further illustrating the concept of “effective pulse width” in the present sense. It is a typical waveform of a pulsed current through a LED load. Since the amount of light is proportional to the current, the time integral of the waveform measures the amount of light emitted from one single pulse. If this time integral is set to be equal the time integral of an ideal rectangular pulse with maximum current I_{max} , the rectangular pulse will represent the same amount of light and an effective pulse width. Hence, in Fig. 4d, showing a

pulse, I_{max} is a maximum (current) level of the pulse, typically occurring on an upper plateau of the pulse. $i(t)$ is the level (the current in this case) as a function of time. W_{eff} is the effective pulse width of the pulse. It is realized that

$$W_{eff} = \frac{1}{I_{max}} \int_{t=0}^T i(t) dt.$$

The relative intensity I can then be computed as W_{eff} divided by the period time T and then yields a value between 0 and 1.

[0257] For systems considered in this analysis, $H(x, e)$ will be a continuous function that have a strictly positive and continuous derivative for all values x that are large enough to produce an output signal $y > 0$. Thus, by the inverse function theorem, an inverse function $x = H^{-1}(y, e)$ exists. If y is the wanted pulse with, x can be computed if H^{-1} is known, and if x is fed to H , it will produce y . Thus, H^{-1} together with H will produce the identity function, $H(H^{-1}(y, e), e) = y$.

[0258] By measuring y for different values of x over the whole spectrum of relevant pulse widths, data points (x_i, y_i) can be gathered for any set of external variables e .

[0259] A parametric model M can now be found such that $M(y, e, v_M) \approx H^{-1}(y, e)$, where v_M is the set of internal variables for M . For an ideal system, the incoming and outgoing PWM-like pulse widths would be the same, $H_{ideal}^{-1}(y) = y$, so it may make more sense to analyze the discrepancy from the ideal:

$$M(y, e, v_M) = \frac{H_{ideal}^{-1}(y)}{G(y, e, v_M)} = \frac{y}{G(y, e, v_G)},$$

where G is another parametric model to be found. As the human eye has higher sensitivity at lower light levels, the model error should be smaller for lower intensities. Also, for low intensities, the PWM-like pulse widths are shorter and the dynamics of H will have a larger impact on D . Thus, it may be reasonable to expand the input values y in order to get more details for small values of y . This can be done by applying a non-linear function to y , such as $\log$, pow or sqrt . In the following example, the logarithm of the intensity was used:

$$G(y, e, v_G) = F(\log(y), e, v_F),$$

where F is another parametric model.

[0260] As drive circuitry 140 and drive switch 180 behavior usually contains exponential relationships, the curve fitting can be simplified by removing this behavior by taking the logarithm of both sides and finding a model for the residual shape:

$$\log(G(y, e, v_G)) = \log(F(\log(y), e, v_F)) = R(\log(y), e, v_R),$$

where R is another parametric model.

[0261] Putting this together with the gathered data (x_i, y_i) , one gets

$$x_i \approx H_{ideal}^{-1}(y_i)/F(\log(y_i), e, v_F) = y_i/\exp(R(\log(y_i), e, v_R)) \Rightarrow$$

$$R(\log(y_i), e, v_R) \approx \log(y_i/x_i),$$

and after finding R , the parametric model M can be computed by

$$M(y, e, v_M) = y \cdot \exp(-R(\log(y), e, v)).$$

[0262] Left then, is to find the parametric model R using the relationship $R(\log(y_i), e, v_R) \approx \log(y_i/x_i)$. This relationship is plotted in Fig. 9 for the present measurement example.

[0263] There are several ways to model R given the input variable $\log(y)$ and both parametric and non-parametric approaches can be used. For example, spline interpolation, polynomial approximation, lookup tables, kernel functions and parametric models can all be used with their respective pros and cons. One possible approach is to model R as two different low-degree polynomials, one such polynomial to the left and one such polynomial to the right of the maximum value of R . These two polynomials can then be fused together, for instance using a sigmoid function.

[0264] This principle is illustrated in Fig. 10, wherein, the black triangles are measured data. The full-line curves not following the black triangles in the top graph are the two polynomials and the sigmoid function. The sigmoid function itself is shown in the bottom graph. The full-line curve following the black triangles is the resulting model R .

[0265] The polynomials matching the curve to the left and right of its maximum have degrees 3 and 2 respectively. The sigmoid function $S(x)$ consists of two exponential functions that are connected by letting $S(x)$ and $S'(x)$ be continuous at a centerpoint x_c :

$$S(x) = f_1(x) \text{ if } (x < x_c), f_2(x) \text{ otherwise, where}$$

$$f_1(x) = \exp(k_1(x - a_1)) \text{ and}$$

$$f_2(x) = 1 - \exp(-k_2(x - a_2)).$$

[0266] Continuity of $S(x)$ and $S'(x)$ at $x = x_c$, give the parameters a_1 and a_2 :

$$a_2 = x_c + \log(k_1/(k_1 + k_2))/k_2$$

$$a_1 = x_c - \log(1 - \exp(-k_2(x_c - a_2)))/k_1.$$

[0267] This gives an asymmetric sigmoid function when $k_1 \neq k_2$.

[0268] Given the two polynomials and the sigmoid function, a total of 10 parameters are then needed to approximate H^{-1} , namely $p_{11}, p_{12}, p_{13}, p_{21}, p_{22}, k_1, k_2, a_1, a_2, x_c$, where $p_{11}, p_{12}, p_{13}, p_{21}, p_{22}$ are the parameters of the two polynomials used.

[0269] These unknown parameters can be found by any suitable type of optimization algorithm. One possible approach is to minimize the squared error of the PWM-like pulse widths before the system H , e.g. using the differences in x : $\Delta x = M(y_i, e, v) - x_i$, or the logarithm of those values. However, as the quantity y represents the actual PWM-like pulse width after x has passed through H , a better approach would be to compute the error in terms of y since this is the quantity of interest. For any computed value $x_M = M(y_i)$, the closest value x_j in the sampled data set (x_i, y_i) can be used to look up y_j , such that the difference $\Delta y = y_i - y_j$ can be computed and used as the error.

[0270] Generally, a method according to the second aspect of the invention for configuring the LED driver 100 for subsequent dimming of the LED load 10 is illustrated in Fig. 11 and pertains to the case in which the variable current being provided by the LED driver 100 to the LED load 10 is

modulated using at least one transistor of the LED driver 100 based on the binary control signal described above.

[0271] As also described above, the binary control signal comprises or is made up of the repeated control signal pattern, that in turn at each time has an instantaneous time-averaged value as time-averaged over the control signal pattern used at the time in question. This instantaneous time-averaged value is denoted the “duty cycle” of the binary control signal above.

[0272] In a first method step 1101, the method starts.

[0273] In a subsequent step 1102, the LED driver 100 is connected to the LED load 10, or alternatively to a different load 20. See Fig. 12, showing the LED driver 100 driving the LED load 10, in turn radiating light that is detected by a light sensor 11; and the LED driver 100 alternatively driving a different electric load 20, a current through which is in turn measured by a current measuring sensor 21. Of course, the resulting current through the electric load 20, or the light emitted by the LED load 20 can be measured in many different direct or indirect ways, and that Fig. 12 is merely an example. For instance, a current clamp can be used to measure the current. Furthermore, instead of measuring the light emitted from the LED load 10, a current passing through the LED load 10 can instead be measured.

[0274] In a subsequent step 1103, the LED driver 100 is operated to provide the variable current to the LED load 10 or to the other load 20, in the general way described herein, using several different instantaneous time-averaged values for the binary control signal. It is noted that as one single run-through of the control signal pattern could suffice, in some embodiments it is advisable to use several repeated control signal patterns one after the other, as would be the case during continuous operation of the LED driver 100 at the dimming value corresponding to the control signal pattern in question. In other embodiments, multiple measurements can be made consecutively of different controlled duty cycle values. For instance, a slow dimming up or down can be used, by gradually changing the duty cycle of the repeated control signal pattern after each or a few control signal pattern run-throughs, and measuring the current or light as described, providing a plurality of measurements merely involving performing a dimming action and taking the measurements.

[0275] In a subsequent step 1104, for each of the several different instantaneous time-averaged values, a respective measurement value is obtained, such as by reading the sensor 11 or 21, of a quantity, such as the emitted light or the current through load 20. This quantity, in turn, can then be, or be unambiguously related to, at least one of, firstly, an average current flowing through the LED 10 or the load 20, and, secondly, an average light intensity emitted by the LED 10. This way, a measured first relationship is obtained of the absolute or relative current/light intensity as a function of the instantaneous time-averaged value. It is understood that steps 1103 and 1104 can take place iteratively, whereby a first instantaneous time-averaged value is used and a first measurement is made, whereupon a second instantaneous time-averaged value is used and a second measurement is made, and so forth, for instance using a dimming control scheme as mentioned above. It is understood that this step 1104 of obtaining the measurement values and the first relationship can also be viewed as a step of automatically determining the first relationship based on the obtained measurement values.

[0276] The first relationship can be a value-by-value relationship between each absolute or relative current/light intensity as a function of each corresponding instantaneous time-averaged value. This is in contrast to the second relationship, described below, that defines the properties of the function itself, of the absolute or relative current/light intensity in relation to the instantaneous time-averaged value. It is realized that configuration information resulting from the presently described method can simply comprise a table or similar data structure with a set of absolute or relative current/light intensity together with corresponding instantaneous time-averaged values, useful for determining by simple lookup a particular instantaneous time-averaged value (with a corresponding determined repeated control signal pattern) based on a desired absolute or relative current/light intensity. Alternatively, the configuration information can comprise information regarding the second relationship, providing the possibility to calculate, based on the configuration information, the particular instantaneous time-averaged value given a desired absolute or relative current/light intensity.

[0277] In general, either an absolute value for the current or light intensity can be measured, or a relative value of the same metric. For relative values, the metric can be put in relation to a measured current or light intensity for a maximum dimming value, and then any measured value for a lower dimming value can be put in proportion to the value for the maximum dimming value.

To illustrate this, consider a binary control signal with a fixed PWM-like frequency f and a duty cycle (with the above definition) D_i , where i indicates the i :th measured sample. A duty cycle of 1.0 then results in maximum current through the load 20 or light intensity through the LED load 10. First, the maximum current or light intensity is measured by setting $D = 1$, and resulting current is denoted I_{max} (and corresponding for the resulting light intensity in case that is instead measured). Now, for any given duty cycle D_i , the current I_i (or correspondingly the light intensity) can be measured and by normalizing this quantity with I_{max} , an equivalent duty cycle $P_i = I_i/I_{max}$ can be computed. In the following calculations for determining the parametric model, the relative values are then simply used instead of the absolute values. Put more generally, the relative current and/or light intensity can be relative to a measured maximum current or light intensity, respectively.

[0278] For an ideal drive circuitry, the equivalent PWM-like duty cycle is equal to the generated PWM-like duty cycle, $P_i = D_i$, but as non-linear effects are present in the drive circuitry, $P_i \neq D_i$.

[0279] By setting f to f_{min} and varying D_i between 0 and 1, a collection of datapoints (D_i, P_i) can be gathered for constructing a model corresponding to the lowest PWM-like frequency. Likewise, by setting f to f_{max} , datapoints for a model corresponding to the highest PWM-like frequency can be gathered.

[0280] Call these models M_{min} and M_{max} respectively. These models take a number between 0 and 1 as input, corresponding to P , and outputs a compensation value between 0 and 1 corresponding to D :

$$D_{M_{min}} = M_{min}(P)$$

$$D_{M_{max}} = M_{max}(P)$$

[0281] The compensation term is applied on each PWM-like pulse. Given a normalized light intensity I and a fixed PWM-like frequency of f , a control signal pattern of wanted pulse widths are generated. The models are applied on each respective PWM-like pulse in the control signal pattern. If one such pulse is called W , this pulse is related to the relative light intensity by the equation $Wf = P$. Likewise, the compensated term is related to the PWM-like duty cycle by

scaling with $1/f$: $W_{compensated} = D/f$. Putting this together, one gets $W_{compensated} = M(Wf)/f$. Hence:

$$W_{min,compensated} = \frac{M_{min}(W \cdot f_{min})}{f_{min}},$$

$$W_{max,compensated} = \frac{M_{max}(W \cdot f_{max})}{f_{max}}$$

[0282] To mitigate the simplification that was made, $W_{min,compensated}$ and $W_{max,compensated}$ can now be used to construct the final compensation term.

[0283] In case the repeated control signal pattern has a number of PWM-like pulses varying such that the PWM-like frequency is smoothly changed from f_{min} to f_{max} , x can be defined to be a scaling quantity that varies from 0 to 1 over the range where the PWM-like frequency is changing from f_{min} to f_{max} . A good weight factor has been empirically found to be $b = \text{sqrt}(x)$, which is used for the final compensation term:

$$W_{compensated} = (1 - b) \cdot W_{min,compensated} + b \cdot W_{max,compensated}.$$

[0284] In a subsequent step 1105, said configuration information, regarding a mapping of each of several different absolute or relative such current/light intensity values to a corresponding value for the instantaneous time-averaged value, is determined, based on said first relationship. Hence, the mapping can be direct, via a lookup table or similar, or it can be indirect, such as via a parametric model. In other words, configuration information determined based on the first relationship can also be configuration information in the form of information regarding said second relationship. Concretely, the configuration information may for instance be or comprise the parameters of a parametric model of the above-described general type.

[0285] In some embodiments, the method can also comprise, in a step 1106, identifying a parametric model of the second relationship. Such parametric model can then comprise one or several at least section-wise continuous functions determined by a set of parameters. Hence, the functions can be analytical functions as opposed to lookup tables or similar. The parametric model is generally useful for determining the mapping of each of the several different absolute or relative current/light intensity values to a corresponding instantaneous time-averaged value. It is realized

that the identification of the parametric model can comprise using a predetermined parametric model or selecting one parametric model among several possible parametric models depending on the type of LED driver 100 used, or similar. The identifying of the parametric model itself does not have to entail determining or calculating the values of the parameters comprised or used in the identified parametric model.

[0286] Namely, in a subsequent step 1107, the respective values of the parameters that of the identified parametric model that provide a fit, such as a determined best fit according to some suitable optimization algorithm, of the at least one function to the second relationship can be determined. The fit can be determined using any suitable method wherein the second relationship is evaluated for each of the measurement values and corresponding instantaneous time-averaged values. Then, the configuration information will comprise the parameter values.

[0287] In some embodiments, the second relationship comprises the quote of $\frac{g(x)}{g(y)}$, wherein g is a function, x is the instantaneous time-averaged value (of the repeated control signal pattern), and y is the absolute or relative current/light intensity. For instance, $g(x) = x + 0.1$ yields the quote $\frac{(x+0.1)}{(y+0.1)}$. In another example, $g(x) = \frac{1}{(x+0.1)}$ yields the quote $\frac{(y+0.1)}{(x+0.1)}$. Both of these formulations of $g(x)$ have proven useful in practical embodiments.

[0288] Hence, a function $z(y)$ can be approximated to the measurement points $z(y_i) = \frac{g(x_i)}{g(y_i)}$, providing an approximated relationship $z(y) = \frac{g(x)}{g(y)}$. Solving for x , we get $x = g^{-1}(z(y)g(y))$. In other words, $\frac{g(x)}{g(y)}$ is used during the calculation of the configuration information whereas $g(x)$ and $g^{-1}(x)$ are used once the configuration information is used to operate the LED driver 100.

[0289] In general, any bijective function $g(x)$ that is continuous for all PWM-like pulse widths strictly greater than zero can be used in the following way: When finding parameter values for the parametric model, the quantity $\frac{g(x)}{g(y)}$ is used and, when the parametric model with its parameter values is applied, both g and its inverse function g^{-1} is used.

[0290] The parametric model can comprise one or several polynomials, and/or other primitive functions. Generally, the one or several functions can comprise at least one polynomial of degree

one or higher, such as of degree two or higher, such as of degree three or higher. In some embodiments, the one or several functions can comprise two polynomials of degree one or higher, and/or other primitive functions, that are then interconnected by multiplication using a sigmoid function. Any two polynomials can be selected to approximate, by selection of the parameter values of the polynomials, a general shape of the second relationship on either side of a local minimum or maximum thereof.

[0291] The one or several functions can generally be defined in terms of a function $f(y)$, where an absolute value of a first derivative of $f(y)$ with respect to y , in other words $|f'(y)|$, is decreasing, such as monotonously decreasing across the entire used range for y . y is the absolute or relative current/light intensity. For instance f can be the log or sqrt function. From a general point of view, the parametric model M can include a differentiable function $f(y)$ that takes the system variable y as input and has the property $|f'(y_0)| \geq |f'(y_1)|$ for all y_0 and y_1 that are within the defined range for y and where y_0 represents a shorter pulse width than y_1 and; $f'(y)$ is the derivative of f with respect to y . In some embodiments, the input parameter y to $M(y, e)$ is only used through $f(y)$ such that $M(y, e)$ can be written in the form $M(y, e) = N(f(y), e)$, for some parametric model N .

[0292] In general, the sigmoid function can be defined in terms of two functions s' and s'' , selected to yield a continuous function at an expected local minimum or maximum of the second relationship as a function of the absolute or relative current/light intensity, and so that a derivative of the continuous function does not change sign.

[0293] Such sigmoid function can be of the above-described general type, using one or several exponential functions. However, other types of sigmoid functions can also be used.

[0294] For instance, by replacing $\exp(x)$ with $\frac{1}{(1+k(x-x_c+a))^n}$ but otherwise using the same parametric model construction approach as outlined above, a simpler sigmoid function can be created according to the following:

$$f_1(x) = \frac{1}{(1 + k_1(x_c - x + a_1))^n}$$

$$f_2(x) = 1 - \frac{1}{(1 + k_2(x - x_c + a_2))^n}$$

[0295] Let $f_1(x)$ be used when $x < x_c$ and $f_2(x)$ be used when $x \geq x_c$:

$$f(x) = f_1(x) \text{ if } x < x_c, f_2(x) \text{ otherwise}$$

[0296] Exemplary configuration parameter values are $n = 4$, $x_c = 0.5$, $k_1 = 1$ and $k_2 = 2$. n is here the polynomial degree of the sigmoid function and should be selected so that the degree is higher than the polynomial it needs to suppress. For instance, in case two polynomials are used in the parametric model with degrees two and three, respectively, the sigmoid function should have a degree of at least four. x_c is the center point of the sigmoid function, and defines the point where the two functions constituting the sigmoid function are bound together. k_1 and k_2 define the function's rate of change to the left and right side, respectively, of x_c .

[0297] Using continuity of the function and its derivative in the point $x = x_c$, a_1 and a_2 can be calculated according to the following:

$$f_1(x_c) = f_2(x_c) \text{ and } f'_1(x_c) = f'_2(x_c) \Rightarrow a_1 = (s_1 - 1)/k_1 \text{ and } a_2 = (s_2 - 1)/k_2, \text{ wherein}$$

$$s_1 = b \cdot s_2, s_2 = \frac{(1+b^n)^{1/n}}{b}, \text{ and } b = (k_1/k_2)^{1/(n+1)}.$$

[0298] The exemplary parameter values provided above yields a sigmoid function as shown in Fig. 13. Generally speaking, by defining n, k_1, k_2 and x_c , a_1 and a_2 can be calculated using the above formulas to obtain a continuous and asymmetric sigmoid function, where a symmetric sigmoid function is achieved in the special case $k_1 = k_2$.

[0299] The shape of the functional expression for $f_1(x)$ can generally be written as $1/P_1(x)$, where $P_1(x)$ is a polynomial. The shape of $f_2(x)$ can generally be written as $1 - 1/P_2(x)$, where $P_2(x)$ is another polynomial.

[0300] In addition to the direct or indirect information regarding absolute or relative current/light intensity and corresponding instantaneous time-averaged values, the configuration information can also comprise additional information. Such information can be determined automatically by

the LED driver 100, or manually, in connection to the configuration of the LED driver 100, and can comprise, for instance, information regarding the number of pulses in the control signal pattern; a temperature of the LED driver 100 when obtaining the measurement values; and/or a maximum current provided to the LED driver 100. In some embodiments, the measurement of absolute or relative current/light intensity for various instantaneous time-averaged values can take place for several sets of such measurements, and each set of information regarding absolute or relative current/light intensity for various instantaneous time-averaged values can be stored as part of the configuration information together with, or associated with, such additional configuration information. In other words, configuration information regarding the first and/or second relationship can be stored together with corresponding information regarding number of pulses in the control signal pattern; temperature; and/or maximum current provided. Once this information is stored, it can be used using interpolation, as will be exemplified below, when driving the LED driver 100 in states lying between the measured states in a space spanned by the parameters number of pulses in the control signal pattern; temperature; and/or maximum current provided. Concretely, a current operating state as defined by these parameters can be used to determine the parameter values of the parametric model as a corresponding interpolation between established parameter values for known operating states.

[0301] In some embodiments, the configuration information can thus comprise at least two different number of pulses of the control signal pattern; at least two different temperatures of the LED driver 100 when obtaining the measurement values; and/or at least two different maximum allowed currents to be provided to the LED driver 100.

[0302] In a subsequent step 1108, the configuration information is stored for future use. The storing can be in the RAM area 134, elsewhere in the LED driver 100 or in an external storage unit. For instance, the configuration information can be stored in a non-volatile memory such as a ROM memory or a flash memory for use across consecutive power cycles of the LED driver 100. Once the configuration information is stored, it can be used for operation of the LED driver 100 whereby the configuration information is used to achieve a compensated binary control signal adapted for providing a desired light intensity of the LED driver 100, as will be further explained below.

[0303] In a subsequent step 1109, the method ends.

[0304] The other load 20 can correspond, with respect to electrical properties such as impedance, to a particular LED load 10 to be subsequently used with the LED driver 100. Similarly, the LED load 10 used for the configuration needs not be the same LED load 10 that is to be driven later by the LED driver 100 during operation, but it suffices that the load used for the configuration is similar to the LED load 10 to be used during lighting operation or that the configuration information can be translated or interpreted in an unambiguous manner knowing any differences regarding electrical properties between the load used for the configuration and the LED load 10 later driven by the LED driver 100.

[0305] Fig. 14 illustrates another method, for operating the LED driver 100.

[0306] In a first method step 1401, the method starts.

[0307] In a subsequent step 1402, the LED driver 100 is configured using a method of the type illustrated in Fig. 11 and as described above. As is recalled, at the end of such configuration there is stored configuration information that can be used to produce a compensated binary control signal given a desired light intensity for the driven LED load 10.

[0308] In a subsequent step 1403, that can be performed at a later point, the LED driver 100 is then operated by determining a binary control signal corresponding to a particular desired current or light intensity, the determining of the binary control signal being performed using the stored configuration information. The binary control signal is then used to provide a variable current to the driver output 182 of the LED driver 100. More particularly, the variable current is provided based on the determined binary control signal in any of the ways generally described herein. It is preferred that the same LED driver 100 that was used in the calibration method is also used in the operating method. However, it is realized that the calibration can take several different aspects into consideration, as is described herein, and in particular the calibration information can comprise information that is not directly and specifically aimed to compensate for differing electric properties in component parts of the LED Driver 100. Therefore, it is also possible to perform, at least partly, the calibration method for a standard LED driver 100, and then use the resulting calibration information when operating a different LED driver 100 of the same standard type, such as several different same-type LED drivers 100.

[0309] For instance, and as has been described above in relation to the first aspect, the determining of the binary control signal can comprise adjusting (compensating) one or several pulse widths within the repeated binary signal pattern and/or adjusting a number of pulses within the repeated binary signal pattern; and the pulses within the repeated binary signal pattern can be adjusted so as to be distributed over a predetermined set of available pulse positions across the repeated binary signal pattern, such as a more or less evenly distributed such predetermined set of available pulse positions. The pulse compensator 137 can be arranged to perform the adjustment/compensation based on the previously determined and stored configuration information, such as a parametric model of one of the various types described herein.

[0310] As discussed above in connection to the first aspect, in embodiments of the invention the binary control signal frequency can be constant in the sense that the repeated control signal pattern has a constant set period length. In one of the examples provided, the frequency $f = 250 \text{ Hz}$. At low dimming levels the repeated control signal pattern may only contain one single pulse, meaning that the binary control signal is a 250 Hz PWM signal. Scaling the desired current or light intensity with the period time $T = 1/f$, the determined parametric model can be used to calculate a compensated pulse width $W_{\text{Compensated}}$ provided a desired pulse width W . As there is only a single pulse in the control signal pattern, this can also be expressed unambiguously using a compensated duty cycle $D_{\text{Compensated}}$, using the desired light intensity I :

$$W_{\text{Compensated}} = D_{\text{Compensated}} \cdot T = \frac{D_{\text{Compensated}}}{f}$$

$$W = I \cdot T = \frac{I}{f} \Rightarrow I = W \cdot f$$

$$\Rightarrow W_{\text{Compensated}} = \frac{D_{\text{Compensated}}}{f} = \frac{M(I)}{f} = \frac{M(Wf)}{f}$$

$$\Rightarrow W_{\text{Compensated}} = \frac{M(Wf)}{f}.$$

[0311] Given this relation, M can now be applied to each PWM-like pulse, even as the frequency changes as new pulses are added to the repeated control signal pattern. However, there is a problem with this if the drive circuitry 140 is dependent on the instantaneous time-averaged value:

If it is assumed that there is only one pulse during a 250 Hz cycle, M is applied only once and since the signal is the same as when the calibration was performed a perfect inverse model is achieved. If it is instead assumed that the average light intensity or current is the same but the pulse was divided into two separate and evenly distributed pulses over the 250 Hz cycle, effectively forming a 500 Hz PWM signal, M will need to be applied twice. This causes the signal going into the drive circuitry 140 to be slightly different, in turn causing the external variables to deviate from the values used when doing the calibration (the instantaneous time-averaged value is different). If more pulses were to be added to the repeated control signal pattern, even under constant total duty cycle of the control signal pattern, the deviation would grow. In case the maximum number of pulses in a 250 Hz cycle is 128, a maximum frequency of 32 kHz is reached.

[0312] To solve this problem, two parametric models can be constructed: one $M_{250\text{Hz}}(I)$ which is optimized for a 250 Hz binary control signal and another one $M_{32\text{kHz}}(I)$ which is optimized for a 32 kHz binary control signal. For intermediate frequencies, $W_{\text{Compensated}}$ can then be calculated using interpolation between these two extreme-point models. Then, let x be a value between 0 and 1, such that x assumes the value 0 up to a point where the first pulse has reached the threshold pulse width (as described in the example in connection to the first aspect). As the second pulse is added and starts growing, $x > 0$, and thereafter grows linearly up to a point where the maximum number of pulses is reached, at which point $x = 1$. Then, $W_{\text{Compensated}}$ can be determined according to the following empirically developed equation providing a good fit under the frequency change that occurs in this and in similar examples:

$$W_{\text{Compensated}} = (1.0 - \sqrt{x}) \cdot W_{250\text{Hz},\text{Compensated}} + \sqrt{x} \cdot W_{32\text{kHz},\text{Compensated}}.$$

[0313] Finally, given $W_{\text{Compensated}}$ a model has been formulated that takes into consideration component variations, electric properties of the drive circuitry 140 and the drive switch 180, and in particular behavior due to used transistors and signal frequency variations.

[0314] Generally, in some embodiments the determining of the binary control signal in step 1403 can comprise determining a number of pulses within the control signal pattern. Then, the selection of the binary control signal to fit the desired average current or light intensity can be made according to an interpolation between a first and a second respective expression for the binary

control signal. The first expression can be determined based on the configuration parameters for a first number of pulses within the control signal pattern and the second expression can be determined based on the configuration parameters for a second number of pulses within the control signal pattern. The interpolation can be performed for a current number of pulses within the control signal pattern between the first number of pulses and the second number of pulses. When dimming between a first dimming value and a second, different, dimming value, several different interpolations can hence be used. For instance, the interpolation can be continuous from the first to the second dimming value.

[0315] Further generally, the first and second expressions can be determined based on a respective pulse width within the control signal pattern.

[0316] Further generally, the interpolation can be performed using as a weight factor, for the first and second expressions, a square root of a normalized value for the current number of pulses.

[0317] Another example takes into consideration the fact that the drive circuitry 140 itself can be dependent on the average value of the binary control signal s . This fact will be discussed in detail below in connection to the third aspect. More particularly, the average value of s can in some embodiments alter the rise and fall times for H . To take this into considerations, two models at the two extremes were used, one when the rise and fall times were at the slowest rates of change, and one when they were at the highest rates of change. This gave two models, M_0 and M_1 respectively, which would then be fused together using a weight function $w(e)$.

$$M(y, e, v) = (1 - w(e)) \cdot M_0(y, e_0, v_0) + w(e) \cdot M_1(y, e_1, v_1),$$

where $w(e) = \text{sqr}t(s_{avg})$. All external sets e , e_0 and e_1 contains the variable s_{avg} and e_0 and e_1 represent the conditions that were used when creating M_0 and M_1 respectively. In general, the methodology described above can be used for any other variable that may affect the drive circuitry 140 or the characteristics for the power transistor 181. For example, the external sets could contain information about the temperature of the system or the load size of the led load 10. Assuming that a dependency on temperature is to be modelled, by way of example, then two models $M_3(y, e_3, v_3)$ and $M_4(y, e_4, v_4)$ could be constructed, where e_3 and e_4 correspond to the different temperatures that were used during the calibration. When applying these models, the

current temperature is then measured (and is contained in the variable e in question) and a similar interpolation can then be done using another weight function $w(e)$.

Further generally, the model can be written as a weighted sum of submodels $M(y, e) = \sum_i w_i(e) \cdot M_i(y, e)$, where $w_i(e)$ is a weight function dependent on external variables.

[0318] In a subsequent step 1404, the method ends.

[0319] It is realized that the binary control signal selected, using the configuration information and to match a desired light intensity or current as described above, can be considered to constitute a “compensated” binary control signal in the sense that the binary control signal that is actually used (such as fed to the drive circuitry 140) is not a naïve binary control signal devised with a particular control signal pattern duty cycle corresponding to the desired light intensity or current, but being compensated in relation to such naïve binary control signal to take the specific electric properties of the drive circuitry 140, the drive switch 180, and so forth into consideration to actually produce the desired waveform corresponding to the naïve binary control signal at the output 182 of the LED driver 100 and into the LED load 10.

[0320] It is realized that the various ways and approaches to determine the configuration information presented and exemplified herein can be combined in various ways, depending on the concrete needs of the embodiment at hand.

[0321] In particular, given measured current or light intensity, as well as set duty cycle (the binary control signal), there are many ways to identify and determine parameterized models to achieve a desired precision of the inverse model $D(I)$. The inverse model $D(I)$ will generally to a high degree depend on how the drive circuitry 140 and drive switch 180 is implemented. For instance, the parameterized model will likely differ depending on if the drive circuitry 140 uses a variable resistance driven by a BJT transistor or a DAC (Digital Analog Converter) (see below in relation to the third aspect). One example of another parameterized model that has been used by the present inventors is one where $D(I)$ is calculated as

$$D = \exp\left(x - ((k_1 \cdot x + m_1) \cdot (\operatorname{atanf}(k_2 \cdot x + m_2) + m_3) + m_4)\right),$$

where $x = \log(I)$ and the other parameters are constants in the model being adapted after the measurement data, the parameters being determined using some suitable and per se conventional optimization method.

Third aspect of the invention

[0322] Turning now specifically to the third aspect, the LED driver 100 comprises the drive circuitry 140 and the drive switch 180 as already described above. The drive switch 180 is arranged to provide the variable current or voltage to the LED load 10 as a switched electric signal. The microcontroller 130 is arranged to provide a control signal, such as a compensated binary control signal as described in connection to the second aspect, to the drive circuitry 140 to in turn, such as via the drive switch 180, provide the variable current or voltage to the LED load 10.

[0323] In fact, the third aspect presupposes a binary control signal source, arranged to provide the binary control signal as a square wave, the binary control signal having a control signal pattern that is repeated over time to form the binary control signal as described above. As also described, the control signal pattern at each time has an instantaneous time-averaged value being or corresponding to a time-average of the signal over the control signal pattern used at the time in question. The binary control signal source can be the microcontroller 130 itself, but it is realized that the third aspect of the invention in principle works also with a different internal or external binary control signal source, such as a separate piece of hardware arranged to provide the binary control signal to the drive circuitry 140.

[0324] The LED driver 100, and in particular the one or several drive switches 180, also comprises one or several electric driver outputs 182 as described above, each arranged to provide the drive current to the LED load 10 based on the binary control signal to drive one or several LEDs of the LED load 10.

[0325] As is illustrated in Fig. 15, showing an exemplary LED driver 100 connected to an LED load 10 for driving the LED load 10, the LED driver 100 comprises a power transistor 181. In the example shown in Fig. 15, the power transistor 181 in fact constitutes the switch 180. The power transistor

181 is arranged to power the LED load 10 via the driver output 182, and has a power transistor control terminal 181a as well as a pair of different terminals 181b, 181c. The control terminal 181a is arranged to accept, from the drive circuitry 140, a voltage or current signal arranged to modulate the power transistor 181. One of the other terminals 181b, 181c (in the example shown in Fig. 15 the terminal 181c) is connected to the driver output 182. The power transistor 181 can be a FET (Field-Effect Transistor), such as a MOSFET.

[0326] The drive circuitry 140 is connected to the power transistor control terminal 181a.

[0327] The exemplary LED driver in Fig. 15 is a single-channel LED driver 100. It is realized that, in the case of a multi-channel LED driver, the switch 180 and other relevant components would be duplicated and provided one for each channel.

[0328] In Fig. 15, the positive pole of the LED load 10 is connected to the feed voltage, and the negative pole is connected to the drain terminal of an N-channel MOSFET transistor (the power transistor 181). The source terminal of the transistor 181 is connected to ground, and its gate is connected to the drive circuitry 140. To handle parasitic inductance from long cables to the LED load 10, causing slow current decays, a Schottky diode 190 is provided, arranged to provide the current with a way back. It is realized that any such Schottky diode 190 can also form part of the LED driver 100. It is realized that other types of diodes can be used as alternatives to the Schottky diode 190, such as a standard silicon diode.

[0329] It is realized that the switch 180 can generally be provided in other ways. For instance, a GaN transistor could be used instead of the MOSFET. P-channel MOSFETs could be used, and the connection point of the transistor could be to VDC.

[0330] As described above, the binary control signal can be generated directly by a binary control signal generator 136 of the microcontroller 130, or be provided from an external source.

[0331] From a general point of view, a MOSFET transistor is excellent for uses where it is either completely on or completely off. However, power losses arise at the transition during which the transistor is switched on or off. Therefore, shortening such transition times decreases such losses.

This can be achieved by designing the drive circuitry 140 to be fast, but as discussed above this leads to other problems in terms of uneven light at low dimming levels.

[0332] One common way to limit the speed of a drive circuit is to connect a resistance in series with gate drive logic circuitry. However, such approach would limit the maximum PWM-like frequency of the LED driver 100, since the power losses are directly proportional to the operating frequency.

[0333] However, the present inventors have realized that the binary control signal can be designed so that the PWM-like frequency is low at low dimming levels and high at high dimming levels. In fact, this is the case using many reasonable dimming approaches when operating according to the principles described herein, such as the one using PWM-like pulses described above in connection to the first aspect. Furthermore, the driver circuitry 140 can be designed to be slow at relatively low dimming levels and fast at relatively high dimming levels. This way, it is possible to achieve both even lighting at low dimming levels and high efficiency at high dimming levels, despite the PWM-like frequency then being higher. This will now be described and exemplified.

[0334] The drive circuitry 140 is arranged to construct the electric control signal needed to operate the switch 180, in turn powering the LED load 10. Given the binary control signal for driving the LED load 10 on and off, the LED driver 100 should generate a drive signal with the right voltage/current levels, and the drive circuitry 140 should achieve this end goal while providing a control signal with suitable rise and fall times for the concrete embodiment at hand. Specifically, when dealing with switches 180 based on n-channel FET transistors, a suitable positive voltage level should be produced on the power transistor's 181 gate terminal 181a, with respect to its source terminal 181b.

[0335] For FET-transistors in general, the main contributors to power losses are switching losses and conduction losses. In order to minimize losses without using an unnecessary costly transistor, both loss types are usually balanced such that they contribute to the losses in the same order of magnitude.

[0336] However, for a constant-voltage LED load 10, the current through the LED load 10 is strongly correlated with the control signal going into the switch 180, which means that additional

factors must be taken into account. Firstly, a pulse being generated will have some physical length inside the electrical traces across the LED load 10. As discussed above, for an LED strip of 5 m physical length and with the speed of light inside copper roughly being half of that in vacuum, it takes about $5/150e6 = 33 \text{ ns}$ for the signal to travel through the whole LED strip. After reaching the other end of the LED strip, the wave will be reflected and go in the other direction. If the length of the wave is in the same order of magnitude as the LED strip, visible interference patterns may emanate. This is usually not a problem for conventional LED drivers because at their lowest possible dimming level (such as 0.1%), the pulses are long enough to make the resulting interference pattern invisible. Putting this into mathematical rigor, if a PWM frequency of 230 Hz and dimming level is 0.1% is used, the pulses being generated are $0.001/230 = 4348 \text{ ns}$, equivalent to a pulse of length 652 m.

[0337] Keeping in mind that the pulses being generated are of rectangular shape, higher frequencies than the base frequency (e.g. 230 Hz) are contained in the signal (harmonics). To avoid any interference patterns, frequencies up to at least 10 times the base frequency should be considered. For conventional LED drivers, this is still not a problem because the equivalent pulse length is then 65.2 m, still a lot longer than a normal LED strip. However, for dimming down to lower levels, such as 0.01%, this equivalent length gets further reduced down to 6.52 m, which is of comparable length to conventional LED strips and this leads to the risk of interference patterns becoming visible.

[0338] Therefore, pulses of rectangular shape cannot be used for dimming to darkness with high light quality, even at low PWM frequencies, assuming the dimming level has to go below 0.1%.

[0339] An additional problem arises when high varying currents are flowing through a wire, in the form of crosstalk. If high-frequency content of the signal has a corresponding wavelength that is comparable to the length of the wire, the wire will start acting as an antenna, possibly transferring energy to nearby wires. For multi-channel LED strips, this can become a problem as it may produce light from channels that should be off, in turn potentially causing problems such as color errors.

[0340] Hence, the frequency contents of the drive signal to the LED load 10 should be relatively low at relatively low dimming levels, but can be relatively high at relatively higher dimming levels.

[0341] One way to reduce the frequency contents of the drive signal is to reduce the frequency contents of the control signal going to the switch 180. For MOSFETs, this can be done by slowing down the charging and discharging of the gate capacitance, such as by increasing the series resistance between the drive circuitry 140 and the transistor 181 gate 181a. This leads to longer rise- and fall-times.

[0342] However, by doing so the switching losses will increase, which constrains the viable PWM-like frequency of the binary control signal, in turn leading to possible flicker. Thus, in order to increase frequency when intensity is increased, while at the same time being both efficient and being able to dim all the way down to complete darkness, slow rise and fall times can be used for low light intensities while fast rise- and fall times can be used for higher light intensities.

[0343] As discussed herein, the LED driver 100 can be designed so that an average light intensity of the connected LED load 10 is positively correlated with the number of pulses generated per time unit. Therefore, the average intensity can be used as a control signal to the drive circuitry.

[0344] A block diagram of an exemplifying drive circuitry 140 is shown in Fig. 16. The binary control signal is delivered by the (internal or external) binary control signal generator 136 to a signal averaging part 170, in turn providing a time-averaged signal value representing a positive and/or negative value of a general signal level currently used, which value can be correlated to the currently used repeated control signal pattern. In general, the drive circuitry 140 is arranged to receive or produce one or more level signals (such as said time-averaged signal values), each such level signal being provided as an increasing or decreasing function of an increase in the instantaneous time-averaged value.

[0345] The respective time-averaged signal values are then used to control a first and second variable, current-controlling resistances 161 (first and second current-throttling parts), each such current-controlling resistances 161 in turn being connected in series between, firstly, a respective first 151 or second 152 switch transistor (the switch transistors 151, 152 together forming a switch 150 of the drive circuitry 140) and, secondly, the switch 180 (the power transistor 181). More particularly, it is the control terminal 181a of the power transistor 181 that is connected in series in the way discussed here. The first switch transistor 151 is connected to a high voltage 154 (such as a drive power supply 123 of the power supply 120), and is arranged to provide a current via the first

variable resistance 161 to the switch 180 (the control terminal 181a) as a function of the provided binary control signal provided from the binary control signal generator 136. Correspondingly, the second switch transistor 152 is connected to a low voltage 153, in this example ground, and is arranged to provide a current via the second variable resistance 161 from the switch 180 (the control terminal 181a) as a function of the provided binary control signal provided from the binary control signal generator 136. The exemplary circuit shown in Fig. 16, being a push-pull circuit, employs two such current-throttling parts 161, one arranged to throttle the current to the gate terminal 181a and the other arranged to throttle the current from the gate terminal 181a. In other configurations, only one current-throttling part 161 could be used.

[0346] Generally, the drive circuitry 140 can comprise the drive circuitry switch 150, which is arranged to selectively provide an electric coupling between the control terminal 181a of the power transistor 181 to either the low voltage 153 or to the high voltage 154, in dependence of an instantaneous low value or high value of the binary control signal. It is realized that such coupling can be mediated by the variable resistances 161 but possibly also additional electric components. The coupling can also be a direct connection, through and via the variable resistances 161.

[0347] Further generally, the drive circuitry 140 can comprise one or several such variable resistances 161, arranged to provide a respective variable resistance along said electric coupling, the variable resistance of each of the variable resistances 161 being arranged to vary as a function (such as an increasing or decreasing function, depending on how the level signal is defined and produced) of the level signal, resulting in that an increase in the instantaneous time-averaged value results in an increase in an instantaneous current flowing to or from the control terminal 181a of the power transistor 181. For the upper part of the circuit in Fig. 16, the inverted binary control signal relative to the high voltage V_{drive} is averaged and used as the level signal, so that a larger negative value signal translates into a larger current flowing to the control terminal 181a. For the lower part, the non-inverted binary control signal relative to the low voltage GND is averaged and used as the level signal, so that a larger positive signal translates into a larger current flowing from the control terminal 181a.

[0348] To explain this setup more closely, first a conventional push-pull drive circuit can be considered, shown in Fig. 17. The push-pull drive circuit of Fig. 17 is based on a couple of MOSFET

transistors, one n-channel and one p-channel. This circuit uses individual resistors to tune the rise and fall times individually.

[0349] In the schematic shown in Fig. 17, $\sim$ PWM is the inverted input control signal. When the binary control signal (in these examples denoted "PWM") is low, $\sim$ PWM is high and will turn on Q6A and turn off Q6B. This will discharge the gate of the power transistor, connected to GATE_DRIVE, through R34. When PWM is high, $\sim$ PWM is low and will turn off Q6A and turn on Q6B. This will charge the gate of the power transistor through the other resistor, R33.

[0350] Now consider the more complex circuit shown in Fig. 18, in which resistors 163, 165 are introduced and wherein the combination of a first current-controlling transistor 162 and the resistor 163 together constitute a first current-throttling mechanism 161 and a second current-controlling transistor 164 together with the resistor 165 constitute a second current-throttling mechanism 161. Both current-throttling mechanisms 161 depend on the average value of the binary control signal PWM in a way corresponding to what has been discussed above.

[0351] In Fig. 18, a first current-controlling PNP transistor 162 Q2B and a second current-controlling NPN transistor Q2A 164 are connected in series with the push-pull circuit shown in Fig. 17. In the example shown, the current-controlling transistors 162, 164 are BJT transistors, comprising a respective base terminal 162a, 164a; a respective emitter terminal 162b, 164b; and a respective collector terminal 162c, 164c. In other embodiments, the current-controlling transistors 162, 164 can be MOSFET transistors with corresponding gate, source and drain terminals.

[0352] In general, the variable resistance part 160 can comprise one or several current-throttling parts 161, in this case the current-controlling transistors 162, 164, in combination with the resistors 163, 165, arranged to throttle the current that can pass through said electric coupling and therefore limiting a rise-time and/or fall-time of an electric signal provided to the power transistors 181 control terminal 181a, in turn controlling the rise-time and/or fall-time of the current through the drive output 182 as the switch 150 switches the electric coupling between the low voltage 153 and the high voltage 154. As mentioned, the variable resistance part 160 can be arranged to vary the resistance as a function, such as a decreasing function, of the level signal. This function can be a monotonous function.

[0353] Further generally, the variable resistance part 160 can comprise one or several current-controlling transistors (in this case again 162 and 164), configured so that a current flowing through said electric coupling flows across the current-controlling transistor 162, 164 in question, via the current-controlling source/emitter terminal 162b, 164b and the current-controlling drain/collector terminal 162c, 164c. The level signal can be coupled to the current-controlling gate/base terminal 162a, 164a so that an increase in the instantaneous time-averaged value results in a higher instantaneous current across the current-controlling source/emitter terminal 162b, 164b and the current-controlling drain/collector terminal 162c, 164c. This way, a faster drive circuitry 140 is achieved both for the rise and fall flanks of the current waveshape output to the LED load 10, for higher dimming values, and vice versa.

[0354] Each of the current-controlling transistors 162, 164 can then be series-connected to a respective resistor 163, 165 along said electric coupling in order to limit the currents to desired values.

[0355] Moreover, the switch 150 can comprise one or several switch transistors 151, 152, each having a respective gate/base terminal 151a, 152a, a respective source/emitter terminal 151b, 152b and a respective drain/collector terminal 151c. Generally, the gate/base terminal 151a, 152a of each such switch transistor 151, 152 can be connected to the positive or negative binary control signal, in the form of a voltage or current varying according to the value of the binary control signal. In the case illustrated in Fig. 18, the two switch transistors 151, 152 together form and provide a push/pull circuit, the two switch transistors 151, 152 being arranged between two different voltage potentials in the form of the low voltage 153 and the high voltage 154. Also, the power transistor 181 control terminal 181a is coupled to a point between the two switch transistors 151, 152. For the case using BJT transistors, they can be connected either as so-called "common emitter" (emitter terminals being interconnected) or "common collector" (collector terminals being interconnected). For the case using MOSFET transistors, the drain terminals can be interconnected.

[0356] In Fig. 18, the switch transistors 151, 152 are each a FET. However, by modifying the circuitry layout BJT transistors can be used instead as the switch transistors 151, 152.

[0357] As is also specifically exemplified in Fig. 18, the variable resistance part 160 can comprise both the first current-controlling transistor 162, which is connected so that a current flowing through the electric coupling between the first switch transistor 151 and the power transistor 181 control terminal 181a passes through the first current-controlling transistor 162, and also the second current-controlling transistor 164, which is connected so that a current flowing through the electric coupling between the second switch transistor 152 and the power transistor control terminal 181a passes through the second current-controlling transistor 164. In other words, the electric coupling discussed herein can consist of two separate connection lines, both terminating to source or sink current to the control terminal 181a but each being operable only during either the rise or the fall of a pulse.

[0358] Regarding the signal averaging part 170, it can be arranged to provide the level signal to be, or to correspond to, the instantaneous time-averaged value or to the inverse of the instantaneous time-averaged value as discussed above. Specifically, the signal averaging part 170 can comprise a low-pass filter or a digital to analog converting circuitry, arranged to provide the level signal as a smoothed or time-averaged, positive or negative, version of the binary control signal. The level signal itself can be a current or a voltage corresponding to the instantaneous time-averaged value in any of said manners.

[0359] One goal of the drive circuitry 140 is to minimize switching losses in a power transistor 181 that is driven with a control signal designed such that low PWM-like frequencies are used for low light intensities and higher PWM-like frequencies are used for higher light intensities, and to provide switching characteristics that are slow for low light intensities. Put differently, the rise and/or fall-times at low light intensities should or could be so long so that if the intensity and the PWM-like frequency were to be increased, an unpractical amount of heat risks being generated. In cases wherein the time-averaged value of the binary control signal is positively correlated to the number of pulses per second (the PWM-like frequency), the time-averaged value of the binary control signal can be used as a level signal for controlling a variable resistance. On the other hand, this also means that the inverse of the time-averaged binary control signal is anticorrelated with the number of pulses per second and can also be used for controlling a variable resistance. Hence, the level signal can either be, or be correlated with, the time-averaged binary control pattern or be, or be correlated with, the negative time-averaged binary control pattern. Either way, the goal

is still to lower the variable resistance when the light intensity increases and the variable resistance will be configured to change with the level signal to achieve this goal.

[0360] In examples provided herein, the average value of the binary control signal is useful for controlling an NPN BJT transistor, while the average value of the inverse binary control signal is useful for controlling a PNP BJT transistor. Likewise, if the current-limiting transistor would be a MOSFET, the non-inverted signal would typically be useful for an N-channel MOSFET while the inverted signal would be useful for a P-channel MOSFET.

[0361] Hence, to assume that the PWM-like frequency increases when the time-averaged value of the binary control signal increases is equivalent to assumed that the PWM-like frequency increases when the light intensity emitted from the LED load 10 increases. A level signal can now be constructed that is either increasing or decreasing with light intensity, depending on if it was based on the non-inverted or the inverted binary control signal, respectively. The level signal is then used to control a variable resistance such that when light intensity is increased, the variable resistance is decreased.

[0362] As noted above, the level signal can be provided as a function of the instantaneous time-averaged value. It is, of course, noted that the level signal in some embodiments is not calculated directly as a function of the instantaneous time-averaged value, but can instead be calculated so as to correlate with the instantaneous time-averaged value in some other way. For instance, the level signal can be calculated based on the control input 110 and to (in a way corresponding to what has been said above) be calculated or determined as an increasing or decreasing function of an increase in such a control signal that in turn is correlated with the instantaneous time-averaged value.

[0363] Returning to the added components of the circuit shown in Fig. 18, one can first observe the differences between Fig. 17 and Fig. 18, and note that the resistors R11 and R12 together with the transistors Q2A and Q2B, are not mounted in Fig. 17, but that resistors R33 and R34 are. In this case, a traditional push-pull drive circuit is achieved, based on the two MOSFET transistors Q6A and Q6B. The inverted signal $\sim$ PWM is used to control the gates of Q6A and Q6B, and the high voltage value for $\sim$ PWM is the same as the voltage Vdrive. R33 controls how fast the gate connected to GATE_DRIVE is charged, and R34 controls how fast it is discharged. This provides the

same rise time and fall time for the current to the LED load 10, irrespective of the duty cycle (defined as above) of the repeated control signal pattern PWM.

[0364] Now, the situation can be investigated when R11, R12, Q2A and Q2B are used instead of R33 and R34, as is the case in Fig. 18. The bias current to the BJT transistors Q2A and Q2B will now decide the effective resistance to GATE_DRIVE. Looking at the lower part of the circuit, the PWM signal first passes through a low-pass filter R_{15} and C_2 . These components are used to create a constant voltage level that is proportional to the duty cycle of the PWM signal. The low-pass filtered signal is now combined with a resistor divider R_{13} and R_{17} , so that a suitable selected mapping between duty cycle and bias voltage can be created, $(0\%, 100\%) \rightarrow (V_{min}, V_{max})$. R_{16} is then used to create a bias current to the BJT transistor Q2A, which is amplified by the amplification factor h_{FE} of the transistor Q2A. The current passing through R_{12} is therefore determined by the duty cycle as long as the transistor is operating in its active region. Once it has been saturated, the current is instead limited by R_{12} .

[0365] For analysis of the bias network, the circuits in Fig. 19 can be observed. As the PWM signal is fed into R_c , the signal V_{out} results, that will vary in a linear manner between V_{min} and V_{max} . When the duty cycle is 0%, $V_{out} = V_{min}$ and when the duty cycle is 100%, $V_{out} = V_{max}$. Therefore, the circuit can be redrawn as shown in Fig. 19, so that an analytical expression for V_{min} and V_{max} can be derived.

[0366] By using the principles for resistance laws (Ohm's law and Kirchhoff's current law), R_a and R_b can be calculated given R_c :

$$R_a = R_c \frac{(V_{max} - V_{min})V_d}{V_{min}V_c} \quad R_b = \frac{V_{min}R_aR_c}{V_dR_c - V_{min}(R_a + R_c)}.$$

[0367] Since C and R_c are used together as a low-pass RC filter, values are assigned to them so that they together achieve a desired suppression of the varying signal so that a DC voltage is created. The cut-off frequency f_c for this filter, i.e. the frequency when the filter starts dampening the signal, thereby becomes a design parameter and defines C and R_c by

$$f_c = \frac{1}{2\pi R_c C}.$$

[0368] What is now left is to determine the resistance R_{16} given the voltage V_{out} . When Q1A is closed, the circuit is simplified according to Fig. 20. Since the base-emitter voltage V_{be} in an NPN transistor can be modelled as a forward diode, Shockley's diode equation can be used here also, and the current I_b as a function of the voltage V_{out} will follow a curve similar to the above-described for an LED in series with a resistor. Hence, Shockley's diode equation yields:

$$V_{be} = nV_T \cdot \ln(I_b/I_S) \text{ and } I_b = I_S \cdot \exp\left(\frac{V_{be}}{nV_T}\right),$$

where V_T is the thermal voltage, n is the ideality factor and I_S is the scale factor current.

[0369] Now, V_{out} can be described as a function of V_{be} :

$$V_{out} = V_{be} + I_b \cdot R_{16} = V_{be} + R_{16}I_S \cdot \exp\left(\frac{V_{be}}{nV_T}\right).$$

[0370] Example values for n and I_S for a silicon-based diode is $n = 1.7$ and $I_S = 2.5 \text{ nA}$, and are used in the graphs shown in Figure 21 and 22.

[0371] For a given voltage V_{out} , an expression is now desired for the effective resistance $R_e(V_{out})$ so that a resistance ratio $K = R_e(V_{min})/R_e(V_{max})$ can be calculated. As the switching losses in the power transistor 181 is more or less proportional to the rise and fall-times of the electric signal delivered to the power transistor's 181 control terminal 181a, a twice as fast rise and fall-time will result in half as large power losses. Thus, if $K = 2$, only half as large power losses will be generated for binary control signals with high enough average values, as compared to a circuit with the same value for $R_e(V_{min})$ but with a resistance ratio of $K = 1$ (corresponding to the case when a constant, non-variable resistance is used). Thus, the resistance ratio K measures the potential efficiency gain compared with a conventional circuit.

[0372] A simplified analysis is first motivated by plotting V_{be} as a function of V_{out} given the values above and $R_{16} = 10 \text{ k}\Omega$ (Fig. 21). In this graph, it can be seen that the voltage V_{be} is rather stable in the linear region, whereas it is temperature dependent. V_{be} also depends on the choice of R_{16} (Fig. 22), but is also here rather stable for various resistance values. Therefore, one can try to regard V_{be} as constant, and further assume the voltage GATE_DRIVE to be equal to V_{drive} in Fig. 18, so that the effective resistance is calculated at the time point when the gate of the MOSFET is just beginning to be charged. Then, the equivalent resistance of R_{12} in series with the transistor

can be defined as R_Q . Ohm's law, together with the amplification factor h_{FE} for the transistor, can be used to calculate R_Q when the transistor is operating in its active region:

$$R_Q = \frac{V_{drive}}{I_{CE}} = \frac{V_{drive}}{h_{FE}I_b} = \frac{V_{drive}}{h_{FE}} \cdot \frac{R_{16}}{V_{out} - V_{be}}.$$

[0373] Now, $R_e(V_{out})$ can be determined as a parallel connection of $R_Q(V_{out})$ and R_{14} . Let $R_{Q1} = R_Q(V_{min})$ and $R_{Q2} = R_Q(V_{max})$. Then:

$$\begin{aligned} K &= \frac{R_e(V_{min})}{R_e(V_{max})} = \frac{R_{Q1} || R_{14}}{R_{Q2} || R_{14}} = \\ &= \frac{\frac{R_{Q1}R_{14}}{R_{Q1} + R_{14}}}{\frac{R_{Q2}R_{14}}{R_{Q2} + R_{14}}} = \frac{R_{Q1}(R_{Q2} + R_{14})}{R_{Q2}(R_{Q1} + R_{14})} = \\ &= \frac{\frac{V_{drive}}{h_{FE}} \cdot \frac{R_{16}}{V_{min} - V_{be}}}{\frac{V_{drive}}{h_{FE}} \cdot \frac{R_{16}}{V_{max} - V_{be}}} \cdot \frac{R_{Q2} + R_{14}}{R_{Q1} + R_{14}} \\ &\Rightarrow \\ K &= \frac{V_{max} - V_{be}}{V_{min} - V_{be}} \cdot \frac{R_{Q2} + R_{14}}{R_{Q1} + R_{14}} = \frac{V_{max} - V_{be}}{V_{min} - V_{be}} \cdot \frac{R_{Q1} + R_{14} - R_{Q1} + R_{Q2}}{R_{Q1} + R_{14}}; \text{ and} \\ K &= \frac{V_{max} - V_{be}}{V_{min} - V_{be}} \cdot \frac{R_{Q1} + R_{14} - R_{Q1} + R_{Q2}}{R_{Q1} + R_{14}} = \frac{V_{max} - V_{be}}{V_{min} - V_{be}} \cdot \left(1 - \frac{R_{Q1} - R_{Q2}}{R_{Q1} + R_{14}}\right). \end{aligned}$$

[0374] Since a higher voltage V_{out} yields a lower resistance value $R_Q(V_{out})$, one obtains $R_{Q1} - R_{Q2} = R_Q(V_{min}) - R_Q(V_{max}) > 0$.

[0375] So, in order to maximize the resistance ratio K , the second term in the second factor needs to be minimized, which is achieved by allowing R_{14} to approach infinity so that the term goes to zero. In other words, R_{14} is not needed when optimizing for high values of K , and the expression is then simplified to

$$K = \frac{V_{max} - V_{be}}{V_{min} - V_{be}}.$$

[0376] The closer V_{min} is to V_{be} , the larger K can be, but on the other hand it then also becomes more temperature sensitive since V_{be} depends on the temperature. Therefore, V_{min} needs to be set as low as possible, but not lower. This can be determined experimentally by applying temperature variations to the circuit for different values of V_{min} . The lower the value for V_{min} is

allowed to be, the larger K can be, and the larger the value for K , the lower the power losses for high dimming values result. From experiments conducted by the present inventors, a K value of about 10 has been achieved. If the MOSFET gate is modeled as a capacitor C to be charged using a resistance R at voltage V , the voltage V_C across the gate becomes

$$V_C = V \cdot (1 - \exp(-\frac{t}{RC})).$$

[0377] RC is the time constant for the circuit, which gives an indication of how quickly the capacitor is charged. A K value of 10 therefore means that the time constant is 10 times lower at high dimming values, and since the power losses arise during the transitions when the transistor is opened and closed, these power losses can be decreased considerably.

[0378] Regarding the upper part of the circuit in Fig. 18 for the gate drive logic, it is a direct mirror of the lower part, and the same reasoning can be used to derive identical findings.

[0379] Another possible solution that has similar characteristics as the example provided in Fig. 18 is to separate the gate driver circuit from the variable resistance. By doing so, a conventional gate driver IC can be used in concatenation with a variable resistance, as is illustrated in Fig. 23 (block diagram) and Fig. 24 (detailed circuit example).

[0380] In Fig. 24, the left part of the circuit represents a generic gate driver, being arranged to deliver the voltage V_{drive} when the binary control signal PWM is high and 0 V when PWM is low. As compared to the circuit shown in Fig. 18, the circuit in Fig. 24 is different, but performs what is basically the same thing, as will now be explained.

[0381] V_{out} is the voltage out from the generic gate driver. In the example shown in Fig. 24, the generic gate driver comprises a push-pull transistor pair 151, 153 (note the correspondence to 151, 153 in Fig. 18), but in other embodiments it could be replaced with a circuit based on, for instance, a BJT transistor pair in common collector or common emitter configuration; an optocoupler; or a gate driver integrated circuit.

[0382] By looking at the directions of the BJT transistor arrows, the path of the current through transistors Q8A and/or Q8B can be seen. When V_{out} is high, the current takes the path through Q8B and when V_{out} is low, the current takes the path through Q8A.

[0383] VHighBias is the potential at the point between resistors R10 and R32, and VLowBias is the potential at the point between R37 and R40. Compare with Fig. 18, where corresponding VHighBias and VLowBias potentials are also marked.

[0384] When Vout is high, the current through the base terminal of Q8B is determined by the difference between Vout (that can be, for example, 5V) and VHighBias. The higher this difference is, the higher the current that also goes to GATE_DRIVE. A higher difference is achieved by allowing VHighBias to be lower. As can be seen from Fig. 24, VHighBias is connected via a low-pass filter to ~PWM, so the higher average value of the binary control signal PWM, the lower VHighBias will be, and the more current will go to GATE_DRIVE.

[0385] When Vout is low, the current through the base of Q8A is determined by the difference between Vout (that can be, for instance, 0V) and VLowBias. The larger this difference is, the higher the current that goes from GATE_DRIVE. A higher difference is achieved by allowing VLowBias to be higher. As is seen, VLowBias is connected via a low-pass filter to the binary control signal PWM, so the higher the average value of the PWM signal is, the higher VLowBias will be, and the higher the current from GATE_DRIVE will be.

[0386] As can be seen when comparing the circuits in Fig. 18 and Fig. 24, the various parts 150, 160, 170 and so forth are arranged differently but with the corresponding function.

[0387] As seen in the above examples, the drive circuit 140 can comprise a push-pull drive circuit based on MOSFETs. However, as is seen in the example of Fig. 25, a corresponding push-pull circuit can instead be designed based on BJTs. In Fig. 25, V3 and V4 are the bias voltages that are generated by low-pass filtering the binary control signal PWM. When V3 = 0V and V4 = 5V, the fastest possible control is achieved, as is shown in Fig. 26a. When V3 = 5V and V4 = 0V, the slowest possible control is achieved, as is shown in Fig. 26b.

[0388] If V3 and V4 are generated by low-pass filtering the inverted binary control signal PWM and the non-inverted binary control signal PWM, respectively, the speed of the switching can be achieved as a function of the duty cycle (as defined above). Hence, the corresponding functionality as in Figs. 18 and 23 is achieved.

[0389] Other possible ways to generate V3 and V4 include that the microcontroller 130 comprises a DAC (Digital to Analog Converter), the outputs of which are used to achieve an even better control over the control signal. A dedicated 2-channel DAC could also be used for each output channel.

[0390] Fig. 27 illustrates a method for driving the LED load 10 using the LED driver 100.

[0391] In a first step 2701, the method starts.

[0392] In a subsequent step 2702, the driver output 182' of the LED driver 100 is connected to the LED load 10.

[0393] In a subsequent step 2703, electric power is provided to the LED driver 100, such as via the DC bus 121, and the binary control source 136 is caused to provide the binary control signal, in turn causing the power transistor 181 to provide the drive current to the driver output 182' as described above, resulting in a variable current being provided to the LED load 10 as generally described herein.

[0394] In a subsequent step 2704, the binary control signal can be adjusted, such as to reflect a differently set dimming value, thereby modifying the instantaneous time-averaged value. This step can entail mapping the adjusting of the dimming state to a corresponding adjustment of the binary control signal.

[0395] In a subsequent step 2705, step 2703 can be repeated but using the updated binary control signal.

[0396] In a subsequent step 2706, the method ends.

[0397] Above, preferred embodiments have been described. However, it is apparent to the skilled person that many modifications can be made to the disclosed embodiments without departing from the basic idea of the invention.

[0398] For instance, the LED driver 100 can comprise various types of additional component parts, in addition to the ones described and exemplified herein. It is also realized that that the examples

provided herein are kept simple for reasons of clarity. In various embodiments of the invention, different voltages and currents can be used and applied to the LED load 10.

[0399] Generally, all that has been said in relation to the various principles and exemplifying methods and LED drivers 100 described herein can be combined freely, pending compatibility. Moreover, one or several aspects of two or all of the first, second and third aspects described herein can be combined freely in one and the same LED driver or method for operating such an LED driver.

[0400] Hence, the invention is not limited to the described embodiments, but can be varied within the scope of the enclosed claims.

CLAIMS

1. An LED, Light Emitting Diode, driver (100), comprising
 - a binary control signal source, arranged to provide a binary control signal as a square wave, the binary control signal having a control signal pattern that is repeated over time to form the binary control signal, the control signal pattern at each time having an instantaneous time-averaged value as time-averaged over the control signal pattern used at the time in question;
 - a first-channel electric driver output (182'), arranged to provide a drive current based on the binary control signal to drive an LED (10);
 - a power transistor (181), having a power transistor control terminal (181a) and a pair of different terminals (181b,181c), one of the pair of different terminals (181b,181c) being connected to the first-channel electric driver output (182'); and
 - a drive circuitry (140), connected to the power transistor control terminal (181a),
 - the drive circuitry (140) comprising a switch (150), arranged to provide an electric coupling between the power transistor control terminal (181a) to either a low voltage (153) or a high voltage (154) in dependence of an instantaneous low value or high value of the binary control signal,
 - the drive circuitry (140) being arranged to receive or produce a level signal, the level signal being provided as an increasing or decreasing function of an increase in the instantaneous time-averaged value or as an increasing or decreasing function of an increase in a control signal in turn being correlated with the instantaneous time-averaged value,
 - the drive circuitry (140) further comprising a variable resistance part (160), arranged to provide a variable resistance along the electric coupling, the variable resistance varying as a function of the level signal, resulting in that an increase in the instantaneous time-averaged value results in an increase in an instantaneous current flowing to or from the power transistor control terminal (181a).

2. The LED driver (100) according to claim 1, wherein
the drive circuitry (140) comprises a signal averaging part (170), arranged to provide the level signal to be, or to correspond to, the instantaneous time-averaged value or to the inverse of the instantaneous time-averaged value.
3. The LED driver (100) according to claim 2, wherein
the signal averaging part (170) comprises a low-pass filter or a digital to analog converting circuitry, arranged to provide the level signal as a smoothed and/or or time-averaged version of the binary control signal, or to provide the level signal as a smoothed and/or time-averaged signal calculated based on the binary control signal, wherein a value of the level signal at a particular time is determined to correspond to a general level of the binary control signal at the same particular time.
4. The LED driver (100) according to any preceding claim, wherein
the level signal is a current or voltage corresponding to the instantaneous time-averaged value.
5. The LED driver (100) according to any preceding claim, wherein
the power transistor (181) is a FET, Field-Effect Transistor.
6. The LED driver (100) according to any preceding claim, wherein
the switch (150) comprises a switch transistor (151), having a gate/base terminal (151a), a source/emitter terminal (151b) and a drain/collector terminal (151c), the gate/base terminal (151a) of the switch transistor (151) being connected to the binary control signal in the form of a voltage or current varying according to the value of the binary control signal.

7. The LED driver (100) according to claim 6, wherein
the switch (150) comprises two switch transistors (151,152), a gate/base terminal (151a,152a) of each being connected to the binary control signal in the form of a voltage or current varying according to the value of the binary control signal, the two switch transistors (151,152) together providing a push/pull circuit, wherein
the two switch transistors (151,152) are arranged between two different voltage potentials, and wherein
the power transistor control terminal (181a) is coupled to a point between the two switch transistors (151,152).
8. The LED driver (100) according to claim 6 or 7, wherein
the switch transistor (151) is a FET or a BJT, Bipolar Junction Transistor.
9. The LED driver (100) according to any preceding claim, wherein
the variable resistance part (160) comprises a current-throttling part (161), arranged to throttle the current that can pass through the electric coupling and therefore limiting a rise-time and/or fall-time of an electric signal provided to the power transistor control terminal (181a), in turn limiting a rise time and/or a fall time of a current through the drive output (182) as the switch (150) switches the electric coupling between the low voltage (153) and the high voltage (154).
10. The LED driver (100) according to claim 9, wherein
the variable resistance part (160) comprises a current-controlling transistor (162), in turn comprising a current-controlling gate/base terminal (162a), a current-controlling source/emitter terminal (162b) and a current-controlling drain/collector terminal (162c), wherein
a current flowing through the electric coupling flows across the current-controlling transistor (162), via the current-controlling source/emitter terminal (162b) and the current-controlling drain/collector terminal (162c), and wherein

the level signal is coupled to the current-controlling gate/base terminal (162a) so that an increase in the instantaneous time-averaged value results in a higher instantaneous current across the current-controlling source/emitter terminal (162b) and the current-controlling drain/collector terminal (162c).

11. The LED driver (100) according to claim 10, wherein
the current-controlling transistor (162) is a BJT.
12. The LED driver (100) according to claim 10 or 11, wherein
the current-controlling transistor (162) is series-connected to a first resistor (163) along the electric coupling.
13. The LED driver (100) according to claim 7 and claim 11, wherein
the variable resistance part (160) comprises a first current-controlling transistor (162),
connected so that a current flowing through the electric coupling between the first switch
transistor (151) and the power transistor control terminal (181a) passes through the first current-
controlling transistor (162), and wherein
the variable resistance part (160) comprises a second current-controlling transistor (164),
connected so that a current flowing through the electric coupling between the second switch
transistor (152) and the power transistor control terminal (181a) passes through the second
current-controlling transistor (164).
14. The LED driver (100) according to any preceding claim, wherein
the binary control signal source is arranged to produce the binary control signal in response
to an LED dimming value by varying both a pulse width and a number of pulses over the control
signal pattern, and wherein

the binary control signal source is arranged to produce the binary control signal in response to the LED dimming value by, when the LED dimming value increases, widening a pulse of the control signal pattern before increasing the number of pulses in the control signal pattern.

15. A method for driving an LED (10), comprising
providing, to a driver output (182') of an LED driver (100) according to any preceding claim being connected to the LED (10), electric power, in turn causing the binary control source to provide the binary control signal and the power transistor (181) to provide the drive current to the driver output (182').
16. A method according to claim 15, further comprising
adjusting the binary control signal, thereby modifying the instantaneous time-averaged value.
17. A method according to claim 16, further comprising
adjusting a dimming state of the LED driver (100); and
mapping the adjusting of the dimming state to a corresponding adjustment of the binary control signal.