

APPARATUS FOR CONDITIONING PRIORITY ARBITRATION IN
BUFFERED DIRECT MEMORY ADDRESSING

ABSTRACT

A data processing system includes an arrangement for modifying the usual priority arbitration of an input/output channel controller (IOCC) used in granting direct memory access (DMA) service among contending peripheral devices sharing a common peripheral bus. The IOCC includes logic for conditioning the established priority arbitration scheme based upon the data status of the data buffers. If the higher priority requesting device requires a data transfer between the system memory and the IOCC prior to performing an operation directly between the IOCC and the peripheral device, the priority will instead be granted to a lower priority peripheral device that does not require a system memory access operation.

This Sheet Has Been Replaced

