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An integrated circuit package

Field of the invention

The present invention relates to methods of packaging integrated circuits, and to the packaged integrated circuits.

5 Background of Invention

Packaging refers to the process of mounting integrated circuits (dies) body which are principally composed of a semiconductor within a protective body, with electric contacts of the integrated circuit connected to conductive
10 elements extending through the body, so that the conductive elements can electrically connect the integrated circuit to other electronic circuitry. Perhaps the commonest conventional packaging technique is wire bonding, in which wire bonds are formed between electrical contacts (pads) on the integrated circuit and fingers of a lead frame. A resin body is then moulded around the
15 integrated circuit and wire bonds, and the lead frame is cut to leave portions of the lead fingers projecting out of resin body, for easy connection to a PCB (printed circuit board) or other substrate.

Many variations of this technique are known, such as variations in which the
20 integrated circuit is mounted directly on the PCB, and the wire bonds are formed directly between the PCB and the integrated circuit. In other variations, multiple integrated circuits are stacked on one surface of the PCB. In yet further variations, integrated circuits are packaged on opposite surfaces of the PCB.

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Another common packaging technique employs "flip chips", that is integrated circuits which have electric contacts on one of their major faces, and are adapted to be placed with that major surface directed downwardly onto a surface of the substrate, with the electric contacts of the flip chips in register

with corresponding electric contacts of the substrate. Special measures are taken to ensure that all the respective pairs of contacts meet, despite any unevenness which may exist in the surface of the integrated circuit or substrate. The space between the flip-chip and the substrate is then filled with
5 an insulating "underfill" layer.

Summary of the Invention

In general terms, the present invention proposes that two integrated circuits having circuitry on respective ones of their major surfaces are ground on their
10 opposite major surface to reduce their thickness, and that the ground integrated circuits are placed back-to-back in a chamber formed within a substrate (such as a PCB). Electrical connections are formed between pads of the integrated circuits and contact points on the walls of the chamber. The contacts points of the substrate are electrically connected to wiring, e.g. for
15 connecting the integrated circuit to other components mounted on the substrate.

The invention makes it possible for integrated circuits to be packaged while occupying a very small amount (or even none) of the outer surface area of the substrate. Accordingly, the invention makes it possible for an increased
20 number of integrated circuits (or other components) to be connected to a substrate without increasing the surface of the substrate.

This may be achieved without increasing the thickness of the substrate, since the total ground thickness of the integrated circuits is preferably less than the thickness of the substrate.

25 Therefore, in contrast to conventional techniques (such as wire bonding and flip-chips) the present invention may lead to the following possible advantages:

1. The number of integrated circuits which can be provided for a given substrate surface area is increased.
2. The total thickness of the combination of the substrate and integrated circuit combination is reduced, in comparison to arrangements in which the integrated circuit rests on one exterior surface of the substrate.
3. Since no wire bonds are required, it is possible to connect the pads of the integrated circuits to other components by shorter electrical connection paths as compared to the wire bonding packaging technique. This leads to more robust signals, having less signal distortion at very high operating frequencies.
4. The technique does not leave a resin body exposed on either side of the substrate.
5. The substrate provides effective protection of the integrated circuits, to at least as high a degree as the resin body used in the known technique.
6. The assembly process is simplified, since there is no need for a wire bonding step, an underfill step, a moulding step, etc.

The surface of each integrated circuit carrying the circuitry may be formed by conventional flip chip technology. The wall of the chamber which this surface of the integrated circuit faces may include contact points in register with the electric contacts of the integrated circuit, and electrically connected to leads which extend through the substrate material, e.g. to an outer surface of the substrate. When the integrated circuit is inserted into the chamber, the respective contact points of the integrated circuit and wall may directly contact each other, or with a conducting material located between them. This connection may be formed by the flip-chip process conventionally known as "thermal compression" (in which force and temperature are simultaneously applied with an ACF (anisotropic conductive film) or ACP (anisotropic

conductive paste) between the integrated circuit and corresponding contacts of the chamber) and/or the flip-chip process conventionally known as "solder reflowing" (such as IR solder reflowing).

- 5 The two integrated circuits may be adhered together at their ground down surfaces, for greater stability. This may be done to form a composite body, which is subsequently placed into the chamber. Alternatively, the integrated circuits may be placed consecutively into the chamber, and optionally adhered together there.

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Preferably an electrically conductive layer is placed between the integrated circuits, extending over at least a part, and more preferably substantially all, of the interface between the integrated circuits. The conductive layer may for example be adhesive too, so that it performs both roles. This conductive layer
15 may act as a common earth to which one or more of the electric contacts of either or both of the integrated circuits may be connected.

In some arrangements, the substrate may be formed as two or more substrate elements which are joined together sandwiching the integrated circuits.

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- One possibility is for each of two substrate elements to contain a cavity, and for the two substrate elements to be placed with the cavities facing each other to define the chamber. The cavities may be of the same size, or of different sizes, e.g. to receive respective integrated circuits of different respective sizes. Each
25 of the cavities extends through the entire thickness of the primary substrate element from a first major surface of the primary substrate to a second major surface of the primary substrate, and has two openings.

- Another possibility, is for the chamber to be formed as a cavity within a primary
30 substrate element, and for the cavity to be closed by one or more secondary substrate elements which are arranged to extend over an opening of the cavity on the first and second major surface of the primary substrate. The second

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substrate elements may be thinner than the primary substrate elements and integrated circuits, and may contain electric circuitry.

The integrated circuit package may further include, on one or both sides of the primary substrate element, (i) one or more additional integrated circuits (preferably integrated circuits ground down on their major surface opposite the circuitry, as discussed above) on the outer surfaces of the secondary substrate elements, and (ii) tertiary substrate elements over the additional integrated circuits. The electrical contacts on the additional integrated circuit(s) may face and be electrically connected to either of the secondary substrate elements or the tertiary substrate elements. Any space remaining between the secondary and tertiary substrate elements may be filed by resin material (e.g. injected as a liquid into the space and then cured), and/or by "spacer" elements which are placed onto the secondary substrate elements before the tertiary substrate elements are located there.

Optionally, this combination of (i) additional integrated circuits and (ii) additional substrate elements, may repeated an arbitrary number of times on one or both sides of the primary substrate element.

In any case, further integrated circuits may be located on the outer surface(s) of the substrate. These further integrated circuits may be flip-chips with electrical contacts directed onto the outer surfaces of the substrate. Alternatively any one or more of these further integrated circuits could be fixed to the outer surface(s) of the substrate by wire bonding.

Brief Description of The Figures

Preferred features of the invention will now be described, for the sake of illustration only, with reference to the following figures in which:

Fig. 1, which is composed of Figs. 1(a) to 1(c), shows steps which are part of a method which is an embodiment of the invention; and

Fig. 2 shows two substrate elements for use in the method of Fig. 1;

Fig. 3 shows a package which is a result of the method of Fig. 1;

Fig. 4 shows two substrate elements which may be used in a variation of the first embodiment; and

Fig. 5 shows in cross-section a second embodiment of the invention.

5 Detailed Description of the embodiments

Referring firstly to Fig. 1(a) two integrated circuits 1, 3 for use in the embodiment are shown. These integrated circuits are similar to conventional flip chips. They have major surfaces 11, 13, 31, 33. A first major surface 11, 31 of each flip-chip includes electrical components. As in conventional flip-chips, these major surfaces also include bumps 15, 35 for making electrical contact with a substrate as explained below. These bumps may be made of solder, gold stud, gold plated or nickel plated polymer, copper pillars, etc.

15 In a first step of the embodiment, the integrated circuits 1, 3 are ground down by a grinding operation performed to their surfaces 13, 33 to reduce the thickness of the integrated circuits.

In a second step of the embodiment, the integrated circuits 1, 3 are adhered together by a layer 5 of adhesive, to give a composite body 7 having bumps 15, 35 on both sides.

The composite body 7 can then be embodied into a substrate 9 which is composed of two substrate elements 91, 93, shown in Fig. 2, which contain respective cavities 95. The substrate elements 91, 93 have respective surfaces 911, 931 which can be placed facing each other such that the cavities 95 together form a chamber 97. The substrate 9 can be of any conventional type, such as a flex substrate, ALIVH (any layer interstitial via holes) substrate, ceramic substrate, lead frame substrate etc. It may be a PCB, with wiring printed on its major surfaces opposite the surfaces 911, 931.

Pick and place equipment is used to arrange the composite body 7 and substrates 91, 93 with the substrate elements 91, 93 sandwiching the composite body. The composite body is located in the chamber 97 formed by the two cavities 95. The completed package 2 is shown in cross-section in Fig. 3.

The substrate 9 contains electric contacts 92 which are in register with the contacts 15, 35 of the composite body 7, so that electrical connections are formed between corresponding contacts when the composite body 7 is placed into the chamber 97. As in known flip chip technology, an interconnect material may be used between the respective contacts, such as an ACF or ACP (anisotropic conductive film or paste), an ICP (isotropic conductive paste), NCF or NCP (non-conductive film or non-conductive paste), and/or an adhesive. The MSL (moisture sensitivity level) performance of the package 2 may only depend on the substrate material, and not on under-fill or mould compound properties.

One or both of the substrate elements 91, 93 may contain electrical connections (not shown) which extend transverse to the surfaces 11, 13, 31, 33 and/or connections 94 which extend parallel to the surfaces 11, 13, 31, 33. Furthermore, components (such as passive components) may be provided within one or both of the substrate elements 91, 93. For example, these may be printed on the surfaces 911, 931 before they are placed together.

Optionally, the substrate elements may include apertures 98 for receiving a resin material 99 (such as an epoxy material). The apertures 98 are in communication with the chamber 97, and the resin material is injected into the chamber 97 after the substrate elements 91, 93 have been joined together sandwiching the composite body 7 in the chamber 97.

Additional electronic components 22 (which can comprise active and/or passive components) can be provided on the outer major surfaces 24 of the package 2, as in conventional techniques. These components 22 are
5 electrically connected to each other as in conventional techniques (e.g. if the outer surfaces 24 of the substrate 9 is equivalent to a conventional PCB), and may be connected to the electrical contacts 15, 35 on the composite body 7 by the connections which extend transverse to the outer surfaces 24 of the package 2. The components 22 may be provided as close to each other as
10 the components conventionally mounted on the surfaces of a PCB.

The electrical connections to and between the integrated circuits 1, 3 (especially the connections extending transverse to the surfaces 24) may be significantly shorter than the connections in conventional packaging
15 techniques, and this reduced routing path leads to more robust signals, having less signal distortion at high operating frequency.

Many variations of the first embodiment are possible within the scope of the invention.

20 For example, although the integrated circuits 1, 3 have the same areas (i.e. the rectangular surfaces 11, 13, 31, 33 each have the same length and each have the same width), the invention is not limited in this respect. For dies of different areas, it may be preferable to form the cavity to be in a shape other
25 than a cuboid. For example, the respective cavities 95 in the substrate elements 91, 93 may be of different sizes to receive respective integrated circuits of different areas, as shown in Fig. 4.

Additionally, although the embodiment shown uses two substrate elements
30 91, 93, the invention is not limited in this respect, and the substrate may

include any number of layers which may be combined together to form a substrate having a chamber. Electronic components, such as passive components, may be provided on any of the surfaces of any of these layers.

5 In a further variation, the two integrated circuits 1, 3 need not be formed into a composite body before being located in the chamber. Rather, they may be located there in separate steps carried out by the pick and place equipment. Optionally, they may be adhered are being inserted into the chamber 97.

10 Turning to Fig. 5, a second embodiment of the invention is shown. In this embodiment elements corresponding to those of the first embodiment are shown by reference numerals 100 higher. Elements of the second embodiment which do not correspond exactly to elements of the first embodiment are indicated by reference numerals starting with "2".

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The second embodiment includes two integrated circuits 101, 103 adhered together by an adhesive layer 105. The integrated circuits 101, 103 have major surfaces 111, 131 which include electronic components. The opposite surfaces of the integrated circuits have been ground down as described
 20 above, and are adhered together by the layer 105. The integrated circuits 101, 103 are of different areas, though they may have substantially the same thickness. The integrated circuits 101, 103 are located within a chamber 197 which is formed as a cavity in a primary substrate element 201. The upper and lower openings of the cavity are closed by secondary substrate elements
 25 203, 205, which are thin layers, containing electronic routing circuitry. Electric contacts 192 of this circuitry contact respective electric contacts 115, 153 of the integrated circuits 101, 103. The chamber 197 may optionally be filed with a resin material, which is injected and then cured.

The package may further include additional integrated circuits 231, 233, 251, 253 located on the outer sides of the secondary substrate elements 203, 205, and tertiary substrate elements 214, 216 covering the additional integrated circuits 213, 233, 251, 253. The additional integrated circuits 231, 233, 251, 253, like the integrated circuits 101, 103 have a first major face containing electrical circuitry and electrical contacts 235, 237, 255, 257, and a second major face which has been ground down. Any of the additional integrated circuits 231, 233, 251, 253 may have their electrical contacts facing the corresponding secondary substrate elements 203, 205, or facing the corresponding tertiary substrate elements 214, 216.

The spaces 211, 213 between the secondary substrate elements 203, 205 and the tertiary substrate elements 214, 216 may be filled by a resin material (such as an underfill layer) which is injected and then cured. Optionally, spacer elements 207, 209 may be provided in the spaces 211, 213 to increase mechanical stability and/or to reduce the amount of resin material required.

The outer faces of the tertiary substrate elements 214, 216 constitute outer surfaces of the package, and are available for electronic components, corresponding to the components 22 of Fig. 3, to be located on them.

In variations of the second embodiment, the structure of Fig. 5 can be built up on one or both sides, by adding on one or both sides additional integrated circuits and additional tertiary substrate elements covering the additional integrated circuits. This process can be carried out for as often as desired.

Claims

1. A method of packaging two integrated circuits, each of the integrated circuits having circuitry on a first of its major surfaces, the method including:

grinding a second major surface of each of the first and second
5 integrated circuits;

positioning the first and second integrated circuits with their second major surfaces facing one another within a chamber formed within a substrate; and

forming electrical connections between electric contacts of the first
10 integrated circuit and electrical contacts of the substrate, and between electric contacts of the second integrated circuit and electrical contacts of the substrate.
2. A method according to claim 1 in which the chamber has at least one wall which includes contact points which are in register with electric contacts
15 of the first integrated circuit when the first integrated circuit is located in the chamber, the substrate further including leads extending from the contact points through the substrate material.
3. A method according to any preceding claim further comprising placing an electrically conductive layer between the integrated circuits, extending over
20 at least a part of the interface between the integrated circuits.
4. A method according to any preceding claim further comprising adhering the first and second integrated circuits together to form a composite body before locating the composite body in the chamber.
5. A method according to any preceding claim in which the substrate is
25 composed of at least two substrate elements which each include at least one

cavity, and the substrate elements are located with the cavities in register to form the chamber.

6. A method according to claim 5 in which one or both of the substrate
5 elements is a printed circuit board.

7. A method according to any of claims 1 to 4 in which the substrate
comprises:

10 a primary substrate element which includes at least one cavity having at
least one opening, and

one or more laminar secondary substrate elements which extend over
the opening or opening.

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8. A method according to claim 7 in which the secondary substrate
elements include electrical circuitry.

9. A method according to any preceding claim including attaching one or
20 more additional integrated circuits to the substrate and covering them by one or
more tertiary substrate elements.

10. An integrated circuit package comprising:

25 (a) a substrate defining a chamber;

(b) a first integrated circuit having circuitry on a first of its major
surfaces and having a thickness less than that of the substrate and located
within the chamber;

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(c) a second integrated circuit having circuitry on a first of its major surfaces and located in the chamber with second major surfaces of the first and second integrated circuits facing one another;

5 (d) electrical connections between electric contacts of the first integrated circuit and electrical contacts of the substrate, and between electric contacts of the second integrated circuit and electrical contacts of the substrate; wherein

10 (e) the substrate is composed of at least two substrate elements each of which includes at least one cavity, and the substrate elements are located with the cavities in register thereby forming the chamber.

11. A package according to claim 10 in which the chamber has at least one
15 wall which includes contact points which are in register with electric contacts of the first integrated circuit, the substrate further including leads extending from the contact points through the substrate material.

12. A package according to claim 10 or 11 further comprising an electrically
20 conductive layer between the integrated circuits, extending over at least a part of the interface between the integrated circuits.

13. A package according to any of claims 10 to 12 the first and second integrated circuits are adhered together to form a composite body.

25 14. A package according to any of claims 10 to 13 in which one or both of the substrate elements is a printed circuit board.

15. An integrated circuit package comprising:

5 (a) a substrate defining a chamber;

(b) a first integrated circuit having circuitry on a first of its major surfaces and having a thickness less than that of the substrate and located within the chamber;

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(c) a second integrated circuit having circuitry on a first of its major surfaces and located in the chamber with second major surfaces of the first and second integrated circuits facing one another;

15 (d) electrical connections between electric contacts of the first integrated circuit and electrical contacts of the substrate, and between electric contacts of the second integrated circuit and electrical contacts of the substrate; wherein

20 (e) the substrate comprises a primary substrate element comprising at least one cavity having at least one opening, each of the at least one cavity extending through the entire thickness of the primary substrate element from a first major surface of the primary substrate to a second major surface of the primary substrate and having two openings; and

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(f) one or more laminar secondary substrate elements which extend over the opening or openings, the secondary substrate elements lying against the first or second major surface of the primary substrate.

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16. A package according to claim 15 in which the secondary substrate elements include electrical circuitry.

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17. A package according to any of claims 10 to 16 further including one or more additional integrated circuits and covered by one or more tertiary substrate elements.

10 18. A package according to any of claims 10 to 17 in combination with one or more electronic components electrically connected to the package and mounted on an outer surface of the package.