IMPROVED PILLAR CONNECTIONS FOR SEMICONDUCTOR CHIPS AND METHOD OF MANUFACTURE

BACKGROUND OF THE INVENTION

This invention relates in general to interconnections for semiconductor devices and, in particular, to pillar-shaped connections from a semiconductor chip to a substrate and method for making the connections.

Tin lead based solders is the preferred interconnect material of choice for flip chip bonding of silicon integrated circuits. As dimensions of the electronic devices on the silicon integrated circuits are continually reduced, α particle emissions by lead can cause significant problems. Lead has three stable isotopes which are formed as the end products of natural radioactive decay chains. These stable isotopes, however, usually contain a small amount of residual α particle radioactivity. As the dimensions of electronic devices in silicon integrated circuits become smaller, the distances between the lead-based solder and the devices are also reduced so that the α particle emission from the solder can cause such devices to malfunction.

One way to reduce the effect of α particle emission from solder is to provide a passivation layer covering the electronic devices on silicon. Some materials used for the passivation layer are more effective than others for preserving the integrity of the electronic devices from the α particles. Furthermore, the residual α particle emission from the solder radiate from essentially point sources in the solder, so that the intensity of α particle emission experienced by the electronic devices decreases rapidly with the distances separating the devices from the solder. Shown below is a table setting forth five different materials serving as the medium separating electronic devices from the solder.

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MEDIA (Compound)	Density ρ ($g.cm^{-3}$)	Mol. Wt. M(g)	-dE/dx ($eV.cm^2$/1e15 atoms)	Effective Thickness d(cm)
Air	1.161e-03	39.11	20.96	10.83
Polyimide	1.61	38.0	18.91	0.0084
Epoxy	1.20	40.0	19.68	0.0114
SiO_2	2.65	60.0	27.42	0.0055
Si_3N_4	3.17	140.0	28.18	0.0105

As can be seen from the table above, if air is the only medium that separates the electronic devices from the solder, then in order for the electronic devices not be significantly affected by the α particle emission from the solder, the effective thickness of the air medium separating the electronic devices and the solder should be at least 10.83 cm, which is unacceptable for most applications. From the above table, it will be noted that the best barrier layer substance in terms of minimum absorption length for absorption of α particles from the solder is silicon dioxide, followed by polyimide. Where silicon dioxide or another solid material is used as the passivation layer, only part of the medium separating the electronic devices from the solder is occupied by the material, with the remaining part occupied by air or another material not as effective in absorbing α particles. It will be noted from the table, however, that even where silicon dioxide is used as a compound for the passivation layer covering the electronic devices on silicon, it is preferable that the electronic devices and the solder be separated by at least 0.0055 cm or 55 microns. For polyimide passivation layers, the separation is preferably at least 84 microns.

Conventional interconnect methods employ lead-based solders for connecting flip chips to substrates. Aside from the α particle emission problem described above,

as the structural dimensions of electronic devices get smaller, the use of lead-based solder bumps is disadvantageous also because it may be difficult to achieve a fine pitch between adjacent interconnects without bridging which causes electrical shorting. When the solder bump is formed by electroplating, and where the photoresist is not thicker than 60 microns, the bump size in the horizontal plane of a 100 micron high solder ball will be around 120 microns, and the plated solder bump is in the shape of a mushroom. Therefore, if the pitch or distance between adjacent interconnects using solder bumps of such height is reduced to below 150 microns in either the array or peripheral format, bump bridging can easily occur. It is, therefore, desirable to provide an improved interconnect system to achieve finer pitch with minimum probability of bump bridging and where α particle emission will not significantly affect the functions of electronic devices on the semiconductor chips.

In the document entitled "Wire Interconnect Technology, A New High-Reliability Tight-Pitch Interconnect Technology," by Love et al., from Fujitsu Computer Packaging Technologies, Inc. an all copper interconnect post is proposed. Instead of using lead based solder, the flip chip is connected to a substrate by means of an all copper post which is about 45 or 50 microns in length. While such copper-based interconnects may be able to achieve a finer pitch between adjacent interconnects, such proposed solution still does not avoid the problem of the α particle emission described above. As shown in Fig. 1 of the article by Love et al., solder is used to attach the copper posts to the substrate. Since the height of the copper post or pillars is not more than 50 microns in height, even where silicon dioxide is used as the passivation layer covering the electronic devices on the flip chips, the electronic devices may still be adversely affected by α particle emission by the solder used to attach the copper posts to the substrate. Furthermore, as known to those skilled in the art, the space between the semiconductor flip chip and the substrate is usually filled with an underfill material to provide support and stability to the interconnect structure. Typically, the process of providing the underfill material is by injection that requires a certain minimum separation between the semiconductor chip and the substrate. For most injection processes, the minimum separation is about 75 microns. Therefore, using the interconnect structure proposed by Love et al. in the article, there appears to be inadequate separation between the semiconductor chip and the substrate for injecting the underfill material. The process employed by Love et. al appears to limit the height of the copper post achievable to not more than 50 microns.

None of the above-described interconnect systems is entirely satisfactory. It is, therefore, desirable to provide an improved interconnect system in which the above-described difficulties are not present.

SUMMARY OF THE INVENTION

This invention is based on the observation that an elongated pillar may be advantageously used for connecting a semiconductor chip to a substrate, where the pillar comprises two elongated portions, one portion including a metal material that does not include lead, such as a material including copper, higher reflow temperature solder or gold, and another portion including solder or other wettable material. The portion including the non-lead metal material is in contact with the semiconductor chip and has a length not less than about 50 microns. Preferably, the total length of the pillar is not less than about 55 microns. In a more preferred embodiment, the length of the pillar is not less than about 84 microns, with the length of the portion of the pillar including copper not less than about 55 microns.

Using the elongated pillar of this invention, the separation between the solder in the pillar or any other solder used in the interconnect on the one hand and electronic devices on the semiconductor chip on the other hand can be made to exceed 55 microns or even 84 microns so that adverse effects caused by α particle emission from the solder on the electronic devices on the semiconductor chip will be reduced. This is especially the case where silicon dioxide or polyimide is used as the passivation layer.

In the case where alpha particle is not a concern, all portions of the interconnect can be of made of solder material containing lead in elongated pillar shape.

Where the length of the pillar exceeds 75 microns, adequate separation is provided between the semiconductor chip and the substrate for the injection of the underfill material. Furthermore, by providing elongated pillars of adequate length and suitable cross-sectional dimensions connecting the semiconductor chip to the substrate, the stress induced in the connection between the semiconductor chip and the pillar due to warpage is much reduced, which also reduces the chances of chip failure caused by shear stress on account of the warpage.

The elongated pillar may be formed by first depositing a layer of metal for plating purposes and followed by forming a layer of photosensitive material on the

chip and exposing to radiation the layer of photosensitive material at predetermined areas. Portions of the layer that are exposed to radiation are removed to form through holes in the layer. Portions of the holes are filled with a material containing a metal to form an elongated column in contact with the chip. The metal material is different from top layer metal (and preferably does not include lead.) Portions of the holes are then filled with a material containing any wettable metal to form an elongated column of metal in contact with the bottom portion material, thereby forming a composite pillar, a portion of which includes the metal material and another portion of which includes a wettable metal. The photosensitive layer and deposited layer of metal for plating purposes are then removed to form the elongated pillars. After the pillars have been formed, the pillars may or may not be reflowed prior to being connected to the substrate. Preferably, the filling of the holes of the photosensitive material layer with copper, gold, non lead or solder is done by electroplating. Also preferably the thickness of the photosensitive layer and the depth of the holes therein are such that they are adequate to form the pillars of sufficient height, such as the ones described above.

To enhance the reliability of the portions of the pillars including the metal material, it may be desirable to provide a layer of material covering such portions; the metal material is different from solder and preferably does not include lead. Where such portions include copper, this may be achieved by forming a layer of copper oxide on the sidewall surface of such portion of at least one of the pillars. The copper oxide will also reduce wetting of the sidewall surface during solder reflow, thereby facilitating control of the height of the solder portion of the at least one pillar during solder reflow.

Another aspect of the invention is directed to a flip chip interconnect system for use with a semiconductor chip. Two elongated portions may be employed: a first portion including solder, non lead solder or a wettable material including nickel and gold, and a second portion containing a material with higher reflow temperature than that of the first portion, said second portion in contact with the semiconductor chip. The second portion may or may not contain lead.

Yet another aspect of the invention is directed to a flip chip interconnect system for use with a semiconductor chip, comprising an elongated portion in contact

with semiconductor chip and a ball-shaped portion, said elongated portion including copper, or a solder metal with higher reflow temperature than the ball-shaped portion, said ball shaped portion include a solder material. The elongated portion may or may not contain lead.

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BRIEF DESCRIPTION OF THE DRAWINGS

Fig 1A is a cross-sectional view of a flip chip connected to a substrate using the elongated pillars of this invention to illustrate the invention.

Fig. 1B is an exploded view of a portion 1B of the system of Fig. 1A showing 10 in more detail the interconnection between the elongated pillar, the silicon die and the substrate.

Figs. 2A-2G are cross-sectional views of a portion of a semiconductor die and various layers associated with the die at various stages of fabrication to illustrate a process for making the elongated pillars attached to the die and the attachment of such 15 pillars to a substrate to illustrate an embodiment of the invention.

Fig. 3A is a perspective view of a flip chip with elongated pillars on one side of the chip to illustrate an embodiment of the invention.

Fig. 3B is a cross-sectional view of a portion 3B of the chip of Fig. 3A to illustrate the embodiment of the invention.

20 Fig. 3C is a cross-sectional view of a portion of the flip chip and the substrate after the flip chip has been attached to the substrate and the underfill material injected to illustrate an embodiment of the invention.

Fig. 4A is a cross-sectional view of a flip chip connected to a substrate where both the flip chip and the substrate are warped to illustrate the shear stress in the chip.

25 Fig. 4B is a top view of the flip chip of Fig. 4A.

Figs. 5A and 5B are graphical illustrations of shear stress distribution for a 20 mm die where the die is connected to a substrate using elongated pillars of this invention of 100 microns in height and bump diameter of 60 and 100 microns, and at a bump pitch of 100/120/160/225 microns to illustrate the invention.

30 Fig. 6A and 6B are graphical illustrations of the shear stress in the semiconductor die similar to that shown in Figs. 5A and 5B except that the height of the elongated pillar is 125 microns instead of 100 microns.

For simplicity in description, identical components are identified by the same numerals.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 1A is a cross-sectional view of a semiconductor die in the form of a flip chip 12 connected to a substrate 14 by means of elongated pillars 16 to illustrate an embodiment of the invention. As shown in Fig. 1A, the space between the die 12 and substrate 14 is filled with an underfill material 18 such as one known to those of skill in the art to provide support and stability to the die and interconnect structure formed by the elongated pillars 16.

Fig. 1B is an exploded view of a portion 1B of the system of Fig. 1A showing in more detail an elongated pillar connecting a portion of the silicon die to the substrate. As shown in Fig. 1B, pillar 16 comprises two parts: an upper elongated portion 16a comprising copper of height H1 and a second elongated portion of height H2 comprising a lead-based solder. The junction between the two portions 16a, 16b is at 16c. The bottom part of portion 16b is enlarged compared to its upper part and has a substantially conical shape where the bottom part of the solder portion of 16b is the result of a reflow process as described below to make physical and electrical contact with the copper contact layer 22 on top of substrate 14. The upper end of portion 16a is in attached to a copper contact 24 on the silicon die 12. In this manner, circuits on the silicon die 12 are electrically connected through pillar 16 to a copper contact 22 on the substrate 14. As shown in Figs. 1A and 1B, the space between the semiconductor die 12 and substrate 14 is filled with an underfill material 18.

As shown in Fig. 1B, circuits (not shown) on the silicon die 12 are spaced apart from the solder portion 16b by the length or height of portion 16a containing copper. The surface of the silicon die 12 facing the substrate is coated with a passivation layer (not shown) made of a suitable material such as silicon dioxide or polyimide. Therefore, if the length or height H1 of portion 16a exceeds the effective thickness shown in the table above, then the circuits on die 12 will not be significantly adversely affected by the α particle emission from solder 16b. In the preferred embodiment, the height H1 of the portion 16a is not less than 55 microns, where silicon dioxide is used as the passivation layer, and more preferably, more than 84 microns where polyimide is used as the passivation layer. To permit many injection processes to be used for injecting the underfill material 18, the total height H of pillar 16 between die 12 and the substrate 14 is at least 75 microns, such as in the range of about 80 -100 microns. For reasons discussed below, a larger value for H would reduce the shear stress experienced by the silicon die and the connection between the

die 12 and pillar 16. Thus, it may be preferable for the total height H of the pillar to be at least 100 microns, and more preferably 120 microns or more, such as 125 microns. It may be preferable for the ratio H1 to H2 to be about 3 to 1.

Figs. 2A-2G are cross-sectional views of a semiconductor die and the various layers associated therewith to illustrate the process for making the elongated pillar interconnect shown in Figs. 1A, 1B and of process for connecting the pillar to a substrate to illustrate the invention.

As shown in Fig. 2A, a photosensitive layer 32 is formed on the die 12. To simplify the drawing, only portions of the die and of the various layers are shown in Figs. 2A-2G. Various designated areas of the photosensitive layer are exposed to radiation, and the portions that are exposed to radiation are then removed to yield layer 32' with a pattern of through holes 34 therein as shown in Fig. 2B, where the through holes reach all the way to die 12. Portions of the through holes 34 are filled with a material including copper, such as by placing the entire structure in a copper bath. An electric current is passed there through to perform electroplating of the copper material to fill at least a portion of each hole 34 as shown in Fig. 2C. As shown in Fig. 2C, copper material 16a fills a portion of each of holes 34. The entire structure is then transferred to a bath of material containing solder and electroplating is again employed to fill portions of holes 34, resulting in the structure shown in Fig. 2D, where a solder material 16b' fills portions of the holes 34. The photosensitive remaining layer 32' is then removed to form the structure of Fig. 2E. As shown in Fig. 2E, two elongated pillars 16' are then formed, each comprising a copper portion 16a and a solder portion 16b'. To connect the pillars to the substrate, portions 16b' are placed in contact with the copper contacts 22 on the substrate 14 as shown in Fig. 2F. The portions 16b' containing solder are then heated in a manner known to those skilled in the art to reflow the solder 16b' to form the solder portions 16b and pillars 16 as shown in Figs. 1B and 2G. An underfill material 18 is then injected to fill the space between die 12 and substrate 14. Contacts 24 on die 12 are, therefore, physically and electrically connected and attached to contacts 22 on the substrate 14. The resulting structure is illustrated in Fig. 2G.

To provide a metal contact between the pillars and the semiconductor die, an underbump metalization layer (typically composed of a material including Titanium (Ti), titanium-tungsten (TiW), or chromium (Cr) and copper function as an adhesion

layer during the above-described process. This layer also serves as the conducting metal contact for the copper portions of the pillars for the above-described electroplating process. After the photosensitive layer 32' has been removed, all portions of this underbump metalization layer, except for the portions underneath the pillars are removed. For simplicity, this layer has been omitted from the figures.

The spacing or pitch P between adjacent elongated pillars 16 is as illustrated in Fig. 1A and 2E, Using the process described above, fine pitch of not more than 100 microns is achievable; preferably, the pitch or spacing between adjacent pillars is in the range of about 80 to about 100 microns. Since solder forms a portion of the pillar, no extra process of placing solder on the substrate is required, and the connection between the pillar and the substrate can be simply formed by reflowing the solder portion of the pillar. Furthermore, through this process, no mushroom solder bump is formed so that finer pitch can be achieved. The solder composition is flexible and can be 63/37 or 5/95 SnPb ratio, or a non-lead solder. The copper material and solder material used in the above-described electroplating processes may simply be copper metal and solder.

Fig. 3A is a perspective view of a flip chip with elongated pillars on one side of the chip to illustrate an embodiment of the invention. Fig. 3B is a cross-sectional view of a portion 3B of the chip of Fig. 3A to illustrate the embodiment of the invention. Fig. 3C is a cross-sectional view of a portion of the flip chip and the substrate after the flip chip has been attached to the substrate and the underfill material injected to illustrate an embodiment of the invention, as indicated by arrow 100.

Another advantage of the elongated pillar interconnects of this invention is that it reduces shear stress experienced by warped silicon dies and the connection between the dies and the interconnects. This is illustrated in Figs. 4A, 4B. Fig. 4A is a cross-sectional view of a flip chip connected to a substrate where both the flip chip and the substrate are warped to illustrate the shear stress in the chip. Fig. 4B is a top view of the flip chip of Fig. 4A. As shown in Fig. 4A, the silicon die 12' and substrate 14' may become warped for a number of reasons, such as due to thermal effects. Warpage is calculated as Y displacement from center 12a' to the corner 12b' of the die as shown in Fig. 4A.

Figs. 5A and 5B are graphical plots illustrating shear stress distribution in a die of size 20 mm, where elongated pillars of 100 microns in length and diameters of 60 and 100 microns and at bump pitches of 100,120, 160, 225 microns. In the graphical plot, pitch is represented as P and diameter is represented by D. As shown in Figs. 5A and 5B, the peak shear stress at the edge of the die is less than the shear strength of copper so that the elongated pillars of this invention should not fail with the given geometry illustrated, or similar geometries, due to shear stress. Figs. 6A and 6B illustrate similar data to those shown in Figs. 5A and 5B but where the pillar height or length is 120 microns instead of 100 microns. A comparison of Figs. 6A and 6B to those of Figs. 5A and 5B will illustrate that the longer the pillars, the less will be the shear stress experienced at the edge of the die and the interconnects connected to the die.

A layer 50 shown in Fig. 1B of either organic or metal material may be used to cover the copper portion 16a. This will reduce reliability problems. The material used may be Entek or palladium, and may be formed by simply dipping the entire structure (i.e. die 12 and pillar 16) into a bath of such material, where the material will only adhere to the copper portion 16a.

It is found that during reflow of the solder as described above in order to connect the die to the substrate, the sidewall surface of the copper portion 16a may become wetted by solder. When this happens, the solder portion may change in height or even collapse so that the reflow and connection process is more difficult to control. Preferably, the sidewall surface of the copper portion 16a of pillar 16 is oxidized, thereby forming a layer of copper oxide on the sidewall surface. This reduces the chances that the sidewall surface of portion 16a will become wetted by solder during reflow. The layer of copper oxide can be formed by placing the pillars and the die, such as the components shown in Fig. 2E, in an oven heated to a temperature in the range of about 90 to 120 degrees Celsius, such as about 100 degrees Celsius, exposed to an environment that contains oxygen, such as air, for a time period in the range of about 15 to 60 minutes, such as about 30 minutes. While the embodiments have been described above using copper as the non-lead metal material to form the portion(s) of the pillar(s) in contact with the semiconductor chip, it will be understood that metals other than copper such as gold, Sn/Ag, and Sn/Cu can be used as well; such and other variations are within the scope of the invention.

As shown in Fig. 1B, the bottom part of portion 16b is enlarged as a result of a reflow process of the solder. Thus, initially the portion 16b may take the shape of an elongated column. This column may be reflowed to form a ball-shape (shown in dotted lines 16b" in Fig. 1B) prior to being placed in contact with the substrate system. Then the ball-shaped material is reflowed to form the shape shown in Fig. 1B.

Still other variations are possible. Thus, as long as the material in the portion 16a has a higher reflow temperature than portion 16b, the above described process is possible and can be advantageously used. Thus portion 16a may contain copper or a solder material with such higher reflow temperature. Where α particle emission is not a concern, portion 16a may also contain lead. Portion 16b may contain a solder material with or without lead. It may also comprise a wettable material that includes nickel and gold. Any one of such features may be advantageously combined with the above described features.

While the invention has been described above by reference to various embodiments, it will be understood that changes and modifications may be made without departing from the scope of the invention, which is to be defined only by the appended claims and their equivalents.

WHAT IS CLAIMED IS:

1. An elongated pillar connecting a semiconductor chip to a substrate, said pillar comprising at least two elongated portions, a first portion including a metal material that does not contain lead, and a second portion including solder, said first portion in contact with the semiconductor chip and having a length not less than about 50 microns.

2. The pillar of claim 1, wherein the length of the pillar is not less than about 55 microns.

3. The pillar of claim 1, wherein the length of the pillar is more than about 100 microns.

4. The pillar of claim 1, further comprising a layer of material covering the first portion.

5. The pillar of claim 4, said layer of material including an oxide of a metal in the first portion.

6. The pillar of claim 1, the first portion including copper.

7. The pillar of claim 6, further comprising a layer of copper oxide covering the first portion.

8. A semiconductor device comprising:

a semiconductor chip; and

a plurality of pillars connected to the chip, each of said pillars comprising at least two elongated portions, a first portion including a metal material not including lead, and a second portion including solder, said first portion in contact with the semiconductor chip and having a length not less than about 50 microns.

9. The device of claim 8, wherein the lengths of the pillars are not less than about 55 microns.

10. The device of claim 8, wherein the lengths of the pillars are more than about 100 microns.

11. The pillar of claim 8, further comprising a layer of material covering the first portion of at least one pillar of the plurality of pillars.

12. The device of claim 11, said layer of material including an oxide of a metal in the first portion.

13. The device of claim 8, the first portion of at least one pillar of the plurality of pillars including copper.

14. The device of claim 13, further comprising a layer of copper oxide covering the first portion of the at least one pillar of the plurality of pillars.

15. A method for making electrical connections to a semiconductor chip, comprising:

forming a layer of photosensitive material over the chip;

exposing the layer to radiation at predetermined areas and removing portions of the layer that are exposed to radiation to form through holes in the layer, thereby exposing areas of the chip through the holes;

filling portions of the holes with a metal to form an elongated column of metal material, so that the metal material is in contact with the chip;

filling portions of the holes with solder to form an elongated column of solder, so that the solder is in contact with the metal material; and

removing the layer.

16. The method of claim 15, wherein the filling is performed by a process that includes electroplating.

17. The method of claim 16, wherein the forming forms a layer of photosensitive material that is not less than about 50 microns in depth, and the filling with the metal material is performed so that the elongated column of metal material is not less than about 50 microns in length.

18. The method of claim 15, wherein the forming forms a layer of photosensitive material that is not less than about 50 microns in depth, and the filling

with the metal material and solder is performed so that the total length of the elongated column of metal material and of the column of solder is not less than about 55 microns in length.

19. The method of claim 15, wherein the forming forms a layer of photosensitive material that is not less than about 50 microns in depth, and the filling with the metal material and solder is performed so that the total length of the elongated column of metal material and of the column of solder is not less than about 100 microns in length.

20. The method of claim 15, further comprising placing the solder in contact with a substrate and applying heat to the solder to reflow the solder.

21. The method of claim 20, further comprising reflowing the column of solder to form a ball shape body prior to placing it in contact with the substrate.

22. The method of claim 15, further comprising forming a layer of material on a side surface of the metal material.

23. A method for making electrical connections to a semiconductor chip, comprising:

forming a plurality of pillars connected to a semiconductor chip, each of said pillars comprising at least two elongated portions, a first portion including a metal material, and a second portion including solder, said metal material different from the material in the second portion, said first portion in contact with the semiconductor chip; and

providing a layer of material on a side surface of the first portion of at least one of the plurality of pillars.

24. The method of claim 23, wherein said forming forms an elongated portion and a ball-shaped portion including a solder material, said elongated

portion containing a material with a higher reflow temperature than the material of the ball-shaped portion.

25. The method of claim 24, said providing including heating the metal material in an environment that contains oxygen to an elevated temperature to oxidize the metal material

26. A flip chip interconnect system for use with a semiconductor chip, comprising two elongated portions, a first portion including solder, non- lead solder or a wettable material including nickel and gold, and a second portion containing a material with higher reflow temperature than that of the first portion, said second portion in contact with the semiconductor chip.

27. The system of claim 26, said second portion including copper, gold or a solder metal.

28. A flip chip interconnect system for use with a semiconductor chip, comprising an elongated portion in contact with semiconductor chip and a ball-shaped portion, said elongated portion including copper, or a solder metal with higher reflow temperature than the ball-shaped portion, said ball shaped portion include a solder material.

29. The system of claim 28, wherein said ball shaped portion includes no lead.