ABSTRACT OF THE DISCLOSURE

A data sampling circuit has a shift register for sampling bit by bit a radio signal data which is constructed in unit of 32 bits, thereby holding and shifting a sampling data; a data loadable shift register for holding the sampling data; and a error correction unit for receiving bit by bit the sampling data from the data loadable shift register. The data loadable shift register completes a reception of the sampling data corresponding to the radio signal data of the given number of bits from the shift register at least before a time when a sampling of a first bit data in a next radio signal data which is constructed in unit of a given number of bits subsequent to the radio signal data is initiated by the shift register.