IPOS Copy
9806293-0

SEMICONDUCTOR ASSEMBLY WITH IMPROVED DIE ATTACHMENT TO A CARRIER

Field of the Invention

This invention relates to a semiconductor assembly comprising a die mounted to a carrier. The invention is particularly useful for, but not necessarily limited to, improving the die's attachment to the carrier.

Background of the Invention

Conventionally, a die containing electronic circuitry is mounted onto a carrier to form a semiconductor assembly. Typically, the carrier is formed with a non-conductive substrate having conductive pads. Generally, when the die's circuitry requires electrical grounding, a large conductive pad is used as a ground pad. Such a ground pad is normally rectangularly-shaped and takes up substantial space on the non-conductive substrate just beneath the die.

Conventionally, an adhesive is used to attach the die to the carrier. The adhesive needs to be electrically conductive for coupling the die to the ground pad. As is known in the art, adhesives do not bind well to metals, such as gold or silver, forming the ground pad. This causes an adhesion problem for mounting the die, particularly when there is little space on the carrier that is not taken up by the ground pad.

Summary of the Invention

It is an object of this invention to provide a semiconductor assembly with improved attachment of a die to a carrier.

According to one aspect of the invention, there is provided a semiconductor assembly comprising:

a carrier having a non-conductive substrate with an electrically conductive pattern thereon, said pattern including a

plurality of electrically interconnected members; and

a die having an electrically conductive surface, said die being mounted to said carrier, thereby electrically coupling said surface to said pattern.

Preferably, said die is mounted to said carrier with an adhesive.

Suitably, said adhesive may be electrically conductive.

Suitably, said adhesive can be applied to said pattern.

Alternatively, said adhesive may be non-conductive and is applied to said substrate.

Preferably, said surface and said pattern abut each other.

Suitably, said surface is planar.

Preferably, said pattern may be surrounded by a border, said border being raised above said substrate.

Suitably, said border may be formed by a conductive or non-conductive material.

Alternatively, said border may be recessed into said substrate to surround said pattern.

Preferably, said members may radially extend from a common area.

Suitably, one or more conductive pads outside of said border may be associated with at least one of said members.

Alternatively, said members may comprise at least one elongate member.

Brief Description of the Drawings

In order to describe the invention and to put it into practical effect, reference will now be made to preferred embodiments as illustrated with reference to the accompanying drawings in which:

FIG. 1 is an exploded view of a semiconductor assembly with a carrier in accordance with the invention; and

FIG. 2 is a plan view of a first preferred embodiment of the carrier of FIG. 1 in accordance with the invention.

FIG. 3 is a plan view of a second preferred embodiment of the carrier of FIG. 1 in accordance with the invention.

Detailed Description of the Invention

FIG. 1 is an exploded view of a semiconductor assembly 100 with a carrier 102 in accordance with the invention. The semiconductor assembly 100 includes a die 104 having an electrically conductive surface (not shown) underneath for electrically coupling to an electrically conductive pattern 106. The pattern 106 is formed with a metal, such as gold, on a non-conductive substrate 108 of the carrier 102. The pattern 106 serves as a ground pad for the die's 104 circuitry and is surrounded by a border 110 on the carrier 102. In addition to the pattern 106, segments 112 of the non-conductive substrate 108 are exposed within the border 110.

The carrier 102 and the die 104, when attached together, abut each other to form the semiconductor assembly 100. An adhesive (not shown) is used to attach the die 104 and can be electrically conductive or non-conductive. When using an electrically conductive adhesive, the adhesive can be applied anywhere within the border 110. Otherwise, when non-conductive, the adhesive is applied only to the segments 112 to avoid insulating the pattern 106 to the die's electrically conductive surface. The border 110 prevents a resin (not shown), applied over the die 104 after mounting to the carrier 102, from flowing out of the border 110 to other areas of the carrier 102. The border may be formed by a material, such as

a metal, that raises it above the non-conductive substrate 108. Alternatively, the border may be recessed into the non-conductive substrate 108 without requiring any material.

In accordance with the invention, FIG. 2 is a plan view of a first preferred embodiment 200 of the carrier 102 of FIG. 1. As shown in FIG. 2, the pattern 106 in FIG. 2 includes a plurality of electrically interconnected members 204 extending radially from a centre common area 206. One or more conductive pads 208 outside the border 110 is associated with the pattern 106 via at least one of the members 204.

In accordance with the invention, FIG. 3 is a plan view of a second preferred embodiment 300 of the carrier 102 of FIG. 1. In this second preferred embodiment 300, the segments 112 are enclosed by the plurality of electrically interconnected members 204, and, as with the first preferred embodiment 200, one or more conductive pads 208 outside the border 110 is associated with the pattern 106 via at least one of the members 204.

In this invention, the pattern 106 advantageously enables effective attachment of the die 104 to the carrier 102 regardless of the type of adhesive used. As shown in FIGs. 2 and 3, the members 204 in both embodiments 200,300 of the carrier 102 have the segments 112 adjacent to at least one elongate member 210,310 to thereby enable the adhesive to bind either to the pattern 106 or the segments 112. Hence, the pattern 106 improves on conventional carriers with ground pads having little or no space to attached with dies. Further advantageous in this invention is that the segments 112 results in less use of the metal required for the pattern 106, and this saves on cost when metals, such as gold, is used to form the pattern 106. Therefore the invention described herein provides a semiconductor assembly 100 with a carrier 102 adhesively attaching a die 104 effectively and economically.

CLAIMS

We claim:

1. A semiconductor assembly comprising:
a carrier having a non-conductive substrate with an electrically conductive pattern thereon, said pattern including a plurality of electrically interconnected members; and
a die having an electrically conductive surface, said die being mounted to said carrier, thereby electrically coupling said surface to said pattern.

2. The semiconductor assembly as claimed in Claim 1 wherein said die is mounted to said carrier with an adhesive.

3. The semiconductor assembly as claimed in Claim 2 wherein said adhesive is electrically conductive.

4. The semiconductor assembly as claimed in Claim 3 wherein said adhesive is applied to said pattern.

5. The semiconductor assembly as claimed in Claim 2 wherein said adhesive is non-conductive and is applied to said substrate.

6. The semiconductor assembly as claimed in Claim 1 wherein said surface and said pattern abut each other.

7. The semiconductor assembly as claimed in Claim 1 wherein said surface is planar.

8. The semiconductor assembly as claimed in Claim 1 wherein said pattern is surrounded by a border, said border being raised above said substrate.

9. The semiconductor assembly as claimed in Claim 8 wherein said border is formed by a conductive material.

* C L M S *

10. The semiconductor assembly as claimed in Claim 8 wherein said border is formed by a non-conductive material.

11. The semiconductor assembly as claimed in Claim 8 wherein one or more conductive pads outside of said border is associated with said pattern.

12. The semiconductor assembly as claimed in Claim 1 wherein said pattern is surrounded by a border, said border being recessed into said substrate.

13. The semiconductor assembly as claimed in Claim 12 wherein one or more conductive pads outside of said border is associated with said pattern.

14. The semiconductor assembly as claimed in Claim 1 wherein said members radially extend from a common area.

15. The semiconductor assembly as claimed in Claim 1 wherein said members comprise at least one elongate member.

16. A semiconductor assembly manufactured substantially as described herein with reference to and as illustrated by the accompanying drawings.