

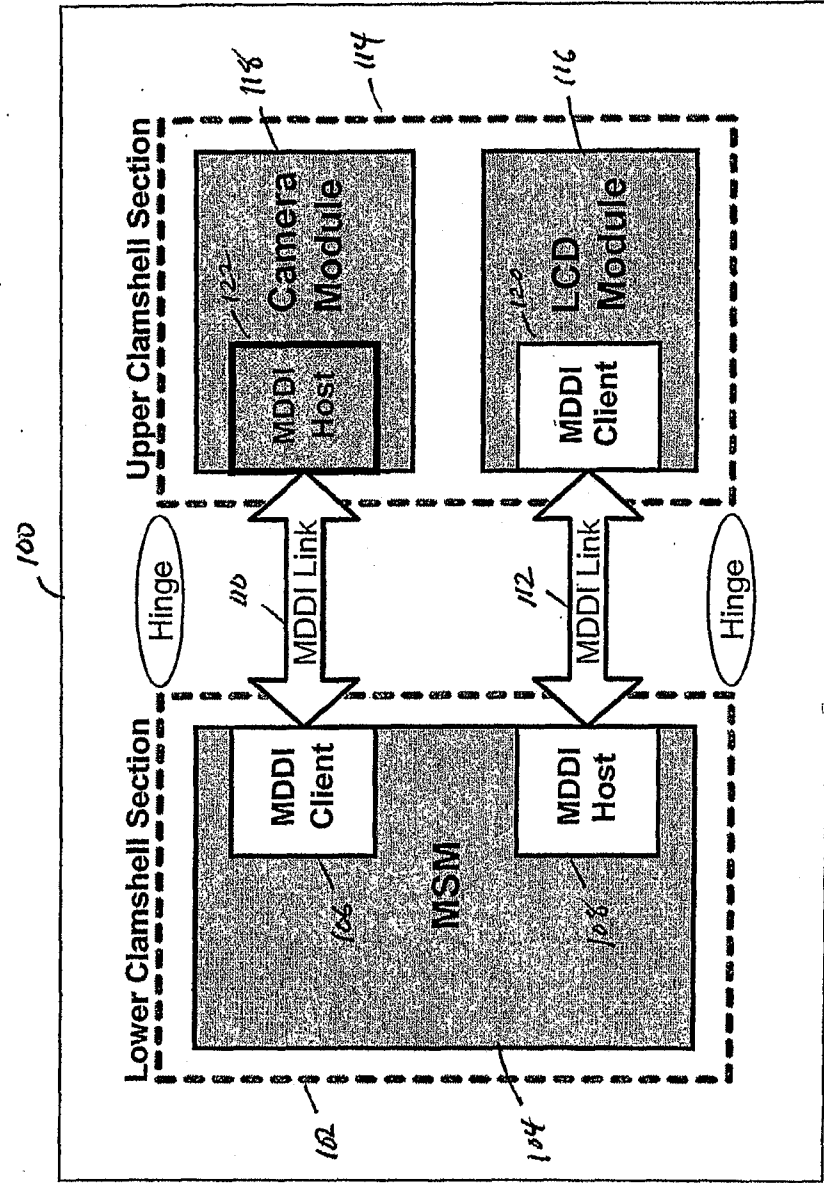


FIG. 1

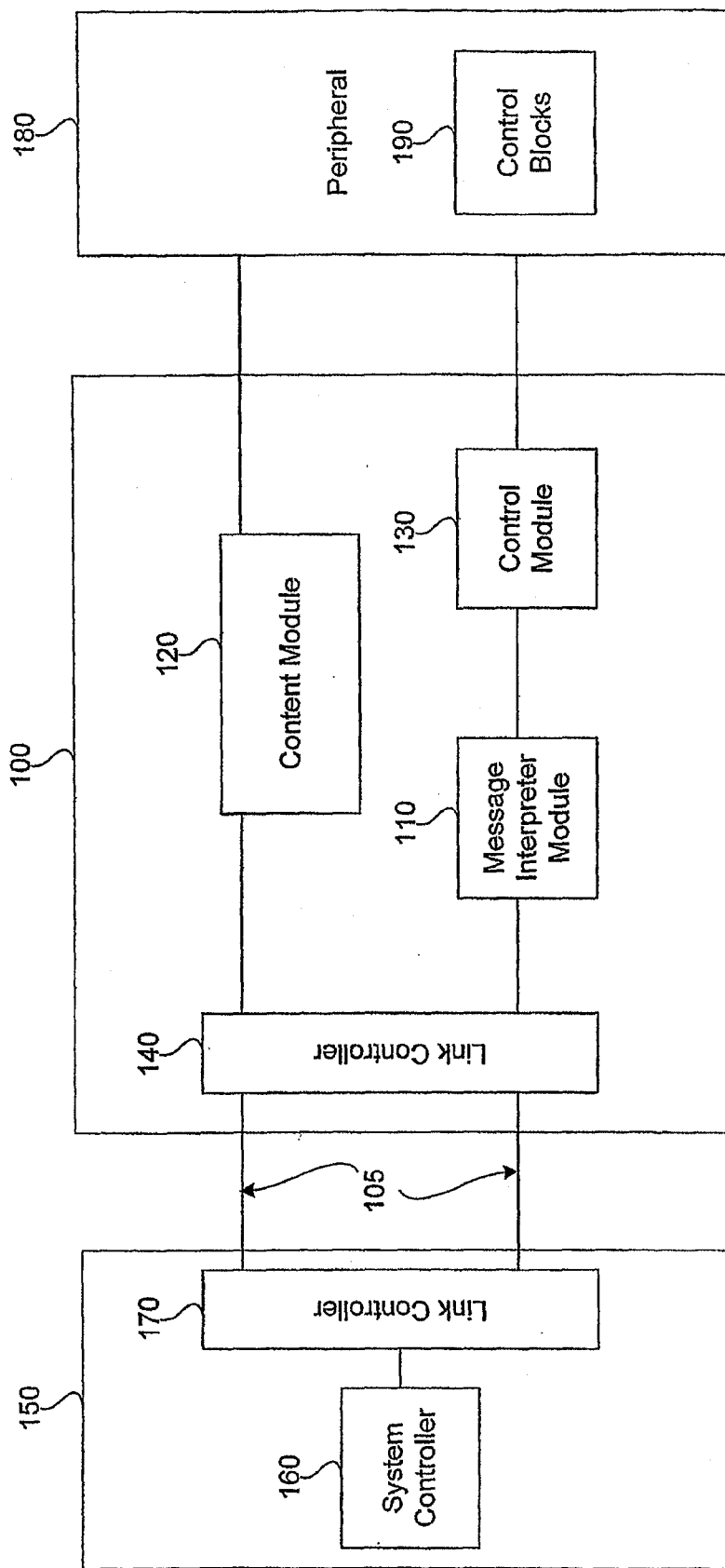


FIG. 1A

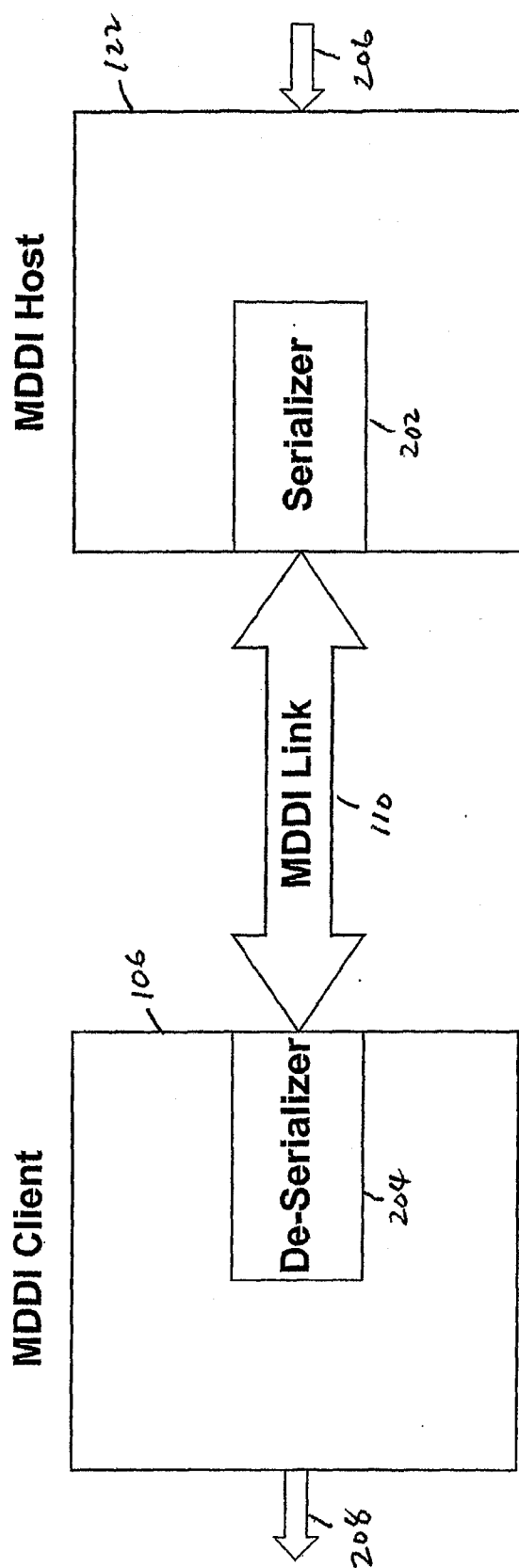


FIG. 2

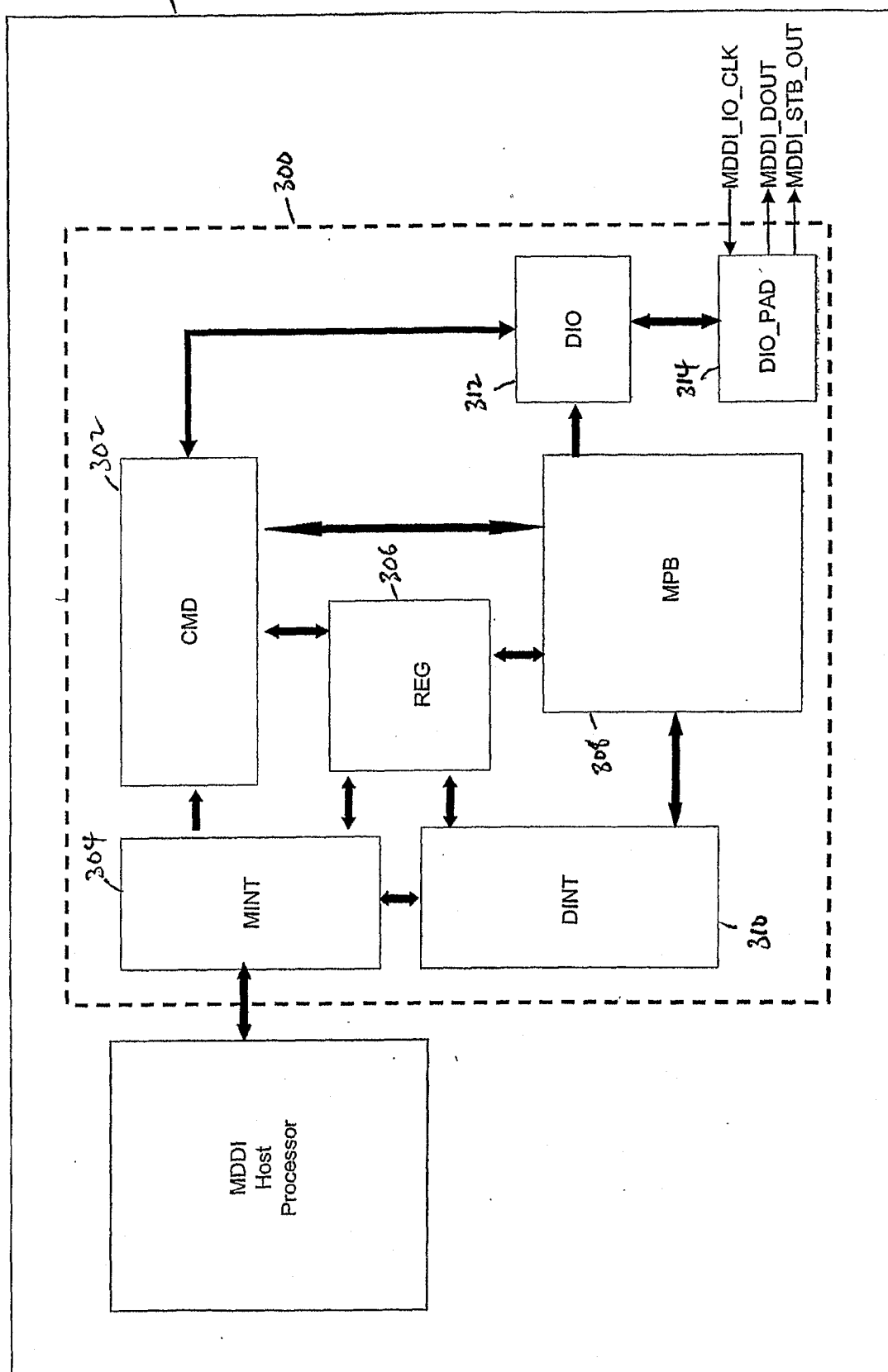


FIG. 3

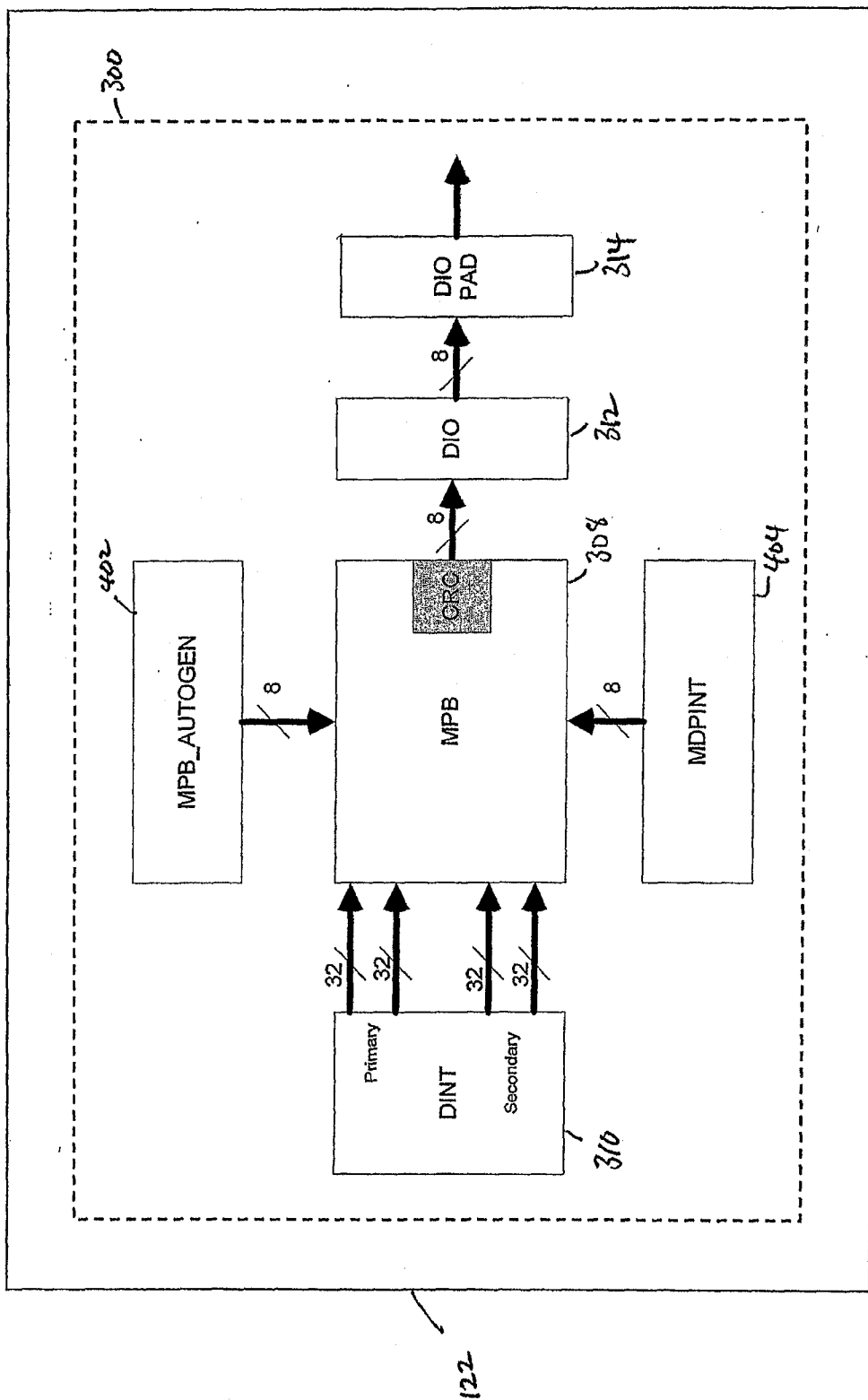


FIG. 4

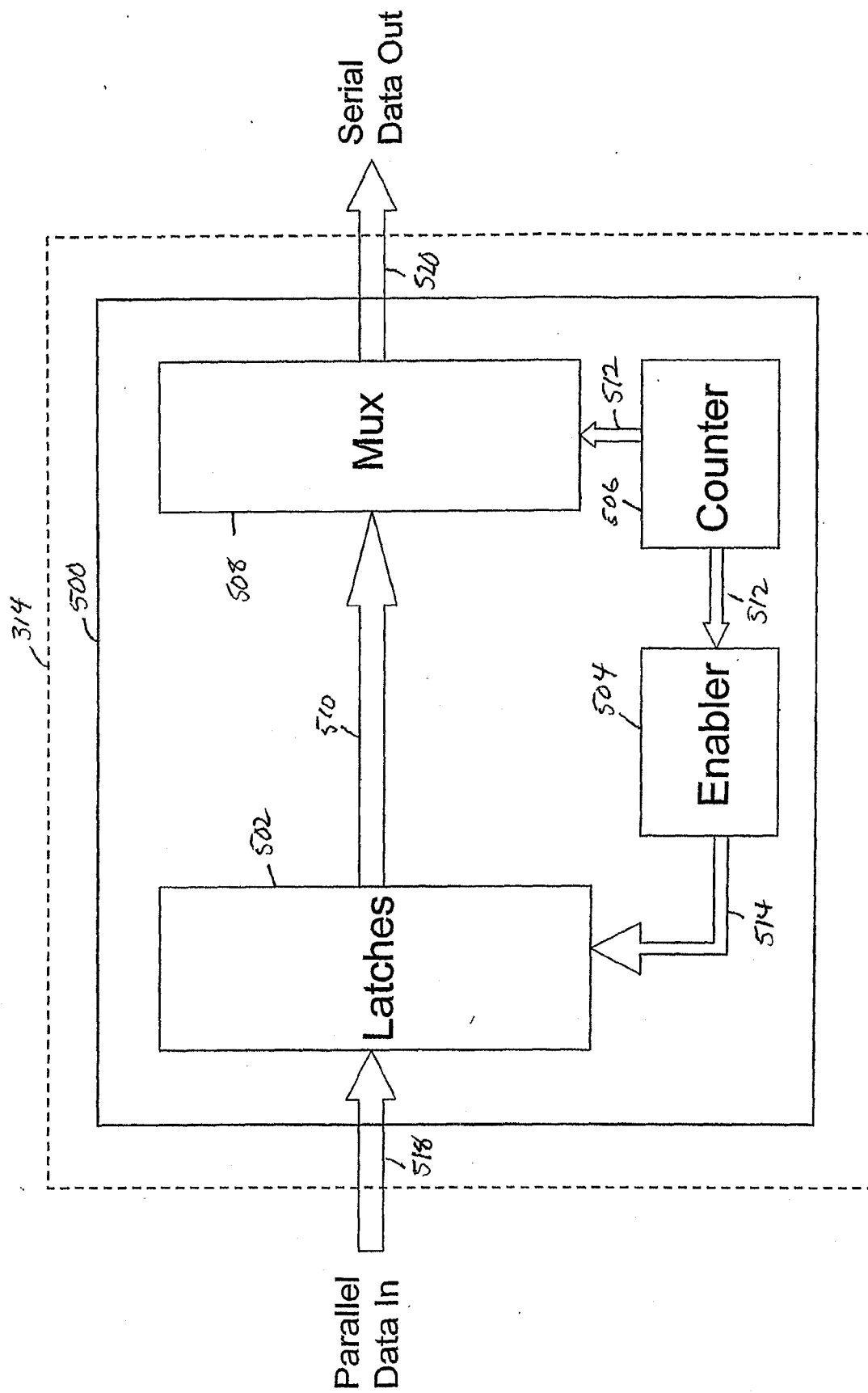


FIG. 5

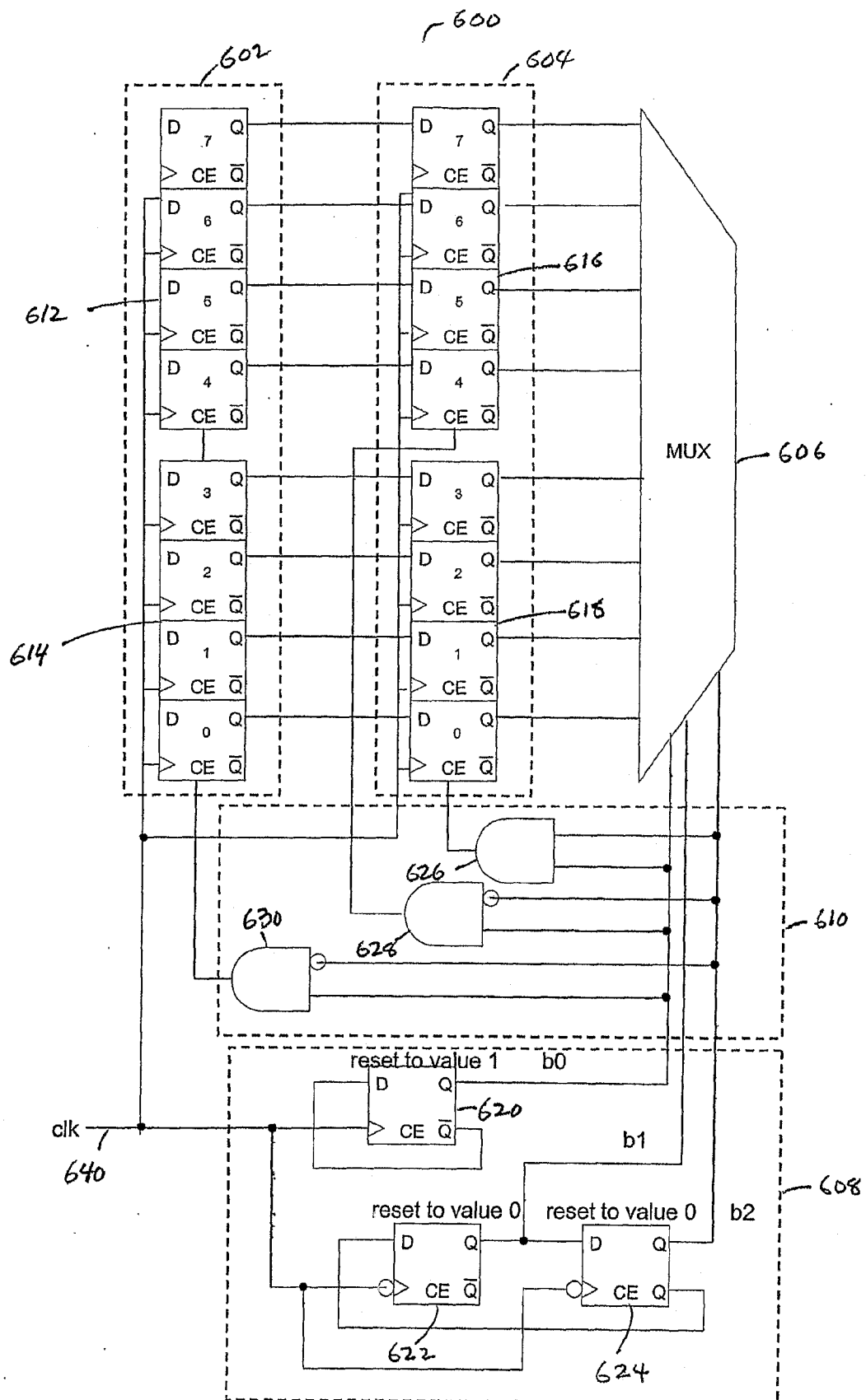


FIG. 6

Mux output for particular
counter input selection value

Input	$S_2 S_1 S_0$
D0	001
D1	011
D2	010
D3	110
D4	111
D5	101
D6	100
D7	000

FIG. 7

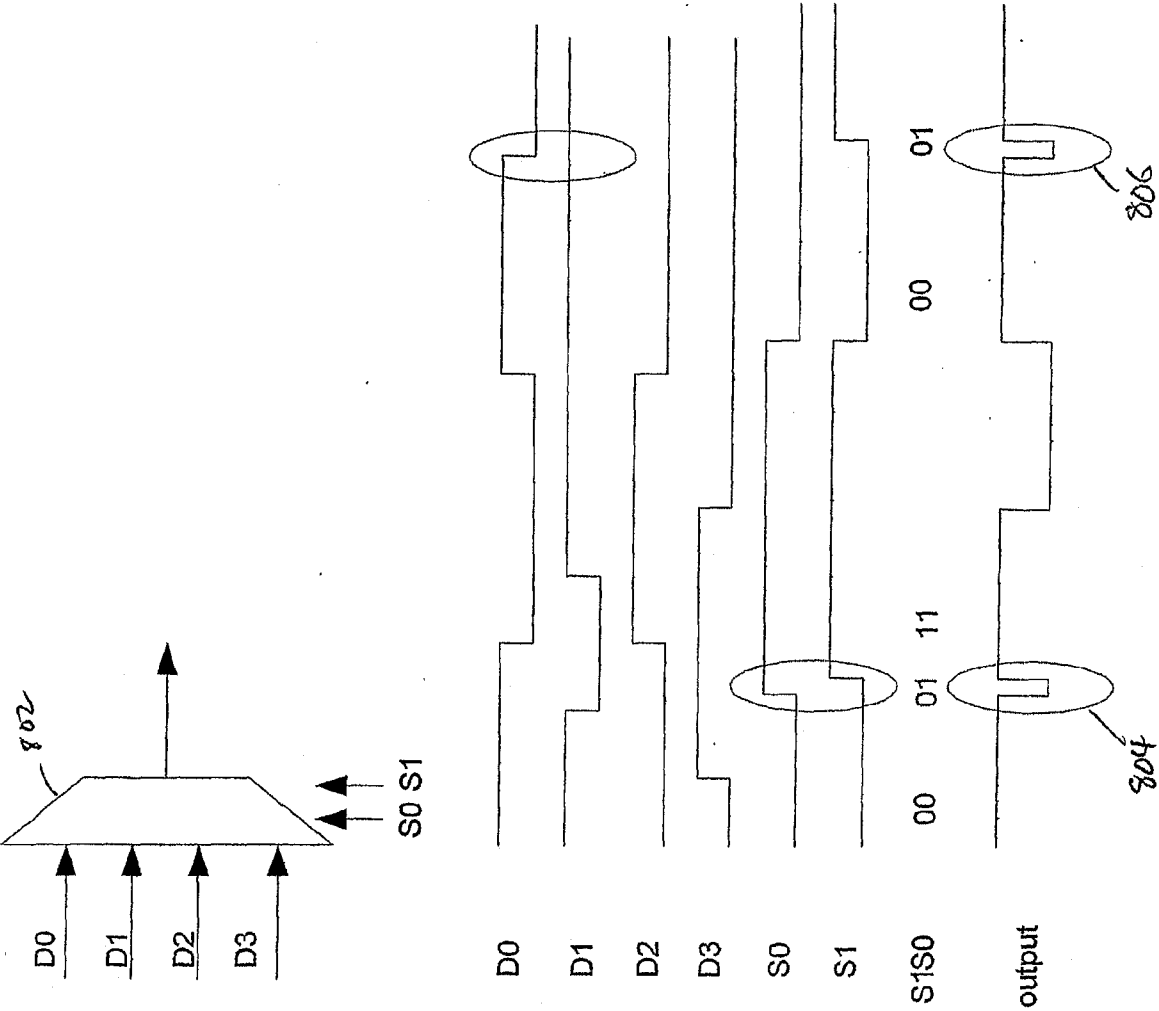


FIG. 8

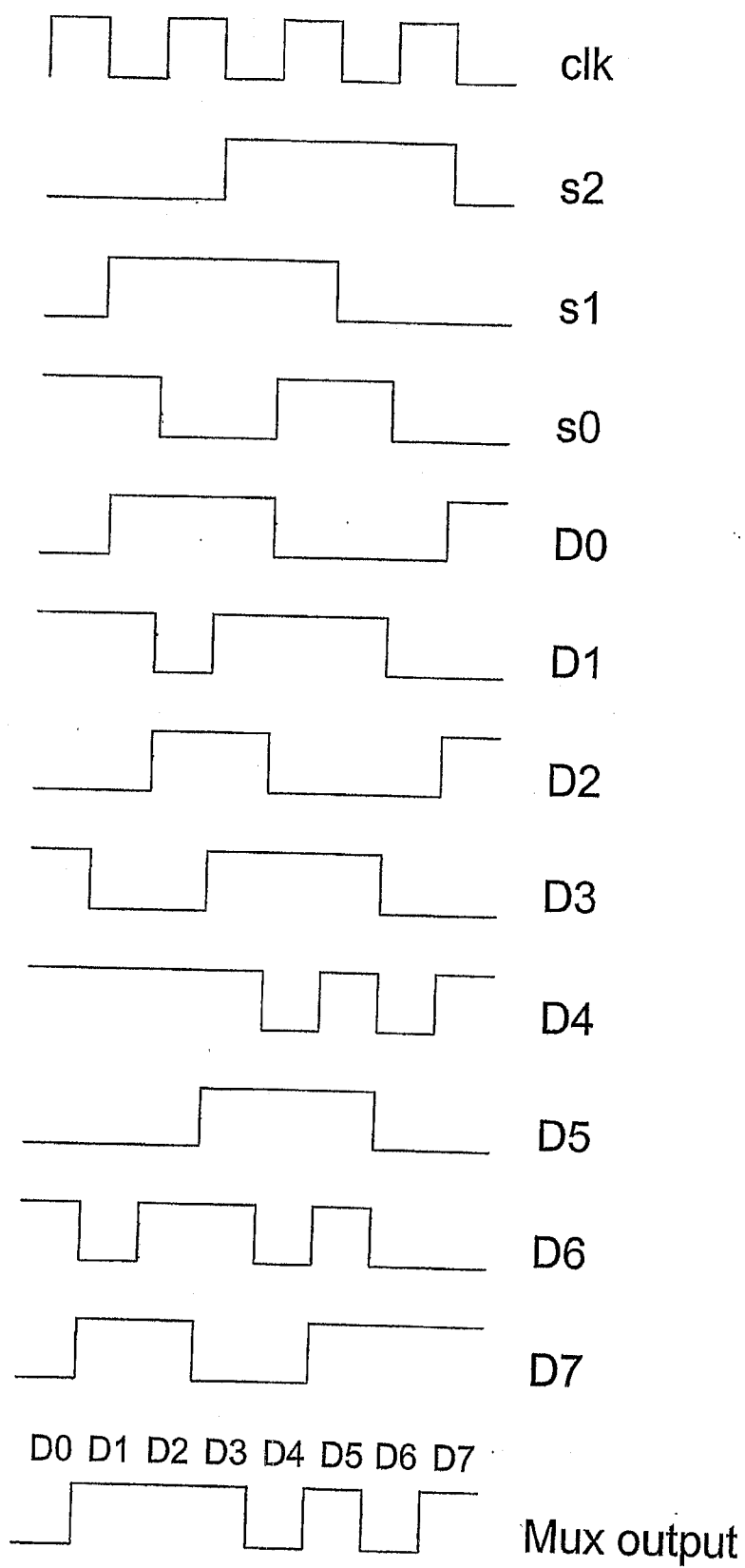


FIG. 9