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A MOS TRANSISTOR HAVING A COMPOSITE GATE ELECTRODE AND METHOD OF FABRICATION

BACKGROUND OF THE INVENTION

1. Field Of The Invention

The present invention relates to the filed of semiconductor devices, and more specifically, to a MOSFET with a composite gate electrode which is compatible with standard CMOS processing.

2 Description Of Related Art

Transistors are well-known in the art. Transistors are the building blocks of all integrated circuits. Modern integrated circuits interconnect literally millions of transistors together to perform a wide variety of functions. The performance and reliability of a specific integrated circuit is directly related to the performance and reliability of the transistors of which it is comprised. Thus, in order to provide better performing integrated circuits in the future, one needs to improve the electrical characteristics of transistors.

Figure 1 shows a cross-sectional view of a well-known lightly doped drain (LDD) metal oxide semiconductor (MOS) transistor 100. Transistor 100 has a standard polysilicon gate electrode 110. Transistor 100 has in the past been a very popular and widely used transistor because of its polysilicon gate electrode 110. An advantage of the polysilicon gate

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electrode is that it allows the transistor to be fabricated with well-known and extremely manufacturable standard CMOS processes. For example, the polysilicon gate allows a self-aligned source/drain process to be utilized since the polysilicon gate can adequately mask the channel region of the transistor from source/drain implants. A self-aligned process allows the source and drain of the transistor to always be perfectly aligned with the gate of the transistor regardless of mask alignment tolerances. Another advantage of polysilicon gate 100 is that a self-aligned silicide process can be used to form silicide 112 on the source, drain, and gate of the transistor. Transistor 100 is compatible with the self-aligned silicide process because polysilicon gate 110 is not vulnerable to the etch used to remove unreacted metal, which is required in the metallic silicide process.

Unfortunately, however, the performance of the standard polysilicon gate transistor 100 is poor due to polysilicon depletion effects. Polysilicon depletion effects reduce the amount of gate voltage applied across the gate oxide. This in turn reduces the drive current of the transistor. Since speed is directly proportional to the drive current, the speed performance of the standard polysilicon gate transistor is poor. The speed performance of the standard polysilicon gate transistor 100 is poor due to polysilicon depletion effects.

Figure 2 is a cross-sectional view of another well-known transistor 200. Transistor 200 has a metal gate electrode 210. Metal gate electrodes are beneficial because their electrical characteristics are superior to doped polysilicon gate electrodes. Unfortunately, however,

such metal gates are incompatible with modern CMOS processing techniques. For example, a self-aligned source/drain implant can not be used in metal gate devices because metal gates can not adequately mask the channel region from impurity doping during the implant. Additionally, metal gate electrodes are incompatible with self-aligned silicide processes because they can be damaged by the etch, which is required to remove the unreacted metal, in the silicide process.

Thus, what is desired is a high performance semiconductor transistor which does not exhibit polysilicon depletion effects and which is compatible with a standard CMOS fabrication process.

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SUMMARY OF THE INVENTION

A novel, high performance, highly reliable LDD MOSFET transistor having a composite gate electrode which does not suffer from polysilicon depletion effects and which is compatible with standard CMOS processing is described. The LDD MOSFET has a composite gate comprising a polysilicon layer formed on a conductive layer. The conductive layer may be formed from TiN, W, Mo, polycrystalline carbon or any metallic silicide with the appropriate work function. The polysilicon layer and the conductive layer of the composite gate electrode have exactly the same length and width. The composite gate is formed on a substrate of a first conductivity type with a gate insulating layer formed between them. A pair of lightly doped drain regions of a second conductivity type are formed in the substrate and in alignment with laterally opposite sidewalls of the composite gate electrode. A pair of silicon nitride or oxide spacers are formed adjacent to laterally opposite sides of the composite gate. The spacers and the polysilicon layer completely encapsulate the conductive layer of the composite gate electrode. A pair of source/drain regions of a second concentration of the second conductivity type are formed in the substrate in alignment with the outside edges of the silicon nitride spacers. Silicide is formed on the source/drain region and on the polysilicon layer of the composite gate.

A goal of the present invention is to provide a high performance, reliable MOS transistor which can be manufactured with a standard CMOS process.

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Another goal of the present invention is to provide a MOS transistor which does not exhibit polysilicon depletion effects.

Yet another goal of the present invention is to provide a high performance transistor which is compatible with a standard self-aligned source/drain implant and a standard self-aligned silicide process.

Still yet another goal of the present invention is to provide an MOS transistor which is extremely stable under high temperature and bias stress conditions.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a cross-sectional illustration of an LDD MOS transistor with a standard polysilicon gate electrode.

Figure 2 is a cross-sectional illustration of a MOS transistor with a metal gate electrode.

Figure 3 is a cross-sectional illustration of an LDD MOSFET with a composite gate electrode.

Figure 4a is a cross-sectional illustration of a silicon substrate having an oxide layer, a conductive layer, a polysilicon layer, and a photoresist layer formed thereon.

Figure 4b is a cross-sectional illustration of the formation of a composite gate electrode on the substrate of Figure 4a.

Figure 4c is a cross-sectional illustration of the formation of a pair of LDD regions in the substrate of Figure 4b.

Figure 4d is a cross-sectional illustration of the formation of a conformal silicon nitride or oxide layer over the substrate of Figure 4c.

Figure 4e is a cross-sectional illustration of the formation of a pair of spacers and the formation of a pair of source/drain regions in the substrate of Figure 4d.

Figure 4f is a cross-sectional illustration of the formation of a metal layer over the substrate of Figure 4e.

Figure 4g is a cross-sectional illustration of the formation of silicide regions on the source/drain regions and on the polysilicon layer on the substrate of Figure 4f.

DETAILED DESCRIPTION OF THE PRESENT INVENTION

The present invention discloses a novel, high performance, highly reliable metal oxide semiconductor (MOS) transistor with a composite gate electrode which is compatible with standard CMOS processing. In the following description numerous specific details such as doping doses, doping types, manufacturing methods etc. are set forth in order to provide a thorough understanding of the present invention. It will be obvious, however, to one skilled in the art that the present invention may be practiced without these specific details. In other instances well-known metal oxide semiconductor transistor concepts and fabrication techniques have not been set forth in detail in order to not unnecessarily obscure the present invention.

The preferred embodiment of the novel MOS transistor with a composite gate electrode of the present invention is shown Figure 3. The composite gate electrode is used to form a high performance, lightly doped drain (LDD) metal oxide semiconductor (MOS) transistor 300. The novel composite gate electrode significantly improves the formed transistor's electrical performance and reliability. Additionally, the method of forming the novel gate electrode is completely compatible with present well-known CMOS processing technologies.

The composite gate electrode comprises a polysilicon layer 302 formed on a thin, highly conductive layer 304. Silicide 306 can also be formed on the top surface of polysilicon layer 302 in order to reduce the

gate contact resistance of transistor 300. In one embodiment an n-channel transistor 300 is formed in a P doped silicon substrate 308. An oxide layer 301 provides the gate insulator for transistor 300. Lightly doped drain (LDD) regions 310a and 310b of N- conductivity are formed in alignment with the outside edges of the composite gate electrode. Spacers 312a and 312b are formed adjacent to the outside edges of the composite gate electrode. Source/drain regions 314a and 314b are formed in alignment with the outside edges of spacers 312a and 312b. Silicide 316a and 316b can be formed on source/drain regions 314a and 314b.

The thin conductive layer 304 significantly improves the electrical characteristics of transistor 300 over transistors having a standard polysilicon gate. Conductive layer 304 completely eliminates the polysilicon depletion effects associated with standard polysilicon gate devices. By eliminating the poly-depletion effects, the drive capability of transistor 300 is increased by 10%-20% over standard polysilicon gate devices. Since drive capability is directly proportional to device speed, the speed performance of transistor 300 is improved over standard polysilicon gate devices.

Additionally, transistor 300 exhibits other performance improvements over the standard polysilicon gate transistors due to its composite gate. The gate oxide tunneling current of transistor 300 is at least one order of magnitude lower than standard polysilicon gate devices for the same electric field. The gate oxide break-down field of transistor 300 is also about 10% higher than that of standard polysilicon gate devices.

Transistor 300 also exhibits minimal charge trapping after bias/temperature stress. Additionally, it is to be noted that there is very little interaction between the gate oxide 301 and the conductive layer 308. These characteristics makes transistor 300 a very stable, reliable and excellent performing transistor.

In fabrication of the invented MOS semiconductor transistor with the presently preferred process, a p-type silicon substrate 500 shown in Figure 4 is used. The p-type substrate 500 is doped with an approximately 10^{13} cm^{-2} dose of Boron atoms. Next, a 20-200Å oxide layer 502 is grown on substrate 500. The oxide layer 502 will provide the gate insulator for the transistor. Oxide layer 502 can be grown in a diffusion furnace at approximately 920°C at atmosphere in 91% 0_2 and 9% TCA.

Next, a 20-2000Å conductive layer 504 is formed over the oxide layer 502. A variety of different materials can be used for conductive layer 504. The material chosen must be able to withstand high temperature (i.e., greater than 850°C) processing. It must be highly conductive (i.e., have a higher conductivity than n+ polysilicon). It is preferred to have a work function close to the mid-gap of silicon, and ideally at the mid-gap of silicon for CMOS applications. Finally, it should be able to be formed uniformly across a wafer and consistently from wafer to wafer. The following materials have been found to meet the necessary physical and electrical requirements of conductive layer 504: Titanium- Nitride (TiN), Tungsten (W), polycrystalline carbon (C), and just about any metallic silicide with the appropriate work function. The preferred embodiment of

the present invention utilizes an approximately 500Å titanium nitride conductive layer 504. If the present invention is used to optimize only NMOS or PMOS transistor's performance, the mid-gap work function may not be required, and many metals which can resist high temperatures will work.

If titanium nitride is used it is formed with a reactive sputter process. Titanium nitride is formed by sputtering titanium from a titanium target in a nitrogen and argon ambient. The percentage of N_2 can be from 100%-30% with the remainder argon. The presently preferred embodiment forms a nitrogen rich titanium nitride layer by using a 70% N^2-30% Argon ambient. The titanium nitride is sputtered in a DC magnetron deposition chamber at a pressure of approximately four mtorr and a power of approximately three kilowatts. If tungsten is used it can be sputtered from a tungsten target at room temperature in an Argon ambient with a power of approximately 1.5-2 kilowatts and a pressure of approximately 30-50 mtorr. If polycrystalline carbon is utilized, it can be formed by CVD deposition in a downstream RF plasma reactor with 5% CH_4 and < 0.1% BCL_3 by volume, with the remainder argon. Polycrystalline carbon is formed at a temperature of approximately 750°C and at a pressure of approximately 1.5 torrs.

After formation of the conductive layer 504, a polycrystalline silicon (polysilicon) layer 506 is formed. The polysilicon layer 506 is formed by LPCVD in SiH_4 at a pressure of 130-190 mtorr and at a temperature of approximately 620°C. In the preferred embodiment of the present invention the polysilicon layer 506 is formed to a thickness of

approximately 3500Å. A photoresist layer 508 is then formed over the polysilicon layer 506.

Next, as shown in Figure 4b, a gate electrode 513 is formed from the polysilicon layer 506 and the conductive layer 504. First the photoresist layer 508 is masked, exposed, and developed with well known techniques to define the location 511 where the gate electrode 513 is to be formed. Next, the polysilicon layer is anistropically etched in a reactive ion etcher with a HBr, Cl_2, He chemistry to form the top portion 512 of the composite gate electrode 513. If titanium nitride is used as conductive layer 504, it is etched in-situ with the polysilicon layer and with the same chemistry as a polysilicon layer to form the lower gate electrode 510. Titanium nitride and most metallic silicides are preferred as conductive layer 504 because a single etch step can be utilized to form the composite gate electrode 513. The gate electrode is etched in-situ until the oxide layer 502 is reached. (It is to be appreciated that some of the exposed oxide layer 502 will be etched away.) The completion of the gate electrode etch can be endpoint detected by analyzing the residual gas exhausted during the etch.

If tungsten is utilized as the conductive layer 504 it is plasma etched (after the polysilicon etch) in a two step process. First it is etched in NF3 and argon and then followed by a second plasma etch in $SF_6/Cl_2/He$. If polycrystalline carbon is utilized, it is also plasma etched (after the polysilicon etch). It is to be appreciated that after the composite gate electrode patterning, conductive layer 510 and polysilicon layer 512 have exactly the same length and width. After the composite gate

electrode has been fully defined, photoresist 511 is removed with well-known techniques.

As shown in Figure 4c, after the formation of the composite gate electrode 513 a pair a n- lightly doped drain (LDD) regions 514a and 514b are formed. The LDD regions 514a and 514b are formed with a standard CMOS self-aligned process. The lightly doped drain regions 514a and 514b are formed by implanting phosphorus atoms at a dose of approximately $1X10^{14}$ cm^{-2} at an energy of approximately 40 KEV. The exposed oxide layer 502 prevents the surface of substrate 500 from being damaged by the implant. The lightly doped drain regions 514a and 514b are formed in alignment with opposite sidewalls running along the width of the gate electrode 513. The polysilicon layer 512 acts as a mask for the LDD implant. In this way the LDD regions 514a and 514b are self aligned to the gate electrode 513 regardless of mask alignment tolerances. It is to be appreciated that such a self-aligned process is not possible with fully metal gates because they cannot sufficiently mask the channel region from the implant. It is also to be appreciated that at this time the polysilicon layer 512 becomes doped with phosphorous atoms.

Next, as shown in Figure 4d, an approximately 2500Å very conformal layer of silicon nitride 516 is deposited over the entire substrate. The silicon nitride layer 516 is formed by LPCVD with SIH_2 Cl_2 and NH_3 at approximately 800°C in a hot wall reaction chamber. Such a process forms a very conformal silicon nitride layer. A very thin (approximately 200Å) oxide layer may be grown before the silicon nitride layer to provide the silicon nitride layer 516 with a good starting surface. Although a

silicon nitride layer is preferred, it is to be appreciated that a CVD oxide layer can be utilized in place of the silicon nitride layer 516.

Next, as shown in Figure 4e, the silicon nitride layer 516 is anisotropically etched to form sidewall spacers 518a and 518b on each side of gate electrode 513. A conformal layer 516 is required in order to form spacers which have a uniform and precisely controlled thickness across a wafer. The silicon nitride layer is anisotropically etched by plasma ion etching with CF_3/O_2. It is to be noted that now conductive layer 510 is completely protected and encapsulated by spacers 518a and 518b and polysilicon layer 512. This is extremely important because later process steps, such as in the planerization of interlevel dielectrics, utilize steam processes which can seriously corrode exposed metal layers.

After formation of spacers 518a and 518b, N+ source/drain regions 520a and 520b are formed. The N+ source/drain regions are formed by ion implanting arsenic atoms at a dose of approximately $6x10^{15}$ cm^{-2} at an energy of approximately 100 kev. The spacers 518a and 518b and the polysilicon layer 512 prevent the channel region from becoming N+ doped. The source/drain regions 520a and 520b are formed in alignment with the outside edges of sidewall spacers 518a and 518b. The polysilicon layer 512 becomes N+ doped with arsenic atoms. Again, oxide layer 502 protects the surface of the silicon substrate 500 from becoming damaged during the arsenic implant.

Next, the substrate 500 is annealed in an N_2 ambient at 900°C for approximately 10 minutes in a standard furnace. The anneal activates

the phosphorus and arsenic atoms from the LDD and source/drain implants. It is because of this high temperature anneal that the conductive layer 510 must be able to withstand high temperature processing. After the anneal, the exposed oxide 502 over the source/drain regions is removed by an HF dip.

Silicide can now be formed on the polysilicon layer 512 and on the N+ source/drain regions 520a and 520b. Silicide can dramatically improve the performance of the fabricated transistor. Silicide is formed in the present invention with a well-known self-aligned processes. First, as shown in Figure 4f, a thin metal layer 522 such as titanium or tungsten is formed over the entire device structure. Next, the metal layer 522 is heated or annealed which causes a silicide reaction to occur wherever the metal is in contact with reactive silicon (i.e., on the source/drain regions 520a and 520b and on the polysilicon layer 512), everywhere else (i.e., over the spacers and field oxides) the metal remains unreacted. Next, the unreacted metal is selectively removed with the use of an etchant which does not attack the silicide. As such, as shown in Figure 4g, silicide 524 is formed on the gate, source, and drain of the fabricated transistor. During the silicide formation, the conductive layer 510 is well sealed by spacers 518a and 518b and the polysilicon layer 512.

It is to be appreciated that the LDD MOSFET with a composite gate electrode of the present invention is now complete. At this time other well-known process steps are used to complete the fabrication of the MOSFET. An interlayer dielectric is deposited to separate the gate from

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the metal layer to follow. This process generally employs a steam flow process for planerization which can damage conductive layer 510 if it is not fully protected. Metal contacts are fabricated next to electrically couple the device to other elements in the circuit. A protective glass or passivation is formed over the device to protect the device from contamination or electrical short.

It is to be appreciated that although the present invention has been described with respect to an LDD MOSFET, aspects of the present invention are equally applicable to standard transistors without LDD regions. It is also to be appreciated that although n-channel transistors have been described in detail herein, the present invention may also be practiced as a p channel transistor. In fabricating a p-channel device, the doping conductivity's of the p channel device are simply opposite to those of the n channel device. The device is formed in an n-type substrate or well with p- LDD regions and p+ source/drain regions formed respectively therein. The gate electrode would still be a composite gate comprising a polysilicon layer formed on a conductive layer in order to eliminate polysilicon depletion effects. Spacers would also be utilized for source/drain alignment and silicide processes. It is also to be appreciated that the composite gate electrode is useful in both long channel and submicron channel transistors.

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Thus, a novel LDD MOS transistor with a composite gate electrode and a standard CMOS compatible fabrication process has been described.

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IN THE CLAIMS

We claim:

1. A metal oxide semiconductor field effect transistor formed on a substrate of a first conductivity type comprising:

a gate insulating layer formed on said substrate;

a composite gate electrode comprising:

a conductive layer formed on said gate insulating layer;

a polysilicon layer formed on said conductive layer wherein said polysilicon layer and said conductive layer have approximately the same length and width; and

a pair of source/drain regions of a second conductivity type formed in said substrate in alignment with the outside edge of said composite gate electrode.

2. The metal oxide semiconductor transistor of claim 1 wherein said conductive layer is selected from the group consisting of: TiN, W, and polycrystalline carbon.

3. The metal oxide semiconductor transistor of claim 1 wherein said conductive layer is a metallic silicide.

4. A lightly doped drain metal oxide semiconductor transistor formed on a substrate of a first conductivity type comprising:

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a gate insulating layer formed on said substrate;

a composite gate electrode having laterally opposite sidewalls along the width of said composite gate electrode, said composite gate electrode comprising:

a conductive layer formed on said gate insulating layer;

a polysilicon layer formed on said conductive layer;

said polysilicon layer and said conductive layer having approximately the same length and width;

a pair of lightly doped drain regions of a first concentration of a second conductivity type formed in said substrate in alignment with said laterally opposite sidewalls of said composite gate electrode;

a pair of spacers formed adjacent to laterally opposite sidewalls of said composite gate electrode;

a pair of source/drain regions of a second concentration of said second conductivity type wherein said second concentration is greater than said first concentration, said source/drain regions formed in said substrate in alignment with the outside edges of said spacers.

5. The lightly doped drain metal oxide semiconductor transistor of claim 4 wherein said conductive layer is formed from the group consisting of TiN, W, and polycrystalline carbon.

6. The lightly doped drain metal oxide semiconductor transistor of claim 4 wherein said spacers are silicon nitride.

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7. The lightly doped drain metal oxide semiconductor transistor of claim 4 wherein said conductive layer has a thickness of approximately 500Å and said polysilicon layer has a thickness of approximately 3500Å.

8. The lightly doped drain metal oxide semiconductor transistor of claim 4 wherein said first conductivity type is p type conductivity, and said second conductivity type is n type conductivity.

9. The lightly doped drain metal oxide semiconductor transistor of claim 4 further comprising silicide formed on said polysilicon layer and on said source/drain regions.

10. The lightly doped drain metal oxide semiconductor transistor of claim 4 wherein said conductive layer is a metallic silicide.

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