RF ASIC FOR SUBSCRIBER COMMUNICATOR

RELATED APPLICATIONS

This PCT Application is based on and claims priority to US Patent Application 10/443,537 filed May 22, 2003. The drawings which form a part of this PCT application include additional embodiments not shown in drawings in 10/443,537. This application is a continuation in part of US Application 10/443,537.

BACKGROUND ART

[0001] The inventions described herein generally pertain to a subscriber communicator for use in satellite communications. They are particularly directed to improved implementations of and methods applicable to receiver and transmitter channels of a subscriber communicator. It is presently preferred that the arrangements and methods be implemented at least in part by an ASIC (Application Specific Integrated Circuit), but they could be practiced using other types of circuit implementations.

[0002] In a subscriber communicator, the receiver channel downconverts and demodulates a received RF (Radio Frequency) communication signal to provide received quadrature components at baseband and processes the quadrature components to respectively provide so-called "I" and "Q" digital data output signals. The transmitter channel processes I and Q digital data input signals to provide input quadrature modulation components; and upconverts and combines the quadrature modulation components to provide an RF communication transmit signal.

[0003] A known RF ASIC for a subscriber communicator comprises a receiver section that includes means for receiving an RF communication signal and means for directly downconverting and demodulating the received RF communication signal to provide analog quadrature components of the received signal at baseband. A transmitter section includes means for upconverting and combining analog input quadrature modulation components to provide an RF communication transmit signal and means for amplifying

the transmit signal for driving an external power amplifier. A synthesizer provides signals at selected frequencies for use in downconversion and upconversion.

DISCLOSURE OF INVENTION

[0004] The inventions described herein provide RF ASIC arrangements and methods of signal processing for a subscriber communicator. The ASIC includes a receiver section, including means for receiving an RF communication signal; and means for downconverting and demodulating the received RF communication signal to provide analog quadrature components of the received signal at baseband. A transmitter section includes means for upconverting and combining analog input quadrature modulation components to provide an RF communication transmit signal; and means for amplifying the transmit signal for driving an external power amplifier. A CODEC processes the analog baseband quadrature components of the received signal to provide I and Q digital output signals, and processes I and Q digital input signals to provide the analog input quadrature modulation components for up-conversion. Preferably, the RF ASIC further includes a single port for combining the I and Q digital output signals for output as a serial digital signal stream, and for separating the I and Q digital input signals from an input serial digital signal stream.

[0005] According to other aspects of the inventions, there is provided an RF ASIC for a subscriber communicator for use in satellite communications. The ASIC includes a receiver channel, including means for downconverting and demodulating a received RF satellite communication signal to provide received quadrature components at baseband; and means for processing the quadrature components of the received signal to respectively provide I and Q digital output signals. A transmitter channel includes means for processing I and Q digital input signals to provide input quadrature modulation components; and means for upconverting and combining the input quadrature modulation components to provide an RF communication transmit signal.

[0006] Additional features of the inventions are described with reference to the detailed description of the preferred embodiments.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] FIG. 1 is a block diagram of a preferred embodiment of the RF ASIC according to the inventions.

[0008] FIG. 2 is a block diagram of a first embodiment of a receiver channel the RF ASIC of FIG. 1.

[0009] FIG. 3 is a block diagram of a first embodiment of a transmitter channel of the RF ASIC of FIG. 1.

[0010] FIG. 4 is a block diagram of an alternative embodiment of a transmitter channel such as shown in FIG. 3.

[0011] FIG. 5 is a block diagram of an alternative embodiment of a receiver channel such as shown in FIG. 2.

DESCRIPTION OF THE BEST MODE

[0012] A preferred embodiment of the RF ASIC according to the inventions is adapted for inclusion in a subscriber communicator that is adapted for use in the ORBCOMM Satellite communication network even though the principles of the described inventions are applicable to other systems. The ORBCOMM network, as configured at the time of this writing, includes twenty-eight low-earth-orbit (LEO) communication satellites, gateway Earth stations, network control centers and a global network operations center in Dulles, Virginia. The ORBCOMM network provides wireless, two-way global satellite data communications between mobile subscriber communicators and operators via the Internet or dedicated leased lines for high-volume operations. ORBCOMM downlink signals are provided in a symmetrical differential phase-shift-keyed (SDPSK) format at 4800 bps in a receive frequency range of 137.0 to 138.0 MHz. ORBCOMM uplink signals are provided in a SDPSK format at 4800 bps in a transmit frequency range of 148.0.0 to 150.05 MHz.

[0013] FIG. 1 is a block diagram of a preferred embodiment of an RF ASIC 10 according to the inventions. RF ASIC 10 includes a receiver section 11, a transmitter

section 12, a stereo CODEC 14; an inter-IC sound (I^2S) port 15, a synthesizer 16, a serial peripheral interface (SPI) port 17, a power section 19 and a power control section 20. The receiver section 11 and transmitter section 12 operate in a half-duplex mode.

[0014] The receiver section 11 receives an RF communication signal RX-IN from an external receive/transmit antenna via an external RX/TX switch and an external bandpass filter, and downconverts and demodulates the received RF communication signal 22 to provide analog quadrature components 23I ,23Q of the received signal at baseband.

[0015] The transmitter section 12 upconverts and combines analog input quadrature modulation components 25I, 25Q to provide an RF communication transmit signal, and amplifies the transmit signal to provide an output transmit signal TX-OUT for driving an external power amplifier that is coupled to the antenna via an external low-pass filter and the external RX/TX switch.

[0016] The various components referred to throughout this description as being "external" typically are included in the subscriber communicator that includes an RF ASIC.

[0017] The CODEC 14 processes the analog baseband quadrature components 23I, 23Q of the received signal to provide I and Q digital output signals 28I, 28Q, and also processes I and Q digital input signals 29I, 29Q to provide the analog input quadrature modulation components 25I, 25Q that are upconverted by the transmitter section 12.

[0018] The I^2S port 15 combines the I and Q digital output signals 28I, 28Q for output as a serial digital signal stream SD-RX, and separates the I and Q digital input signals 29I, 29Q from an input serial digital signal stream SD-TX.

[0019] The synthesizer 16 provides signals at selected frequencies for use in the signal downconversion provided by the receiver section 11 and in the signal upconversion provided by the transmitter section 12. The SPI port 17 is coupled to the synthesizer 16 for programming the synthesizer 16 to synthesize signals at the selected frequencies.

[0020] The power section 19 distributes power to the receiver section 11, the transmitter section 12, the CODEC 14 and the synthesizer 16 (power connections not shown in the drawing). Preferably the power is supplied by a replaceable battery received by the power section 19. The power control section 20 controls the power distribution to the receiver section 11 in accordance with an externally provided PM-RX control signal; controls the power distribution to the transmitter section 12 in accordance with an externally provided

PM-TX control signal; and controls the power distribution to the receiver section 11 in accordance with an externally provided PM-SYNTH control signal.

[0021] The ASIC 10 is connected to an external digital signal processor (DSP) within the signal communicator. The DSP provides the PM-RX control signal, the PM-TX control signal and the PM-SYNTH control signal to the power control section 20.

[0022] The DSP is also connected to the I^2S port 15 for receiving the output serial digital signal stream SD-RX from the I^2S port 15 and for providing the input serial digital signal stream SD-TX to the I^2S port 15 in accordance with a word strobe signal WS and a serial clock signal SCLK that are also provided by DSP is to the I^2S port 15.

[0023] The DSP is connected to the synthesizer 16 via the SPI port 17 for providing a synthesizer programming data signal MOSI in accordance with a strobe signal SS and a programming clock signal PCLK that are also provided by the DSP to the SPI port 17. A confirming data-back signal MISO is provided by the SPI port 17 to the DSP.

[0024] The synthesizer 16 receives timing signals XTAL1 and XTAL2 from external quartz crystals and provides a reference clock signal REF-CLK to the DSP. The synthesizer 16 also provides a lock detect signal LOCK DET to the DSP when the synthesizer becomes locked to a frequency indicated by the synthesizer programming data signal MOSI.

[0025] FIG. 2 is a block diagram of a preferred embodiment of a receiver channel implemented in the receiver section 11 and the CODEC 14 of the RF ASIC 10 shown in FIG. 1. The receiver section 11 includes a low-noise amplifier (LNA) 33, a first mixer 34, a first port 35, a second port 36, a digital-controlled variable gain amplifier 37, an I-channel mixer 39, a Q-channel mixer 40, a 90-degree phase shifter, 41, an I-channel low-pass filter (LPF) 42, Q-channel low-pass filter 44 an I-channel baseband amplifier (BBA) 45 and a Q-channel baseband amplifier 46.

[0026] A local oscillator signal at an intermediate frequency IF is provided to the first mixer 34 by the synthesizer 16. Local oscillator signals at the baseband frequency BBF are provided to each of the I-channel mixer 39 and the Q-channel mixer 40 by the synthesizer 16.

[0027] The receiver section 11 thereby provides a superhetrodyne receiver for downconverting the received signal; wherein the received signal is first downconverted by the first mixer 34 to the intermediate frequency IF and, after being fed from the first port

35 through an external narrow-band IF filter 48 and back onto the ASIC 10 via the second port, 36, is then downconverted from the intermediate frequency by the I-channel mixer 39 and a Q-channel mixer 40, filtered by the respective I and Q-channel low-pass filters 42, 44 and amplified by the respective I and Q-channel bandpass amplifiers 45, 46 to provide the analog quadrature components 23I, 23Q of the received signal at baseband. The external IF filter 48 is a ceramic filter. Such an external IF filter is preferred because it is more economical than if the IF filter were to be implemented in the ASIC 10.

[0028] In an alternative embodiment (not shown) downconversion to baseband is direct.

[0029] The CODEC 14 includes an I-channel anti-alias low-pass filter (AAF) 49, a Q-channel anti-alias low-pass filter 50, an I-channel analog-to-digital converter (A/D) 51, a Q-channel analog-to-digital converter 52, an I-channel digital decimation filter 54 and a Q-channel digital decimation filter 55. Preferably, the I and Q-channel analog-to-digital converters 51, 52 are switched-capacitor and sigma-delta-modulated.

[0030] The analog baseband quadrature components 23I, 23Q of the received signal are processed by the respective I and Q-channel low-pass filters 49, 50, analog-to-digital converters 51, 52 and decimation filters 54, 55 to provide the I and Q digital output signals 28I, 28Q to the I^2S port 15.

[0031] FIG. 3 is a block diagram of a preferred embodiment of a transmitter channel implemented in the transmitter section 12 and the CODEC 14 of the RF ASIC 10 shown in FIG. 1. The CODEC 14 includes an I-channel interpolation filter 57, a Q-channel interpolation filter 58, an I-channel digital-to-analog converter (DAC) 59, a Q-channel DAC 60, an I-channel low-pass filter 61 and a Q-channel low-pass filter 62. Preferably, the I and Q-channel DACs 59, 60 are sigma-delta modulated; and the I and Q-channel low-pass filters 61, 62 are CT switched-capacitor filters which precisely control the baseband frequency by digital clocking.

[0032] The I and Q digital input signals 29I, 29Q are processed by the respective I and Q-channel interpolation filters 57, 58, DACs 59, 60 and low-pass filters 61, 62 to provide the analog input quadrature modulation components 25I, 25Q.

[0033] The transmitter section 12 includes an I-channel anti-alias low-pass filter 64, a Q-channel anti-alias low-pass filter 65, an I-channel baseband amplifier 66, a Q-channel baseband amplifier 67, an I-channel mixer 68, a Q-channel mixer 69, a 90-degree phase shifter 70, and an adder 71. Local oscillator signals at the transmit frequency TF are

provided to each of the I-channel mixer 68 and the Q-channel mixer 69 by the synthesizer 16.

[0034] The analog input quadrature modulation components 25I, 25Q are respectively filtered by the I and Q-channel low-pass filters 64, 65, amplified by the I and Q-channel baseband amplifiers 66, 67, upconverted by the I and Q-channel mixers 68, 69 and combined by the adder 71 to provide an RF communication transmit signal 74, to provide the output transmit signal TX-OUT that drives the external power amplifier.

[0035] FIG. 4 is a block diagram of an alternative embodiment of a transmitter channel. The difference between this embodiment and the one shown in Figure 3 is that this one utilizes a time multiplexed interpolator. In this embodiment, the I^2S port 15 provides its signals to interpolation unit 82. The output of interpolation unit 82 is demultiplexed by demultiplexer 80 which provides inputs to DAC 59 and DAC 60.

[0036] FIG. 5 is a block diagram of an alternative embodiment of a receiver channel. The difference between this embodiment and the one shown in Figure 2 is that this one utilizes a time multiplexed decimator. In this embodiment, the outputs of A/D 51 and 52 are coupled to the inputs of a multiplexer 82. The output of multiplexer 82 is coupled to the input of a single decimation filter 84, the output of which is provided to I^2S port 15.

[0037] The benefits specifically stated herein do not necessarily apply to every conceivable embodiment of the present invention. Further, such stated benefits of the present invention are only examples and should not be construed as the only benefits of the present invention. While the above description contains many specificities, these should not be construed as limitations on the scope of the present invention, but rather as examples of the preferred embodiments described herein. Other variations are possible and the scope of the present invention should be determined not by the embodiments described herein but rather by the claims and their legal equivalents.

Claims

1. An RF ASIC for a subscriber communicator, comprising:

a receiver section, including;

means for receiving an RF communication signal; and

means for downconverting and demodulating the received RF communication signal to provide analog quadrature components of the received signal at baseband;

a transmitter section, including:

means for upconverting and combining analog input quadrature modulation components to provide an RF communication transmit signal; and

means for amplifying the transmit signal for driving an external power amplifier; and

a CODEC for processing the analog baseband quadrature components of the received signal to provide I and Q digital output signals, and for processing I and Q digital input signals to provide the analog input quadrature modulation components for said upconversion, the codec including an analog to digital converter and a decimation filter arranged to receive signals from the analog to digital converter for processing received signals, the codec also including an interpolator and a digital to analog converter arranged to receive signals from the interpolator for processing signals to be transmitted.

2. An RF ASIC according to Claim 1, further comprising:

a signal port for combining the I and Q digital output signals for output as a serial digital signal stream, and for separating the I and Q digital input signals from an input serial digital signal stream.

3. An RF ASIC according to Claim 1, wherein the receiver section includes superheterodyne means for downconverting the received signal.

4. An RF ASIC according to Claim 3, wherein within the superheterodyne means, an output of a first downconverting section at an intermediate frequency is provided to a first port and an input from a second port is provided to a second downconverting section for downconversion from the intermediate frequency.

5. An RF ASIC according to Claim 1, further comprising:

low-pass filtering means between the receiver section and the CODEC.

6. An RF ASIC according to Claim 5, further comprising:

low-pass filtering means between the CODEC and the transmitter section.

7. An RF ASIC according to Claim 1, further comprising:

low-pass filtering means between CODEC and the transmitter section.

8. An RF ASIC according to Claim 1, further comprising:

a synthesizer for providing signals at selected frequencies for use in said downconversion and upconversion.

9. An RF ASIC according to Claim1, wherein the receiving means include a low-noise amplifier.

10. An RF ASIC for a subscriber communicator for use in satellite communications, comprising:

a receiver channel including:

means for downconverting and demodulating a received RF satellite communication signal to provide received quadrature components at baseband; and

means for processing the quadrature components of the received signal to respectively provide I and Q digital output signals the processing means including a codec having an analog to digital converter and a decimation filter arranged to receive signals from the analog to digital converter for processing received signals; and

a transmitter channel, including:

means for processing I and Q digital input signals to provide input quadrature modulation components the processing means including a codec having an interpolator and a digital to analog converter arranged to receive signals from the interpolator for processing signals to be transmitted; and

means for upconverting and combining the input quadrature modulation components to provide an RF communication transmit signal.

11. An RF ASIC according to Claim 10, further comprising:

a single port for combining the I and Q digital output signals for output as a serial digital signal stream, and for separating the I and Q digital input signals from an input serial digital signal stream.

12. An RF ASIC according to Claim 10, further comprising:

a port for combining the I and Q digital output signals for output as a serial digital signal stream.

13. An RF ASIC according to Claim 10, further comprising:

a port for separating the I and Q digital input signals from an input serial digital signal stream.

14. An RF ASIC according to Claim 10, wherein the receiver channel includes superheterodyne means for downconverting the received signal.

15. An RF ASIC according to Claim 14, wherein within the superheterodyne means, an output of a first downconverting section at an intermediate frequency is provided to a first port and an input from a second port is provided to a second downconverting section for downconversion from the intermediate frequency.

16. An RF ASIC according to Claim 10, wherein the receiver channel includes:

low-pass filtering means between the downconverting and demodulating means and the processing means.

17. An RF ASIC according to Claim 16, wherein the transmitter channel includes:

low-pass filtering means between the processing means and the upconverting and combining means.

18. An RF ASIC according to Claim 10, wherein the transmitter channel includes:

low-pass filtering means between the processing means and the upconverting and combining means.

19. An RF ASIC according to Claim 10, further comprising:

means for synthesizing signals at selected frequencies for use in said downconversion and upconversion.

20. An RF ASIC according to Claim 10, wherein the receiver section includes:

means for low-noise amplifying of the received signal prior to said downconversion.

21. An RF ASIC comprising:

a receiver constructed and arranged to receive an input signal;

a receiver codec for decoding quadrature signals from the receiver;

a transmitter codec for coding quadrature signals to be tranmitted;

a transmitter constructed and arranged to receive signals from the transmitter codec and transmit them;

an I^2S port constructed and arranged to receive signals from the receiver codec and provide signals to the transmitter codec;

a synthesizer constructed and arranged to synthesize integration signals required to integrate the ASIC with a digital signal processor; and

an SPI Port coupled to the synthesizer for programming the synthesizer to synthesize the integration signals.

22. An RF ASIC according to claim 21 further including:

a digital signal processor coupled to the I^2S port for receiving an output serial digital signal stream of received signals from the I^2S port and providing an input serial digital signal stream of signals to be transmitted to the I^2S port.