

**ADVANCED INTER-LEVEL DIELECTRIC (ILD) LAYER FOR SILICON ULTRA-LARGE SCALE
INTEGRATED (ULSI) CIRCUITS**

ABSTRACT OF THE DISCLOSURE

A method for forming for use upon a patterned layer within an integrated circuit a spin-on-glass (SOG) sandwich composite planarizing dielectric layer construction, and an integrated circuit having formed therein the spin-on-glass (SOG) sandwich composite planarizing dielectric layer construction. To practice the method, there is first provided a substrate having a patterned layer formed thereupon. There is then formed upon the patterned layer and the substrate a first conformal dielectric layer. There is then formed upon the first conformal dielectric layer a spin-on-glass (SOG) planarizing dielectric layer to a thickness greater than the thickness of the patterned layer. There is then planarized through a chemical-mechanical polish (CMP) planarizing method the spin-on-glass (SOG) planarizing dielectric layer and the first conformal dielectric layer, without exposing the patterned layer, to form a planarized spin-on-glass (SOG) planarizing dielectric layer and a partially planarized first conformal dielectric layer. Finally, there is formed upon the planarized spin-on-glass (SOG) planarizing dielectric layer and the partially planarized first conformal dielectric layer a second conformal dielectric layer.

(FIGURE 2 IS SUGGESTED FOR PUBLICATION)