ESD PROTECTION NETWORK USED FOR SOI TECHNOLOGY

ABSTRACT

A method for forming an electrostatic discharge device using silicon-on-insulator technology is described. An N-well is formed within a silicon semiconductor substrate. A P+ region is implanted within a portion of the N-well and an N+ region is implanted within a portion of the semiconductor substrate not occupied by the N-well. An oxide layer is formed overlying the semiconductor substrate and patterned to form openings to the semiconductor substrate. An epitaxial silicon layer is grown within the openings and overlying the oxide layer. Shallow trench isolation regions are formed within the epitaxial silicon layer extending to the underlying oxide layer. Gate electrodes and associated source and drain regions are formed in and on the epitaxial silicon layer between the shallow trench isolation regions. An interlevel dielectric layer is deposited overlying the gate electrodes. First contacts are opened through the interlevel dielectric layer to the underlying source and drain regions. The interlevel dielectric layer is covered with a mask that covers the first contact openings. Second contact openings are opened through the interlevel dielectric layer, shallow trench isolations, and the oxide layer to the N+ region and P+ region. The mask is removed. The first and second contact openings are filled with a conducting layer to complete formation of an ESD device.

(Figure 1)