

Description

Technical Field

This invention relates generally to digital telephone systems and, more particularly, to a digital loop transceiver for use in a digital telephone system comprising a digital PABX and a plurality of digital subscriber sets.

Background Art

When a voice call is made using a conventional analog subscriber set, only a small portion of the frequency spectrum available on the typical subscriber line is utilized. During the development of distributed data processing systems, an effort was made to utilize the existing subscriber line network to facilitate communication of the digital data used by such systems. Various types of modulator/demodulator (modem) devices have been developed to take advantage of the latent capability of the subscriber line network to support digital data communication at data rates significantly greater than that required for analog voice communication. For example, synchronous modems are commercially available which utilize the differential phase shift keyed (DPSK) modulation/demodulation technique to provide data communication at rates up to 9600 baud. However, even in the digital private automatic branch exchanges (PABXs) which support intra-exchange communication of voice information in the form of digital PCM voice data words, the response characteristics of the several analog components of the typical analog card used therein generally prevent reliable communication at higher rates.

Several techniques have been proposed for providing higher speed digital data communication between subscribers through such PABXs. An example of a digital conventional PABX and an analog line circuit using dedicated digital integrated circuits is taught by N. Wellenstein on pages 131—136 of *Electrical Design News*, June 10, 1981. However, previous techniques typically require the installation of additional pairs of subscriber lines to subscribers requiring the service and/or redesign/modification of the particular PABX to provide the capability to process the pure digital data words in a manner different from the digital PCM voice data words. Another example of use of integrated circuits in a digital telephone is taught by A. Boleda et al. in the February 14, 1980 IEEE International Solid-State Circuits Conference, pages 176—177. Boleda et al. teach a line interface circuit which uses BPRZ format. Becker et al. teach in EP—A—0 036 622, U.S. Patent 4,397,030, a digital communication system utilizing eight speech bits, a synchronization/signalling bit and a data bit in a thirty-two word format. The system receives data in frame format comprising thirty-two ten bit words. Each ten bit word has eight data bits, a synchronization/signalling bit and an additional data bit. The system also transmits data in the same frame format. However, the system taught by Becker et

al. does not fully utilize the bandwidth capacity of the signalling channel for useful data. Additional circuitry is also required in the frame oriented system of Becker et al. to implement a pattern search and recognition algorithm required to obtain data synchronization.

Summary of the Invention

Accordingly, it is an object of the present invention to enable digital data words to be communicated at significantly higher speeds and for greater distances over an existing, installed base of subscriber lines, without any redesign or modification of the conventional digital PABX.

In accordance with the present invention, there is provided a digital loop transceiver circuit which provides duplex communication of digital data words on either a single or on first and second channels and a signalling bit associated with at least one of the channels. Communication is between a duplex subscriber line and a digital I/O port. The circuit has a receiver for successively receiving a first and a second of the digital data words and the signalling bit in synchronization with a receive data clock. The first digital data word and the signalling bit are received from the digital I/O port in response to a first channel receive enable signal. The second digital data word is received from the digital I/O port in response to a second channel receive enable signal. The circuit also has a transmitter for transmitting third and fourth digital data words and the signalling bit in synchronization with a transmit data clock. The third digital data word is transmitted to the digital I/O port in response to a first channel transmit enable signal. The fourth digital data word is transmitted to the digital data port in response to a second channel transmit enable signal. The circuit is characterized by modulation means for serially modulating the first and second digital data words and the respective signalling bit for transmission via a first portion of the subscriber line, the first and second data words and the respective signalling bit being received from the digital I/O port in response to at least one receive enable signal (RE1); sync detection means for providing a valid sync signal to synchronize the digital loop transceiver circuit in response to detecting the energy of a differential phase shift keyed signal having a predetermined frame length on a second portion of said subscriber line, said modulated signal comprising a third and a fourth digital data word and respective signalling bit; and demodulation means for serially demodulating data in response to said valid sync signal, said demodulation means demodulating the third and fourth digital data words and said signalling bit received via the second portion of the subscriber line.

Brief Description of the Drawings

Figure 1 is a block representation of a private automatic branch exchange (PABX) adapted in accordance with the present invention.

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Figure 2 is a schematic diagram of an analog line card for use in the PABX of Figure 1.

Figure 3 is a digital line card constructed in accordance with the present invention for use in the PABX of Figure 1.

Figure 4 is a digital subscriber set constructed in accordance with the present invention to communicate over a subscriber line with the digital line card of Figure 3.

Figure 5 is a digital loop transceiver (DLT) constructed in accordance with the present invention for use in the digital line card of Figure 3 and the digital subscriber set of Figure 4.

Figure 6 is a schematic representation of a 4-wire communication system between the DLT in the digital line card of Figure 3 and the DLT in the digital subscriber set of Figure 4.

Figure 7 is a timing diagram illustrating a typical exchange between the DLT in the digital line card of Figure 3 and the PABX of Figure 1.

Figure 8 is a timing diagram illustrating a typical exchange between the DLT in the subscriber set of Figure 4 and the codec/filter therein.

Figure 9 is a schematic representation of a 2-wire communication system between the DLT in the digital line card of Figure 3 and the DLT in the digital subscriber set of Figure 4.

Description of the Preferred Embodiment

Shown in Figure 1 is a conventional private automatic branch exchange (PABX) 10 comprised generally of a main call processor 12 having associated memory 14, a time slot interchange circuit 16, a set of call processing microprocessors 18—18', each having an associated memory 20—20', and a plurality of conventional analog line cards 22. In the illustrated form, the PABX 10 also includes at least two digital line cards 22' constructed in accordance with the present invention.

In a typical digital telephone switching system such as the PABX 10, the main call processor 12 coordinates, via a system bus 24, the call processing activities of each of the several call processing microprocessors 18—18'. In turn, each of the call processing microprocessors 18—18' controls, via respective control buses 26—26', the communication of digital PCM voice data words via respective data buses 28—28' between the several line cards 22 assigned to such microprocessor 18—18'.

In general, each of the analog line cards 22 comprises a time slot assignment and control circuit (TSAC) 30 for selectively enabling a codec/filter 32 to digitally encode an analog voice input signal received via a subscriber line interface circuit (SLIC) 34 from a conventional single channel subscriber set (not shown) coupled to tip and ring conductors for output as a digital pulse code modulation (PCM) voice data word on the respective data bus 28—28', and to decode a digital PCM voice data word received on the data bus 28—28' for output as an analog voice output signal to the subscriber set (not shown) via the SLIC 34. Shown in Figure 2 is a circuit schematic

for such a conventional analog line card 22, using components commercially available from Motorola. The various control and data signals which are provided to or by the line card 22 are generally referred to as the "backplane" of the PABX 10.

In a typical telephone call initiated by a subscriber served by a "source" line card 22 controlled by, say, the call processing microprocessor 18 to a subscriber served by a "destination" line card 22 controlled by, for example, the call processing microprocessor 18', the TSAC 30 on the source line card 22 initially detects via the associated SLIC 34 that the source subscriber set is off hook, and routes the call routing information to the call processing microprocessor 18 for transfer to the main call processor 12. If the destination line card 22 is not indicated in the memory 14 as being busy, the main call processor 12 then requests the call processing microprocessor 18' to notify the destination line card 22 of the call. If, upon providing the system-generated ring signal to the destination subscriber set via the respective SLIC 34, the associated TSAC 30 advises the call processor 18' that the destination subscriber set has been taken off hook, the call processing microprocessor 18' advises the main call processor 12 that the requested connection has been established. During a particular transmit time slot assigned by the main call processor 12, the TSAC 30 on the source line card 22 enables the associated codec/filter 32 to encode the analog voice signal then being received from the source subscriber set via the SLIC 34 for output as a digital PCM voice data word onto the data bus 28. Meanwhile, the main call processor 12 has enabled the time slot interchange circuit 16 to couple the data bus 28 to the data bus 28' to facilitate the requested intra-exchange communication of the digital PCM voice data word. Simultaneously, the TSAC 30 on the destination line card 22 enables the associated codec/filter 32 to decode the digital PCM voice data word on the data bus 28' for output as an analog voice signal to the destination subscriber set via the SLIC 34. In a similar manner, but during a different receive time slot assigned by the main call processor 12, the destination line card 22 is allowed to encode the analog voice signal received from the destination subscriber set for transmission as a digital PCM voice data word via data bus 28', interchange circuit 16 and data bus 28' to the source line card 22 for decoding and output to the source subscriber set. If this exchange of digital PCM voice data words occurs at a sufficiently high frame rate, say of the order of 8 kHz, then it will appear to each of the subscribers that there is a direct analog link between their respective subscriber sets.

In the general form shown in Figure 1, each of the digital line cards 22' comprises a time slot assignment and control circuit (TSAC) 30' for selectively enabling a digital loop transceiver (DLT) 36 (see Figure 5) to receive digital data words via a subscriber line interface network 38

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from a dual channel, digital subscriber set, such as that shown in Figure 4, which is coupled to respective receive and transmit pairs of tip and ring conductors, for direct output on the respective data bus 28—28' in the same manner as the digital PCM voice data words are output by the codec/filter 32 in the analog line cards 22; and to receive digital data words on the data bus 28—28' for direct output to the subscriber set via the subscriber line interface network 38. Shown in Figure 3 is a circuit schematic for the digital line card 22', wherein: the TSAC 30' comprises a pair of the Motorola time slot assignment circuits (TSACs), one for each of the two digital communication channels the digital line card 22' is capable of simultaneously supporting; the DLT 36 comprises an integrated circuit constructed in accordance with Figure 5; and the subscriber line interface network 38 comprises a transit isolation transformer 40 coupled to the tip and ring conductors which comprise the receive pair of the subscriber line and a receive isolation transformer 42 coupled to the tip and ring conductors which comprise the transmit pair of the subscriber line. As illustrated in Figure 3, the digital line card 22' responds to and provides the same control and data signals which are provided to or by the analog line card 22 via the backplane of the PABX 10.

Shown in Figure 4 is a dual channel, digital subscriber set 44 constructed in accordance with the present invention. In general, the subscriber set 44 comprises a digital loop transceiver (DLT) 36' (see Figure 5) for receiving digital data words from the digital line card 22' (see Figure 3) via a subscriber line interface network 38' coupled to respective receive and transmit pairs of tip and ring conductors, for output, if digital PCM voice data words, to a conventional codec/filter 32' for subsequent decoding and output as an analog voice output via a voice I/O network 46, or, if digital data words, to a subscriber data processor (not shown) via a data port 48; and for transmitting digital data words provided either by the codec/filter 32' in the form of digital PCM voice data words of by the subscriber data processor in the form of digital data words, to the digital line card 22' via the subscriber line interface network 38'. In the preferred form, the voice I/O network 46 includes a voice input portion 50, and a voice output portion 52; the DLT 36' comprises an integrated circuit constructed in accordance with Figure 5; and the subscriber line interface network 38' comprises a transmit isolation transformer 40' coupled to the tip and ring conductors which comprise the transmit pair of the subscriber line and a receive isolation transformer 42' coupled to the tip and ring conductors which comprise the receive pair of the subscriber line. In the illustrated form, a conventional tone generator 54, such as the Mostek MK5087, interacts with a dial keypad 56 and the voice I/O network 46 to provide the call routing information required to establish each of the two communication channels, while a conventional hook switch

58 provides call initiation signalling information to the DLT 36'. An audible indication of an incoming call is provided via a ringing transducer 60. A subscriber set power supply 62 derives operating power for the several components of the subscriber set 44 from the subscriber line in a conventional manner.

Shown in Figure 5 is a block diagram of the digital loop transceiver (DLT) 36, constructed in accordance with the present invention. In general, the DLT 36 comprises a digital interface portion 64 for interfacing with the PABX 10 in a master operating mode and with the codec/filter 32 and subscriber data processor in a slave operating mode, a modulator/demodulator portion 66 for transmitting and receiving digital data words via the subscriber line, and a sequencer and control portion 68 for controlling the sequence of operations performed by the digital interface and modulator/demodulator portions 64 and 66, respectively.

In the digital interface portion 64, a receive (RX) control circuit 70 responds to either of two channel receive enable signals, RE1 and RE2, by enabling a receive (RX) register 72 of the shift register type to serially receive digital data bits via a receive (RX) terminal in synchronization with a receive data clock (RDC) on a CLK/RDC terminal. When a predetermined "frame" of data (see discussion below) has been received, the sequencer and control portion 68 enables the RX register 72 to transfer the "transmit" frame of data in parallel into a transmitter (XMIT) register 74 in the modulator/demodulator portion 66. Simultaneously, the then-current states of the two channel signalling bits on respective S11 and S21 terminals are latched and inserted into the frame of data in the XMIT register 74. Substantially independently, the sequencer and control portion 68 enables a transmit (TX) register 76 to receive a "receive" frame of data in parallel from a receiver (RCV) register 78 in the modulator/demodulator portion 66. Simultaneously, the two channel signalling bits in the receive frame of data are latched and outputted on respective S10 and S20 terminals. In response to either of two channel transmit enable signals, TE1 and TE2, a transmit (TX) control circuit 80 enables the TX register 76 to serially transmit the receive frame of data via a TX terminal in synchronization with a transmit data clock (TDC) on an X1/TDC terminal.

In the modulator/demodulator portion 66, a digital to analog converter (DAC) control circuit 82 periodically enables a digital to analog converter (DAC) 84 to transmit the transmit frame of data in the XMIT register 74 to the transmit transformer 40 in the subscriber line interface network 38 using a differential pair of output drivers 86 and 88 coupled to respective line output terminals LO1 and LO2. In the preferred embodiment, the DAC 84 utilizes a burst differential phase shift keyed (DPSK) modulation technique at a carrier frequency of 265 kHz. Substantially independently, an input buffer 90 of the differential to single ended output type in the modulation/

demodulation portion 66 couples the signal received from the receive transformer 42 in the subscriber line interface network 38 via line input terminals L11 and L12 to a sync detector 92 via a window detector 94 and to a correlator 96 via a comparator 98. As phase shifts of the proper form are decoded by the correlator 96, the "decoded" bits are shifted into a shift register portion thereof which maintains the most recently received set of data bits which might constitute a frame. When the energy of a DPSK signal of the proper frame length is detected, the sync detector 92 provides a valid sync signal to enable the correlator 96 to transfer the receive frame of data bits being maintained therein, in parallel to the RCV register 78. A switched capacitor bandgap reference 100 similar to that shown and described in WO-A-82/02806 provides a precision reference voltage to the DAC 84, the window detector 94, and the comparator 98. Periodically, the offsets of the input buffer 90, the window detector 94, the comparator 98, and the bandgap reference 100 are zeroed by an auto-zero circuit 102 in a manner similar to that shown and described in WO-A-82/02804.

In operation, the DLT 36 provides duplex communication of digital data words on a pair of independent channels and a signalling bit associated with each of the channels, between the duplex subscriber line and a digital data port. In a typical line transmission operation, the RX register 72 successively receives a digital data word for each of the channels in synchronization with the receive data clock, with the digital data word for the first of the channels being received from the digital I/O port via the RX terminal in response to the first of the channel receive enable signals, RE1, and the digital data word for the second of the channels being received from the digital I/O port via the RX terminal in response to the second of the channel receive enable signals, RE2. After the last data bit of the frame has been clocked into the RX register 72, both data words are transferred to the XMIT register 74, and the then-current states of the respective channel signalling bits on the S11 and S21 terminals added to complete the frame. As soon as the frame has been assembled, the DAC control circuit 82 actuates the DAC 84 to serially modulate the first and second digital data words and the respective channel signalling bits in the frame, for transmission via the transmit transformer 40 to one of the pairs of wires in the subscriber line.

In a typical line reception operation, the sync detector 92 monitors the signal received via the receive transformer 42 on the other pair of wires in the subscriber line, and provides a valid sync signal in response to detecting the energy of a DPSK modulated signal of the proper frame length. Meanwhile, the correlator 96 has been serially demodulating the sequentially received bits which might constitute a frame containing a digital data word for each of the channels and the respective channel signalling bits. In response to the valid sync signal, indicating that a valid frame

has indeed been received, the correlator 96 transfers the frame to the RCVR register 78. At an appropriate time depending upon the mode of operation, the frame is then transferred from the RCVR register 78 to the TX register 76 and the respective channel signalling bits latched for output on the S10 and S20 terminals. The TX register 76 then sequentially transmits the digital data words in synchronization with the transmit data clock, with the digital data word for the first channel being transmitted to the digital I/O port via the TX terminal in response to the first of the channel transmit enable signals, TE1, and the digital data word for the second channel being transmitted to the digital I/O port via the TX terminal in response to the second of the channel transmit enable signals, TE2.

Shown in Figure 6 is a schematic representation of a 4-wire or duplex subscriber line which has been coupled at the exchange end thereof to the DLT 36 in the digital line card 22' via the transmit and receive transformers 40 and 42, respectively, and the subscriber end thereof to the DLT 36' in the digital subscriber set 44 via the transmit and receive transformers 40' and 42', respectively. In the dual-channel form of the duplex system, a frame of data comprises an 8-bit digital data word for the first channel, an 8-bit digital data word for the second channel, and the signalling bits for the first and second channels. Preferably, the frame also includes a parity bit, either even or odd, as desired. A suitable frame format is illustrated in Figure 6.

In the digital line card 22' shown in Figure 3, the DLT 36 is placed in the master mode of operation by a logic high signal on a master/slave (M/S) terminal. In the master mode, the DLT 36 emulates the codec/filter 32 with respect to the backplane by receiving/transmitting the digital data words just like the codec/filter 32, and by responding to the various control signals just like the codec/filter 32. In particular, the RX register 72 successively receives a digital data word for each of the channels in synchronization with the data clock provided by the PABX 10 via the backplane, with the data word for the first channel being received from the backplane via the RX terminal in response to the RE1 signal provided by a respective one of the TSACs 30 during the receive time slot assigned to the first channel, and the data word for the second channel being received from the backplane via the RX terminal in response to the RE2 signal provided by the other TSAC 30 during the receive time slot assigned to the second channel. In response to the next master sync input (MSI) received via an X2/MSI terminal after the last data bit of the frame has been clocked into the RX register 72, both digital data words are transferred to the XMIT register 74, and the then-current states of the respective channel signalling bits provided via the S11 and S21 terminals by the TSACs 30, respectively, added to complete the frame. As soon as the frame has been assembled, the DAC control circuit 82 actuates the DAC 84 to serially modulate

the first and second digital data words and the respective channel signalling bits in the frame, for transmission via the transmit transformer 40 to the receive pair of wires in the subscriber line.

Simultaneously, the sync detector 92 monitors the signal received via the receive transformer 42 on the transmit pair of wires in the subscriber line, and provides the valid sync signal in response to detecting the energy of a DPSK modulated signal of the proper frame length. Meanwhile, the correlator 96 has been serially demodulating the sequentially received bits which might constitute a frame containing a digital data word for each of the channels and the respective channel signalling bits. In response to the valid sync signal, indicating that a valid frame has indeed been received, the correlator 96 transfers the frame to the RCVR register 78. In response to the next MSI, the frame is then transferred from the RCVR register 78 to the TX register 76 and the respective channel signalling bits latched for output on the S10 and S20 terminals. The TX register 76 then sequentially transmits the digital data words in synchronization with the transmit data clock provided by the PABX 10 via the backplane, with the digital data word for the first channel being transmitted to the backplane via the TX terminal in response to the TE1 signal provided by the first one of the TSACs 30 during the transmit time slot assigned to the first channel, and the digital data word for the second data channel being transmitted to the backplane via the TX terminal in response to the TE2 signal provided by the other TSAC 30 during the transmit time slot assigned to the second channel. A typical sequential interaction of the DLT 36 with the TSACs 30, and with the PABX 10 is illustrated by way of example in the timing diagram of Figure 7.

In the subscriber set 44 shown in Figure 4, the DLT 36' is placed in the slave mode of operation by a logic low on the master/slave (M/S) terminal. In the slave mode, the DLT 36' emulates the functions of the TSAC 30 and the backplane with respect to the codec/filter 32' by providing the digital PCM voice data words and control signals necessary for the codec/filter 32' to operate, and by receiving the digital PCM voice data words provided by the codec/filter 32' just like the backplane. In this mode, the sync detector 92 monitors the signal received via the receive transformer 42' on the receive pair of wires in the subscriber line, and provides the valid sync signal in response to detecting the energy of a DPSK modulated signal of the proper frame length. Meanwhile, the correlator 96 has been serially demodulating the sequentially received bits which might constitute a frame containing a digital data word for each of the channels and the respective channel signalling bits. In response to the valid sync signal, indicating that a valid frame has indeed been received, the correlator 96 transfers the frame to the RCVR register 78. The frame is then promptly transferred from the RCVR register 78 to the TX register 76 and the respective channel signalling bits latched for output on the

S10 and S20 terminals. The TX register 76 then sequentially transmits the digital data words in synchronization with a transmit data clock generated by a prescaler and oscillator 104 using a crystal coupled between the X1/TDC and X2/MSI terminals, with the digital data word for the first channel being transmitted to the codec/filter 32' via the TX terminal in synchronization with a TE1 signal generated by the TX control 80 relative to the last valid sync signal, and the digital data word for the second data channel being transmitted to the data port 48 via the TX terminal in synchronization with a TE2 signal generated by the TX control 80 relative to the last valid sync signal.

In response to each of the valid sync signals provided by the sync detector 92, the RX register 72 successively receives a digital data word for each of the channels in synchronization with a receive data clock generated by the sequencer and control 68, with the digital PCM voice data word for the first channel being received from the codec/filter 32' via the RX terminal in synchronization with an RE1 signal generated by the RX control 70 relative to the last valid sync signal, and the digital data word for the second channel being received from the data port 48 via the RX terminal in response to an RE2 signal generated by the RX control 70 relative to the last valid sync signal. In response to the next valid sync signal provided by the sync detector 92, both digital data words are transferred to the XMIT register 74 and the then-current states of the respective channel signalling bits provided via the S11 and S21 terminals by the hook switch 58 and, if appropriate, the subscriber data processor, respectively, are added to complete the frame. As soon as the frame has been assembled, the DAC control circuit 82 actuates the DAC 84 to serially modulate the first and second digital data words and the respective channel signalling bits in the frame, for transmission via the transmit transformer 40' to the transmit pair of wires in the subscriber line. A typical sequential interaction of the DLT 36' with the codec/filter 32' and the subscriber data processor is illustrated by way of example in the timing diagram of Figure 8.

Although the DLT 36 is designed to operate primarily in the dual-channel mode over a duplex subscriber line, the DLT 36 may be operated in an exchange which has only one pair of wires in each subscriber line by applying a logic high to a format (FOR) terminal thereof. In the illustrated form of such a 2-wire system shown in Figure 9, the half duplex subscriber line is coupled at the exchange end thereof to the DLT 36 in the digital line card 22' via a transmit/receive isolation transformer 106, and at the subscriber end thereof to the DLT 36' in the digital subscriber set 44 via a transmit/receive isolation transformer 106'. In the dual-channel form of the half duplex system, a frame of data comprises an 8-bit digital data word for the first channel, the signalling bit for the first channel, and a second signalling bit for use by the subscriber data processor as a digital data bit.

Preferably, the frame also includes a parity bit, either even or odd, as desired. A suitable frame format is illustrated in Figure 9. Since only a single digital data bit may be transferred in each frame, the effective data bit transmission rate is only 8 kHz rather than the 64 kHz of the duplex system. However, this reduced data rate may be acceptable in situations where the cost to install the second pair of wires in the subscriber line outweighs the benefits of higher transmission rate.

Claims

1. A digital loop transceiver circuit (36) for providing duplex communication of digital data words on first and second channels and a signalling bit associated with one of said first and second channels, between a duplex subscriber line and a digital I/O port interfacing a data bus (28') and a control bus (26'), the circuit (36) having a receiver (68, 70, 72) for successively receiving a first and a second of the digital data words and the signalling bit in synchronization with a receive data clock, the circuit (36) also having a transmitter (68, 76, 80) for transmitting a third and a fourth of the digital data words and the signalling bit in synchronization with a transmit data clock, the circuit being characterized by:

modulation means (66, 82, 84) for serially modulating the first and second digital data words and the respective signalling bit for transmission via a first portion of the subscriber line, the first and second data words and the respective signalling bit being received from the digital I/O port in response to at least one receive enable signal (RE1);

sync detection means (92) for providing a valid sync signal to synchronize the digital loop transceiver circuit (36) in response to detecting the energy of a differential phase shift keyed signal having a predetermined frame length on a second portion of said subscriber line, said modulated signal comprising a third and a fourth digital data word and respective signalling bit; and

demodulation means (90, 96) for serially demodulating data in response to said valid sync signal, said demodulation means demodulating the third and fourth digital data words and said signalling bit received via the second portion of the subscriber line.

2. A digital loop transceiver circuit (36) for operation in a digital subscriber terminal, for providing duplex communication of digital data words between a duplex subscriber line and first, second and signalling bit channels, the circuit (36) having a transmitter (68, 76, 78, 80) for successively transmitting first and second digital data words and the signalling bit in synchronization with an output data clock (Clk), the circuit also having a receiver (68, 70, 72, 74) for successively receiving a third and a fourth digital data word and a signalling bit in synchronization with the output data clock (Clk), the circuit (36) being characterized by:

sync detection means (92) for detecting the energy of a differential phase shift keyed signal having a predetermined frame length on a first portion of the subscriber line, the modulated signal comprising a first and a second digital data word and respective signalling bit, for providing a valid sync signal in response to said detection;

demodulation means (90, 96) for serially demodulating data in response to said valid sync signal, said demodulation means demodulating the first and second digital data words and said signalling bit received via the first portion of the subscriber line, and providing the demodulated signalling bit to the transmitter; and

modulation means (66) for serially modulating the third and fourth digital data words and the respective signalling bit for transmission via the second portion of the subscriber line in response to the valid sync signal, said third and fourth digital data words.

3. The digital loop transceiver circuit of claim 2 further characterized by:

logic means (68, 70, 80, 104) for providing at least one transmit enable (TE1), one receive enable (RE1) and one data clock (Clk) signal in response to the valid sync signal, said transmit enable, receive enable and clock signals controlling the timing of said first, second and signalling bit duplex channels.

Patentansprüche

1. Digitalschleifen-Sender-Empfänger-Schaltung (36) zur Errichtung einer Duplexübertragung von Digitaldatenwörtern auf ersten und zweiten Kanälen und eines einem der genannten ersten und zweiten Kanäle zugeordneten Signalisierungsbits zwischen einer Duplexteilnehmerleitung und einem digitalen I/O-Tor, das die Schnittstelle zwischen einem Datenbus (28') und einem Steuerbus (26') bildet, wobei die Schaltung (36) einen Empfänger (68, 70, 72) zum aufeinanderfolgenden Empfang eines ersten und eines zweiten der Digitaldatenwörter und des Signalisierungsbits synchron mit einem Empfangsdaten-takt aufweist, die Schaltung (36) weiterhin einen Sender (68, 76, 80) zur Aussendung eines vierten und eines fünften der Digitaldatenwörter und des Signalisierungsbits synchron mit einem Sendetakt aufweist, gekennzeichnet durch:

eine Modulationseinrichtung (66, 82, 84) zur seriellen Modulation der ersten und zweiten Digitaldatenwörter und des entsprechenden Signalisierungsbits zur Aussendung über einen ersten Abschnitt der Teilnehmerleitung, wobei die ersten und zweiten Datenwörter und das entsprechende Signalisierungsbit von dem digitalen I/O-Tor in Abhängigkeit von wenigstens einem Empfangsfreigabesignal (RE1) empfangen werden;

eine Sync-Detektoreinrichtung (92) zum Abgeben eines gültigen Sync-Signals zur Synchronisierung der Digitalschleifen-Sender-Empfänger-Schaltung (36) in Abhängigkeit von der Ermittlung der Energie eines differenzphasen-

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Preferably, the frame also includes a parity bit, either even or odd, as desired. A suitable frame format is illustrated in Figure 9. Since only a single digital data bit may be transferred in each frame, the effective data bit transmission rate is only 8 kHz rather than the 64 kHz of the duplex system. However, this reduced data rate may be acceptable in situations where the cost to install the second pair of wires in the subscriber line outweighs the benefits of higher transmission rate.

Claims

1. A digital loop transceiver circuit (36) for providing duplex communication of digital data words on first and second channels and a signalling bit associated with one of said first and second channels, between a duplex subscriber line and a digital I/O port interfacing a data bus (28') and a control bus (26'), the circuit (36) having a receiver (68, 70, 72) for successively receiving a first and a second of the digital data words and the signalling bit in synchronization with a receive data clock, the circuit (36) also having a transmitter (68, 76, 80) for transmitting a third and a fourth of the digital data words and the signalling bit in synchronization with a transmit data clock, the circuit being characterized by:

modulation means (66, 82, 84) for serially modulating the first and second digital data words and the respective signalling bit for transmission via a first portion of the subscriber line, the first and second data words and the respective signalling bit being received from the digital I/O port in response to at least one receive enable signal (RE1);

sync detection means (92) for providing a valid sync signal to synchronize the digital loop transceiver circuit (36) in response to detecting the energy of a differential phase shift keyed signal having a predetermined frame length on a second portion of said subscriber line, said modulated signal comprising a third and a fourth digital data word and respective signalling bit; and

demodulation means (90, 96) for serially demodulating data in response to said valid sync signal, said demodulation means demodulating the third and fourth digital data words and said signalling bit received via the second portion of the subscriber line.

2. A digital loop transceiver circuit (36) for operation in a digital subscriber terminal, for providing duplex communication of digital data words between a duplex subscriber line and first, second and signalling bit channels, the circuit (36) having a transmitter (68, 76, 78, 80) for successively transmitting first and second digital data words and the signalling bit in synchronization with an output data clock (Clk), the circuit also having a receiver (68, 70, 72, 74) for successively receiving a third and a fourth digital data word and a signalling bit in synchronization with the output data clock (Clk), the circuit (36) being characterized by:

sync detection means (92) for detecting the energy of a differential phase shift keyed signal having a predetermined frame length on a first portion of the subscriber line, the modulated signal comprising a first and a second digital data word and respective signalling bit, for providing a valid sync signal in response to said detection;

demodulation means (90, 96) for serially demodulating data in response to said valid sync signal, said demodulation means demodulating the first and second digital data words and said signalling bit received via the first portion of the subscriber line, and providing the demodulated signalling bit to the transmitter; and

modulation means (66) for serially modulating the third and fourth digital data words and the respective signalling bit for transmission via the second portion of the subscriber line in response to the valid sync signal, said third and fourth digital data words.

3. The digital loop transceiver circuit of claim 2 further characterized by:

logic means (68, 70, 80, 104) for providing at least one transmit enable (TE1), one receive enable (RE1) and one data clock (Clk) signal in response to the valid sync signal, said transmit enable, receive enable and clock signals controlling the timing of said first, second and signalling bit duplex channels.

Patentansprüche

1. Digitalschleifen-Sender-Empfänger-Schaltung (36) zur Errichtung einer Duplexübertragung von Digitaldatenwörtern auf ersten und zweiten Kanälen und eines einem der genannten ersten und zweiten Kanäle zugeordneten Signalisierungsbits zwischen einer Duplexteilnehmerleitung und einem digitalen I/O-Tor, das die Schnittstelle zwischen einem Datenbus (28') und einem Steuerbus (26') bildet, wobei die Schaltung (36) einen Empfänger (68, 70, 72) zum aufeinanderfolgenden Empfang eines ersten und eines zweiten der Digitaldatenwörter und des Signalisierungsbits synchron mit einem Empfangsdatenkontakt aufweist, die Schaltung (36) weiterhin einen Sender (68, 76, 80) zur Aussendung eines vierten und eines fünften der Digitaldatenwörter und des Signalisierungsbits synchron mit einem Sendedatenkontakt aufweist, gekennzeichnet durch:

eine Modulationseinrichtung (66, 82, 84) zur seriellen Modulation der ersten und zweiten Digitaldatenwörter und des entsprechenden Signalisierungsbits zur Aussendung über einen ersten Abschnitt der Teilnehmerleitung, wobei die ersten und zweiten Datenwörter und das entsprechende Signalisierungsbit von dem digitalen I/O-Tor in Abhängigkeit von wenigstens einem Empfangsfreigabesignal (RE1) empfangen werden;

eine Sync-Detektoreinrichtung (92) zum Abgeben eines gültigen Sync-Signals zur Synchronisierung der Digitalschleifen-Sender-Empfänger-Schaltung (36) in Abhängigkeit von der Ermittlung der Energie eines differenzphasen-



(18)

verschiebungsmodulierten Signals, das eine vorbestimmte Rahmenlänge hat, auf einem zweiten Abschnitt der genannten Teilnehmerleitung, wobei das genannte modulierte Signal ein drittes und ein viertes Digitaldatenwort und ein entsprechendes Signalisierungsbit enthält; und

eine Demodulationseinrichtung (90, 96) zum seriellen Demodulieren von Daten in Abhängigkeit von dem genannten gültigen Sync-Signal, wobei die Demodulationseinrichtung die dritten und vierten Digitaldatenwörter und das Signalisierungsbit, die über den zweiten Abschnitt der Teilnehmerleitung empfangen werden, demoduliert.

2. Digitalschleifen-Sender-Empfänger-Schaltung (36) zum Betrieb eines digitalen Teilnehmeranschlusses zur Errichtung einer Duplexübertragung von Digitaldatenwörtern zwischen einer Duplexteilnehmerleitung und ersten, zweiten und Signalisierungsbitkanälen, wobei die Schaltung (36) einen Sender (68, 76, 78, 80) zum aufeinanderfolgenden Aussenden von ersten und zweiten Digitaldatenwörtern und des Signalisierungsbits in Synchronisation mit einem Ausgabedatentakt (Clk) aufweist, die Schaltung weiterhin einen Empfänger (68, 70, 72, 74) zum aufeinanderfolgenden Empfangen eines dritten und eines vierten Digitaldatenwortes und eines Signalisierungsbits in Synchronisation mit dem Ausgabedatentakt (Clk) aufweist, gekennzeichnet durch:

eine Sync-Detektoreinrichtung (92) zur Ermittlung der Energie eines differenzphasenverschiebungsmodulierten Signals, das eine vorbestimmte Rahmenlänge aufweist, auf einem ersten Abschnitt der Teilnehmerleitung, wobei das modulierte Signal ein erstes und ein zweites Digitaldatenwort und ein entsprechendes Signalisierungsbit enthält, um ein gültiges Sync-Signal in Abhängigkeit von der genannten Ermittlung zu liefern;

eine Demodulationseinrichtung (90, 96) zum seriellen Demodulieren von Daten in Abhängigkeit von dem genannten gültigen Sync-Signal, wobei die Demodulationseinrichtung die ersten und zweiten Digitaldatenwörter und das Signalisierungsbit demoduliert, die über den ersten Abschnitt der Teilnehmerleitung empfangen werden, und das demodulierte Signalisierungsbit an den Sender liefert; und

eine Modulationseinrichtung (66) zum seriellen Modulieren der dritten und vierten Digitaldatenwörter und des entsprechenden Signalisierungsbits zur Aussendung der genannten dritten und vierten Digitaldatenwörter über den zweiten Abschnitt der Teilnehmerleitung in Abhängigkeit von dem gültigen Sync-Signal.

3. Digitalschleifen-Sender-Empfänger-Schaltung nach Anspruch 2, weiterhin gekennzeichnet durch:

eine logische Einrichtung (68, 70, 80, 104) zur Abgabe wenigstens eines Sendefreigabesignals (TE1), eines Empfangsfreigabesignals (RE1) und eines Datentaktsignals (Clk) in Abhängigkeit von dem gültigen Sync-Signal, wobei die vorgenannten Signale für Sendefreigabe, Empfangsfreigabe

und Takt die Zeitgabe der ersten, zweiten und Signalisierungsbitduplexkanäle steuern.

Revendications

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1. Circuit d'émetteur-récepteur à boucle numérique (36) destiné à établir une communication en duplex de mots de données numériques sur un premier et un second canal et un bit de signalisation associé avec l'un desdits premier et second canaux, entre une ligne d'abonné duplex et une connexion d'entrée/sortie numérique faisant interface avec une ligne omnibus de données (28') et une ligne omnibus de commande (26'), le circuit (36) comprenant un récepteur (68, 70, 72) destiné à recevoir successivement un premier et un second des mots de données numériques et le bit de signalisation en synchronisme avec une horloge de données de réception, le circuit (36) comportant également un émetteur (68, 76, 80) destiné à émettre un troisième et un quatrième des mots de données numériques et le bit de signalisation en synchronisme avec une horloge de données d'émission, le circuit étant caractérisé par:

un dispositif de modulation (66, 82, 84) destiné à moduler en série le premier et le second mot de données numériques et le bit de signalisation respectif pour l'émission par l'intermédiaire d'une première partie de la ligne d'abonné, le premier et le second mot de données et le bit de signalisation respectif étant reçus de la connexion d'entrée/sortie numérique en réponse à au moins un signal d'autorisation de réception (RE1);

un dispositif de détection de synchronisation (92) destiné à produire un signal de synchronisation valide pour synchroniser le circuit d'émetteur-récepteur à boucle numérique (36) en réponse à la détection de l'énergie d'un signal modulé par déplacement de phase différentielle ayant une longueur de trame prédéterminée sur une seconde desdites lignes d'abonnés, ledit signal modulé comprenant un troisième et un quatrième mot de données numériques et un bit de signalisation respectif;

un dispositif de démodulation (90, 96) destiné à démoduler en série des données en réponse audit signal de synchronisation valide, ledit dispositif de démodulation démodulant le troisième et le quatrième mot de données numérique et ledit bit de signalisation reçus par l'intermédiaire de la seconde partie de la ligne d'abonné.

2. Circuit d'émetteur-récepteur à boucle numérique (36) destiné à fonctionner dans un terminal d'abonnés numérique, pour établir une communication en duplex de mots de données numériques entre une ligne d'abonnés duplex et un premier et un second canal et de bit de signalisation, le circuit (36) comportant un émetteur (68, 76, 78, 80) pour émettre successivement un premier et un second mot de données numérique et le bit de signalisation en synchronisme avec une horloge de données de sortie (Clk), le circuit comportant également un récepteur (68, 70, 72, 74) pour recevoir successivement un troisième et un qua-



trième mot de données numériques et un bit de signalisation en synchronisme avec l'horloge de données de sortie (Cik), le circuit 36 étant caractérisé par:

un dispositif de détection de synchronisation (92) destiné à détecter l'énergie d'un signal modulé par déplacement de phase différentielle ayant une longueur de trame prédéterminée, sur une première partie de la ligne d'abonné, le signal modulé consistant en un premier et un second mot de données numérique et un bit respectif de signalisation, pour produire un signal de synchronisation valide en réponse à ladite détection;

un dispositif de démodulation (90, 96) destiné à démoduler en série des données en réponse audit signal de synchronisation valide, ledit dispositif de démodulation démodulant le premier et le second mot de données numérique et ledit bit de signalisation reçus par l'intermédiaire de la première partie de la ligne d'abonné et produisant le

bit de signalisation démodulé pour l'émetteur; et

un dispositif de modulation (66) destiné à moduler en série le troisième et le quatrième mot de données numériques et le bit de signalisation respectif pour l'émission par l'intermédiaire de la seconde partie de la ligne d'abonné en réponse au signal de synchronisation valide, du troisième et du quatrième mot de données numérique.

3. Circuit d'émetteur-récepteur à boucle numérique selon la revendication 2, caractérisé en outre par:

un dispositif logique (68, 70, 80, 104) destiné à produire au moins un signal d'autorisation d'émission (TE1), un signal d'autorisation de réception (RE1) et un signal d'horloge de données (Cik) en réponse au signal de synchronisation valide, lesdits signaux d'autorisation d'émission, d'autorisation de réception et d'horloge commandant la temporisation dudit premier, dudit second canal duplex et celui de bits de signalisation.



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