

Description

The invention relates to arrangement comprising a phase-locked loop whose signal path incorporates a phase detector, a loop filter and a controlled oscillator, and a pilot generator for generating a local auxiliary pilot which is applied to the controlled oscillator, and a pilot detector input of which is coupled to the signal path of the loop and an output of which is coupled to a level detector via a filter member.

An arrangement of this type is known *per se* from Japanese Patent publication Kokai 63-107304 and supplies a binary output signal which gives an indication about the state of phase lock of the phase-locked loop.

In the phase-locked state of the loop the output signal of the controlled oscillator is frequency-modulated with the local auxiliary pilot. In the known arrangement this frequency-modulated oscillator signal is applied to a frequency discriminator operating as a pilot detector. To this end an input of the known pilot detector is coupled to the signal path between the output of the controlled oscillator and an input of the phase detector. The auxiliary pilot demodulated by the frequency discriminator is applied to the level detector via a bandpass selection in the filter member. The level detector supplies the above-mentioned binary output signal which has the value of 0 or 1 with respect to a given threshold value in dependence upon the amplitude of the auxiliary pilot selected by means of the filter member.

In the phase-locked state of the loop the oscillator frequency corresponds to the frequency to which the frequency discriminator is tuned, i.e. the zero frequency, and the frequency-modulated oscillator frequency varies within the detection range of the frequency discriminator. The frequency discriminator then supplies the local auxiliary pilot at an amplitude which exceeds said threshold value and thus gives rise to a given output signal value of the level detector, for example 1.

Outside the locking range the oscillator frequency deviates from said zero frequency to such an extent that it does not coincide with the detection range of the frequency discriminator and that the auxiliary pilot cannot be detected. Consequently, the frequency discriminator supplies no or substantially no signal component at the frequency of the auxiliary pilot so that the output signal of the bandpass filter member remains below said threshold value and the level detector supplies the output signal value of 0.

For a correct locking indication the dimensioning of the frequency discriminator and hence the location, the steepness and the range of the detection curve, as well as said threshold value of the level detector should be accurately set to correct values with respect to the locking range of the phase-locked loop. The circuit settings required for this purpose are com-

plex and time-consuming, hence costly.

A solution is known from US patent 4,866,402 in which measures of the first mentioned prior art are extended such that the pilot detector comprises a multiplier circuit for synchronous detection of the auxiliary pilot, a first input of the multiplier circuit being coupled to the signal path of the loop between the phase detector and the controlled oscillator, and a second input of the multiplier circuit being coupled to the pilot generator, an output of the multiplier circuit being coupled to the filter member, comprising a low-pass filter.

In this known arrangement the local auxiliary pilot is applied to the loop filter. The auxiliary pilot signal circulates through the loop filter, the voltage controlled oscillator and the phase detector. Under locked conditions, the phase detector supplies a mixing product which has a frequency equal to that of the auxiliary pilot, whereas under non-locked condition the phase detector does not supply such a mixing product. The pilot detector comprising a multiplier circuit is arranged between the phase detector and a comparator for indicating the presence or absence of the local auxiliary pilot.

It is an object of the invention to enhance the accuracy of detecting the lock-in state of the phase-locked loop in the arrangement.

According to the invention such an arrangement is therefore characterized in that a first phase-shifting circuit precedes one of the two first and second inputs of the multiplier circuit.

It is based on the recognition that not only the amplitude of said mixing product, also referred to as return pilot, but also the phase shift with respect to the original auxiliary pilot signal is characteristic of the state of phase lock. Loop parameters such as bandwidth, phase shift and loop gain in the phase-locked state of the loop deviate from those outside the phase-locked state.

When the measure according to the invention is used, this recognition is utilized for adjusting the pilot detector at an optimum working point at the desired lock-in state. Consequently, the threshold value of the level detector may vary within a comparatively large tolerance range without influencing the accuracy and uniformity of the locking indication obtained in accordance with the invention.

For an effective locking indication the quantity (amplitude or phase) of the return pilot, which varies to the greatest extent at the transition from the phase-locked state to the unlocked state, and conversely, should be detected.

A preferred embodiment is therefore characterized in that the frequency of the local auxiliary pilot is located within the passband of the loop, the pilot detector being arranged to effect a substantially synchronous amplitude detection of the local auxiliary pilot supplied to the first input of the multiplier circuit.

An optimum synchronous amplitude detection of

the return pilot can be realised in a further preferred embodiment, characterized in that the first phase-shifting circuit precedes the first input of the pilot detector and a second phase-shifting circuit is arranged between the signal generator and the second input of the pilot detector for a 90° phase shift of the local auxiliary pilot, the output signal of the first phase-shifting circuit being substantially in phase or in anti-phase at the frequency of the local auxiliary pilot with respect to the local auxiliary pilot at the output of the second phase-shifting circuit.

The invention will be described in greater detail with reference to the sole Figure shown in the drawing.

The Figure shows an arrangement comprising a phase-locked loop 2 to 6 and a pilot detection device 8 to 10, a low-pass filter member 11, a level detector 12 and a signal generator 7 for generating a local auxiliary pilot. The phase-locked loop 2 to 6 has a signal input 1 to which a modulated or unmodulated RF or IF input signal is applied. The signal input 1 is coupled to a phase detector 2, a loop filter 3, an amplifier 4, an adder stage 5 and a controlled oscillator 6. In the phase-locked state of the loop phase differences deviating from 90° between the oscillator signal from the controlled oscillator 6 applied to the phase detector 2 on the one hand and the carrier of the input signal applied to the input 1 on the other hand are negatively fed back in the loop. This results in a frequency and phase synchronization of said oscillator signal with the carrier of the input signal. If the loop is outside its locking range, the oscillator frequency deviates from the frequency of the input carrier by a value which is larger than the capture range of the loop.

The local auxiliary pilot supplied by the signal generator 7, also referred to as the original auxiliary pilot, is injected in the signal path of the loop preceding the controlled oscillator 6 by adding this original auxiliary pilot to the loop signal in the adder stage 5 arranged between the amplifier 4 and the controlled oscillator 6. As a result, the oscillator signal is modulated in frequency or phase with the auxiliary pilot (also referred to as angle modulation). In the phase-locked state of the loop a mixing product is formed in the phase detector 2 at a frequency which is equal to the frequency of the local auxiliary pilot and at an amplitude and phase which are characteristic of the amplitude and phase transfer of the controlled oscillator 6 and the phase detector 2 in this state of phase lock. This mixing product, also referred to as return pilot, is applied to an input of the pilot detection device 8 to 10 via the loop filter 3 and the amplifier 4.

The pilot detection device 8 to 10 has first and second phase-shifting circuits 8 and 9 via which the amplifier 4 and the signal generator 7, respectively, are coupled to first and second inputs of a multiplier circuit 10 operating as a pilot detector. The return pilot is applied from the controlled amplifier 4 to the last-

mentioned first input of the pilot detector 10 via the first phase-shifting circuit 8 and the original auxiliary pilot is applied to the second input of the pilot detector 10 via the second phase-shifting circuit 9. The second phase-shifting circuit 9 realises a 90° phase shift of the original auxiliary pilot. An output of the multiplier circuit 10 is coupled to a level detector 12 via the low-pass filter member 11. In the phase-locked state of the loop the auxiliary pilot undergoes a phase shift from the input of the adder circuit 5 to the output of the amplifier 4, which phase shift is dependent on the phase transfer of the loop at the frequency of the local auxiliary pilot.

In the embodiment shown a synchronous amplitude detection of the return pilot is realised by causing the two pilot signals applied to the multiplier circuit 10 to be mutually in phase or in anti-phase. To this end the original auxiliary pilot is shifted 90° in phase in the second phase-shifting circuit 9 before it is applied to said second input of the pilot detector 10 and the phase shift realised in the first phase-shifting circuit 8 is chosen to be such that, together with the phase shift occurring in the loop at the auxiliary pilot frequency, it is either equal to the phase of the auxiliary pilot applied to the second input of the synchronous detector 10, or differs 180° therefrom.

The amplitude of the return pilot becomes available in the form of a dc component at the output of the pilot detector 10 and is applied to the level detector 12 after low-pass selection in the low-pass filter member 11. The level detector 12 has a threshold value which is chosen to be such that it is exceeded by said dc component in the phase-locked state of the loop. In that case the level detector 12 supplies a locking indication signal having a given binary value, for example 1, which can be further used (not shown) for adjusting, for example, the loop gain to a given value or for indicating the state of phase lock.

Outside the locking range the amplitude of the return pilot is zero or substantially zero so that no dc component exceeding the last-mentioned threshold value of the level detector 12 is obtained at the output of the pilot detection device 8-10. The level detector then supplies a locking indication signal having the other binary value, i.e. 0 in this case.

In a practical embodiment the loop bandwidth was 75 kHz, the auxiliary pilot was 38 kHz and the bandwidth of the low-pass filter was 50 Hz. A Schmitt trigger was used as a level detection circuit.

It will be evident that the inventive idea is applicable in an embodiment which differs from the embodiment shown. For example, the amplifier 4 and one of the two said phase-shifting circuits may be dispensed with, the frequency of the local auxiliary pilot may be chosen outside the 3 dB loop passband.



Claims

1. An arrangement comprising a phase-locked loop (2, 3, 4, 6) whose signal path incorporates a phase detector (2), a loop filter (3) and a controlled oscillator (6), and a pilot generator (7) for generating a local auxiliary pilot which is applied to the controlled oscillator (6), and a pilot detector (8, 9, 10) an input of which is coupled to the signal path of the loop and an output of which is coupled to a level detector (12) via a filter member (11), wherein the pilot detector comprises a multiplier circuit (10) for synchronous detection of the auxiliary pilot, a first input of the multiplier circuit (10) being coupled to the signal path of the loop between the phase detector (2) and the controlled oscillator (6), and a second input of the multiplier circuit (10) being coupled to the pilot generator (7), an output of the multiplier circuit (10) being coupled to the filter member (11), comprising a low-pass filter, characterized in that a first phase-shifting circuit (8) precedes one of the two first and second inputs of the multiplier circuit (10).
2. An arrangement comprising a phase-locked loop (2, 3, 4, 6) as claimed in Claim 1, characterized in that the frequency of the local auxiliary pilot is located within the passband of the loop, the pilot detector (8, 9, 10) being arranged to effect a substantially synchronous amplitude detection of the local auxiliary pilot supplied to the first input of the multiplier circuit (10).
3. An arrangement comprising a phase-locked loop (2, 3, 4, 6) as claimed in Claim 2, characterized in that the first phase-shifting circuit (8) precedes the first input of the multiplier circuit (10) and a second phase-shifting circuit (9) is arranged between the signal generator (7) and the second input of the multiplier circuit (10) for a 90° phase shift of the local auxiliary pilot, the output signal of the first phase-shifting circuit (8) being substantially in phase or in anti-phase at the frequency of the local auxiliary pilot with respect to the local auxiliary pilot at the output of the second phase-shifting circuit (9).

Patentansprüche

1. Schaltungsanordnung mit einer phasenverriegelten Schleife (2, 3, 4, 6), deren Signalstrecke einen Phasendetektor (2), ein Schleifenfilter (3) und einen geregelten Oszillator (6) aufweist, sowie mit einem Pilotgenerator (7) zur Erzeugung eines örtlichen Hilfspilotsignals, das dem geregelten Oszillator (6) zugeführt wird, und mit einem Pilotdetektor (8, 9, 10), von dem ein Eingang

mit der Signalstrecke der Schleife und ein Ausgang über ein Filterelement (11) mit einem Pegeldetektor (12) gekoppelt ist, wobei der Pilotdetektor einen Multiplizierkreis (10) aufweist zur synchronen Detektion des Hilfspilotsignals, wobei ein erster Eingang des Multiplizierkreises (10) mit der Signalstrecke der Schleife zwischen dem Phasendetektor (2) und dem geregelten Oszillator (6) gekoppelt ist, und wobei ein zweiter Eingang des Multiplizierkreises (10) mit dem Pilotsignalgenerator (7) gekoppelt ist, wobei ein Ausgang des Multiplizierkreises (10) mit dem Filterelement (11) gekoppelt ist, das ein Tiefpaßfilter aufweist, dadurch gekennzeichnet, daß eine erste Phasenverschiebungsschaltung (8) dem ersten oder dem zweiten Eingang des Multiplizierkreises (10) vorgeschaltet ist.

2. Schaltungsanordnung mit einer phasenverriegelten Schleife (2, 3, 4, 6) nach Anspruch 1, dadurch gekennzeichnet, daß die Frequenz des örtlichen Hilfspilotsignals innerhalb des Durchlaßbandes der Schleife liegt, wobei der Pilotdetektor (8, 9, 10) dazu vorgesehen ist, eine nahezu synchrone Amplitudendetektion des dem ersten Eingang des Multiplizierkreises (10) zugeführten örtlichen Hilfspilotsignals durchzuführen.
3. Schaltungsanordnung mit einer phasenverriegelten Schleife (2, 3, 4, 6) nach Anspruch 2, dadurch gekennzeichnet, daß die erste Phasenverschiebungsschaltung (8) dem ersten Eingang des Multiplizierkreises (10) vorgeschaltet ist und eine zweite Phasenverschiebungsschaltung (9) zwischen dem Signalgenerator (7) und dem zweiten Eingang des Multiplizierkreises (10) für eine 90° Phasendrehung des örtlichen Hilfspilotsignals angeordnet ist, wobei das Ausgangssignal der ersten Phasenverschiebungsschaltung (8) im wesentlichen gleichphasig ist oder gegenphasig ist mit der Frequenz des örtlichen Hilfspilotsignals gegenüber dem örtlichen Hilfspilotsignal am Ausgang der zweiten Phasenverschiebungsschaltung (9).

Revendications

1. Dispositif comprenant une boucle à verrouillage de phase (2, 3, 4, 6) dont le chemin de signal contient un détecteur de phase (2), un filtre de boucle (3) et un oscillateur commandé (6), ainsi qu'un générateur de signal pilote (7) pour générer un signal pilote auxiliaire local qui est appliqué à l'oscillateur commandé (6) et un détecteur de signal pilote (8, 9, 10) dont une entrée est connectée au chemin de signal de la boucle et dont une sortie est connectée à un détecteur de niveau



(12) via un élément de filtrage (11), dans lequel le détecteur de signal pilote comprend un circuit multiplicateur (10) pour la détection synchrone du signal pilote auxiliaire, une première entrée du circuit multiplicateur (10) étant connectée au chemin de signal de la boucle entre le détecteur de phase (2) et l'oscillateur commandé (6), une deuxième entrée du circuit multiplicateur (10) étant connectée au générateur de signal pilote (7), une sortie du circuit multiplicateur (10) étant connectée à l'élément de filtrage (11) comprenant un filtre passe-bas, caractérisé en ce qu'un premier circuit de décalage de phase (8) précède une des deux première et deuxième entrées du circuit multiplicateur (10).

5

10

15

2. Dispositif comprenant une boucle à verrouillage de phase (2, 3, 4, 6) selon la revendication 1, caractérisé en ce que la fréquence du signal pilote auxiliaire local se situe dans la bande passante de la boucle, le détecteur de signal pilote (8, 9, 10) étant agencé pour effectuer une détection d'amplitude sensiblement synchrone du signal pilote auxiliaire local délivré à la première entrée du circuit multiplicateur (10).

20

25

3. Dispositif comprenant une boucle à verrouillage de phase (2, 3, 4, 6) selon la revendication 2, caractérisé en ce que le premier circuit de décalage de phase (8) précède la première entrée du circuit multiplicateur (10) et un deuxième circuit de décalage de phase (9) est agencé entre le générateur de signal (7) et la deuxième entrée du circuit multiplicateur (10) pour un décalage de phase de 90° du signal pilote auxiliaire local, le signal de sortie du premier circuit de décalage de phase (8) étant sensiblement en phase ou en opposition de phase, à la fréquence du signal pilote auxiliaire local, par rapport au signal pilote auxiliaire local à la sortie du deuxième circuit de décalage de phase (9).

30

35

40

45

50

55

5