

Description

The invention relates to a synchronized phase-lock-loop circuit. In particular, the invention is useful in synchronizing a horizontal oscillator of a television receiver by a signal obtained from, for example, a multi-head video tape recorder (VTR).

In, for example, a two-head magnetic recording and reproducing apparatus, the video signal is alternately recorded onto and reproduced by two rotating heads from tracks oblique with respect to the longitudinal direction of the magnetic tape. The two heads are disposed apart from each other by 180° . The rotation of the rotary heads is controlled so as to rotate one-half revolution in one vertical field period. When the first head reproduces a video signal that is associated with a picture field F_1 such as shown in FIGURE 2a, no video information is obtained from the second head. On the other hand, when the second head reproduces a video signal of an immediately subsequent picture field F_2 , such as shown in FIGURE 2b, no video information is obtained from the first head. The two video signals are combined to form a TV or video signal 100 of FIGURE 2c where corresponding sync pulses h_{s1} of FIGURES 2a are shown, schematically, in solid narrow lines and corresponding sync pulses h_{s2} of FIGURE 2b are shown in solid thick lines. It should be understood that during each period H of FIGURES 2a, 2b and 2c, the corresponding video signal also includes a corresponding active video portion that contains picture information that is not shown.

Because of, for example, the mechanical arrangement of the heads and tape in the VTR, the horizontal sync pulses h_{s2} reproduced by the second head may be phase-shifted by a phase shift ϕ . Phase shift ϕ corresponds to a fraction of a horizontal period H , as shown in FIGURE 2c, relative to, for example, horizontal sync pulses h_{s1} reproduced by the first head. The frequency f_H of each of sync pulses h_{s1} and h_{s2} associated with each of the heads is substantially the same.

In, for example, a television receiver that is used for displaying the picture information obtained from the video signal of a VTR, the horizontal sync pulses of FIGURES 2a and 2b associated with alternate picture fields F_1 and F_2 are alternately coupled via signal 100 of FIGURE 2c to a synchronizing input terminal of a phase-lock-loop circuit (PLL). The PLL includes, for example, a horizontal oscillator of a horizontal deflection circuit of the receiver which is synchronized by the sync pulses. During the greater portion of each corresponding vertical interval V , the output signal of the oscillator is in phase with the corresponding sync pulses h_{s1} and h_{s2} .

Such PLL may be, typically, designed to have a relatively slow tracking response time to the horizontal sync pulses h_{s1} or h_{s2} , by using a loop filter having a relatively large time constant. The large time constant prevents a noise related signal, that may be included in the horizontal sync pulses of signal 100 of FIGURE 2c, from substantially affecting the phase of the PLL output signal. However, such large time constant, disadvantageously, prevents the PLL from tracking rapid changes in the aforementioned phase shift ϕ . Phase shift ϕ occurs after, for example, time T_1 of FIGURE 2c, when sync pulses h_{s1} associated with the first head are, for example, switched-out and pulses h_{s2} associated with the second head are switched-in, within signal 100. If such slow response time is not speeded-up after instant T_1 , a distortion in the picture formed by TV video signal 100 may occur. For example, a picture that is supposed to contain a straight vertical bar will, contain, as a result of the slow tracking, a bar that is vertical but that is slightly bent, or curved at, for example, the top of the picture. Such bending occurs because of a transient change in the frequency of the output signal of the horizontal oscillator of the PLL. The change in the frequency after instant T_1 occurs in order to track pulses h_{s2} in signal 100 of FIGURE 2c that are phase shifted by phase shift ϕ relative to the phase of the output signal of the oscillator.

Phase shift ϕ of the sync pulses changes from a steady state value that is, for example, approximately 0° prior to instant T_1 , to a value ϕ_0 , after instant T_1 . As is well known, a transient oscillator response is produced by the PLL in order to track or effectuate the corresponding phase shift ϕ in the output signal. As part of the response process, the frequency of the oscillator output signal may momentarily deviate from the steady state value f_H and then return to its value f_H , that existed prior to such deviation.

In one prior art circuit, the problem associated with tracking phase shift ϕ by the output signal of the oscillator is eliminated or reduced by using a variable time constant in the loop filter of the PLL. When the video signal is obtained from the VTR, a user will activate a manually operated switch that causes a reduction in the time constant of loop filter of the PLL. A disadvantage of such solution is that the user must remember to operate the switch.

In another prior art circuit, the time constant of the loop filter of PLL is automatically reduced only during vertical retrace, to speed up the PLL response time when the switching in and out of the corresponding groups of sync pulses h_{s1} and h_{s2} occurs. However, this circuit may be subject to noise during vertical retrace.

In accordance with an aspect of the invention, a phase-lock-loop circuit of a television apparatus

includes a source of synchronizing input signal at a given phase. A controllable generator responsive to the input signal generates a periodic output signal at a frequency that is related to the frequency of the input signal and at a phase that is controlled in accordance with the given phase of the input signal. A phase detector responsive to the output and input signals produces a signal that is indicative of a phase difference therebetween. A low-pass filter responsive to the phase difference indicative signal produces a first signal that is coupled to the generator to form a feedback loop path for controlling the phase of the output signal. When a change between the given phase of the input signal and the phase of the output signal occurs, the first signal varies to cause a corresponding change in the phase of the output signal in a manner that reduces the phase difference between the input and output signals. In this way the output signal is synchronized to the input signal. A second signal is generated when the change in the phase difference indicative signal occurs that persists for a predetermined interval. The second signal is coupled to the generator to cause at least a portion of the change in the phase of the output signal that synchronizes the output to the input signal.

In the drawing:

FIGURE 1 illustrates a block diagram of a circuit embodying an aspect of the invention; and

FIGURES 2a-2g illustrate timing diagrams associated with the circuit of FIGURE 1.

FIGURE 1 illustrates a block diagram of a phase lock loop (PLL) 20, and of a loop filter bypassing arrangement 120, embodying the invention. PLL 20 includes a counter 21 that produces a count or an output word CT at a port 21b of counter 21. Word CT is coupled to a horizontal deflection circuit 401 to control the timing of corresponding horizontal deflection cycles. Arrangement 120 and PLL 20 may be utilized in television circuitry other than the horizontal deflection circuit, in situations where synchronization is required. Counter 21 has the analogous function of a VCO of a conventional analog type PLL that generates an output signal at, for example, the frequency f_H and that is synchronized to a horizontal sync signal. Output word CT of counter 21 is incremented after each leading edge of a clock CK having a period t_{CK} . Counter 21 counts up, or changes state from an initial state that corresponds with, for example, word CT = 1, each time clock CK occurs until it is reset to the initial state.

Word CT is also coupled to an input port 201c of an adder 201 that sums word CT with a phase modifying word VCRM0D to produce at an output port 201a of adder 201 a word CTA, representing the state of counter 21 as modified by word VCRM0D. A word PERIOD, that is analogous to a

control voltage of a VCO of the conventional PLL, is coupled to a comparator 200 that compares the present value of word CTA to that of word PERIOD and generates a pulse RESET at an input terminal 21a of counter 21 that initializes counter 21 when word PERIOD is equal to word CTA. Pulse RESET causes counter 21 to reset to the initial value that, for example, corresponds with word CT = 1. Each word CT supplies in a given sequence N, that occurs between successive pulses RESET, the present count, or state, of counter 21. The rate by which, for example, word CT = 1 recurs defines the frequency of word CT that is analogous to the frequency of the output signal of a VCO of a conventional PLL. Thus, word PERIOD controls, via pulse RESET, the period, frequency and phase of word CT. The length of the period of word CT that is controlled by word PERIOD is defined by the number of clock CK periods t_{CK} that are included between successively occurring pulses RESET. As described later on, when head switching in the VTR occurs, the value of word VCRM0D is changed, to produce an abrupt change in the phase of word CT.

Baseband television signal 100 of FIGURE 2c, which may be of any one of the various television signal formats, is digitized in an analog-to-digital converter 61 of FIGURE 1 and then low-pass filtered in a low-pass filter 25. The low-pass filtered signal is coupled to a sync separator 60 that generates a digitized signal 100a that includes horizontal sync pulses H_s .

Horizontal sync pulses H_s having a period H are coupled to an input port of a phase detector 202 of FIGURE 1. An example of such phase detector that is included in a digital PLL is described in U.S. Patent No. US-A-4639780, entitled TELEVISION SYNCHRONIZING APPARATUS, issued to D. H. Willis on 27 January 1987.

A decoder 23 generates timing and control signals DC_n and a pulse MS when predetermined corresponding values of word CT are detected. Pulse MS is indicative of the phase of word CT. As described in the Willis patent, when PLL 20 is phase-locked to sync pulses H_s , the leading edge of each pulse MS that is coupled to phase detector 202 occurs, for example, substantially coincidentally with the last clock CK edge that occurs before the center of the corresponding sync pulse H_s .

Phase detector 202 generates a phase difference word PH, in accordance with a phase difference between sync pulses H_s and word CT. Phase difference word PH, that is analogous to an output of a phase detector of a conventional PLL, is coupled to a lowpass, or loop filter 33, that is analogous to the loop filter of a conventional PLL. Loop filter 33 generates word PERIOD, that controls the phase and frequency of word CT, by

summing up successively generated phase words PH. Each of detector 202 and filter 33, that utilize digital techniques, is controlled by a corresponding control signal DC_n that is, like pulse MS, produced in accordance with timing information obtained from word CT. For example, the corresponding control signal DC_n that is coupled to detector 202 determines the time when word PH is updated.

In steady state operation of PLL 20, each phase difference word PH of phase detector 202 is substantially zero. This maintains word PERIOD, in steady state, substantially constant. It should be understood that in other embodiments of the invention, that are not shown in the FIGURES, the PLL may be designed such that, in steady state operation, the phase detector output word is nonzero, in order to maintain word PERIOD constant.

During transient operation, phase difference word PH varies. The variation of word PH causes a change in word PERIOD that, in turn, causes a phase shift in word CT. The phase shift synchronizes word CT to sync pulse H_s .

FIGURES 2a-2g illustrate timing diagrams useful in explaining the operation of loop filter bypassing arrangement 120 and of PLL 20 of FIGURE 1. Similar symbols and numerals in FIGURES 1 and 2a-2g illustrate similar items or functions.

FIGURE 2c, that was mentioned before, also illustrates sync pulses h_{s1} and h_{s2} of sync pulses H_s of FIGURE 1, when signal 100 originates in a VTR, that is not shown in the FIGURES. When pulses h_{s1} of FIGURE 2c are produced by the first head of the VTR, that occurs prior to instant T_1 , a given pulse h_{s1} is separated from the next one by an interval that is equal to period H.

Immediately after instant T_1 of FIGURE 2c, a given pulse h_{s2} , drawn in thick lines in FIGURE 2c, that originates from the second head of the VTR, is separated from, for example, the following pulse h_{s2} by an interval that is also equal to period H. However, the pulse h_{s2} that occurs immediately after constant T_1 is phase-shifted. The amount of phase shift ϕ is equal to, for example, the value ϕ_0 relative to the pulse h_{s1} that occurs immediately before instant T_1 .

FIGURE 2d illustrates, schematically, the timing of a predetermined word CT_1 having a predetermined value. Illustratively, each time word CT_1 occurs, a given sequence N ends, that is associated with a corresponding cycle of word CT of counter 21 of FIGURE 1, and the next subsequent sequence begins. Each word CT_1 of FIGURE 2d that occurs prior to instant T_1 is in phase with the corresponding pulse h_{s1} of FIGURE 2c. Therefore, phase difference word PH of FIGURE 2g is zero. After instant T_1 , pulses h_{s2} are phase shifted relative to the corresponding words CT_1 of FIGURE 2d. Until instant T_4 , when word CT_1 is caused to

be in phase again with pulses h_{s2} , due to operation of PLL 20 and arrangement 120 of FIGURE 1, word PH of FIGURE 2g contains the value ϕ_0 . Thus, word PH of FIGURE 2g may be illustrated as, for example, a pulse having a leading edge 350 that occurs at an instant T_2 after instant T_1 and an amplitude that corresponds to the magnitude of word PH. Word PH changes slowly in value from time T_2 to time T_4 due to the slow response time of PLL 20.

As described later on, except for a short interval when the VTR head switching occurs, word VCRM0D of FIGURE 1 contains a constant such as, illustratively, zero. If word VCRM0D is zero, counter 21 is reset and the next word CT of counter 21 is equal to 1, the initial counting state, when word CT of counter 21 is equal to word PERIOD. Thus, as explained before, word PERIOD expresses, in multiples of clock CK periods t_{CK} the length of sequence N of counter 21. It should be understood that the length of sequence N may be a noninteger multiple of period t_{CK} . When the VTR head switching occurs, word VCRM0D will assume a nonzero value that will cause an abrupt phase shift of word CT, with the phase shift having the magnitude ϕ_0 .

For a given value of word PERIOD, the phase of words CT can be changed by varying the value of word VCRM0D from its steady state value that is zero. Word VCRM0D that is different from zero occurs, as described later on, when the VTR head switching occurs. The nonzero value of word VCRM0D will cause a corresponding change of the value of word CTA, and therefore of the time within sequence N of counter 21 when word CTA becomes equal to word PERIOD. In such circumstances, pulse RESET, that is generated when word CTA is equal to word PERIOD, produces an abrupt phase shift in word CT that is in accordance with the value of word VCRM0D.

In accordance with a further aspect of the invention, as described later on, a value of phase modifying word VCRM0D of FIGURE 2e that is representative of the value ϕ_0 is applied to port 201b of adder 201 by loop filter bypassing arrangement 120 to cause an abrupt change in the phase or word CT such as, for example, word CT_1 of FIGURE 2d that occurs after instant T_4 . The change in phase or word CT_1 is illustratively, equal to the value ϕ_0 so as to cause word CT to be immediately in phase with the corresponding pulse h_{s2} of FIGURE 2c. Except for a short interval during the vertical scanning interval, when word VCRM0D causes the change in the phase of word CT_1 , word VCRM0D is zero. Without the operation of arrangement 120, when the phase of pulses H_s change, PLL 20 would have adjusted the phase of words CT_1 of FIGURE 2d to be equal to, for example, that

of corresponding pulses h_{s2} of FIGURE 2c by varying word PERIOD of FIGURE 1 in a relatively slow transient manner that is a function of the response time of PLL 20 and that is determined by filter 33. The elimination or reduction of the slow transient variation in word PERIOD is desirable for preventing such long settling time of PLL 20 that may cause picture distortion, as described before. When the transient variation in word PERIOD is reduced, the phase of, for example, word CT_1 of FIGURE 2d tracks in a fast manner the above-mentioned phase shift ϕ having the value ϕ_0 that is caused by the head switching in the VTR. Advantageously, the phase change by the value ϕ_0 , that is caused by applying the nonzero value of word VCRM0D of FIGURE 2e, prevents the occurrence of the undesirable long transient variation in word PERIOD of FIGURE 1.

Word VCRM0D of FIGURE 1 is generated in loop filter bypassing arrangement 120, embodying another aspect of the invention, as will now be described. In arrangement 120, phase difference word PH of phase detector 202 of PLL 20 is coupled to an input port 300a of an averager 300 that generates, in a conventional manner, one corresponding word PH_{AV} in each horizontal period H. Word PH_{AV} is representative of a running average of, for example, three lastly received words PH that occurred in corresponding three preceding periods H. Thus, averager 300 operates as a lowpass filter, but one having a cutoff frequency that is substantially higher than that of filter 33.

Each word PH_{AV} is stored, in the corresponding period H, in a register 301 under the control of the corresponding control signal DC_n to produce a word DIFFD1. In the immediately following period H, word DIFFD1 is transferred to, and stored in a register 302 to produce a word DIFFD2 that is stored under the control of the corresponding control signal DC_n . Thus, words DIFFD1 and DIFFD2 represent, at a given instant, a pair of running averages of words PH that are separated by horizontal period H. Words DIFFD1 and DIFFD2 are coupled to corresponding input ports of a subtractor 303 that produces a word 303a that is representative of the difference between the pair. Word 303a that is indicative of the occurrence of a change in phase word PH, is coupled to an arrangement 304 that produces the absolute value of word 303a. When the absolute value of word 303a, that is indicative of the magnitude of the phase change, or the rate of change of word PH, exceeds a threshold level indicative signal REF, a comparator 305 produces a logic signal PHCNGE in a TRUE state. Signal PHCNGE is used for detecting the time within the vertical scanning interval when, as a result of head switching in the VTR, word VCRM0D is to be generated at the nonzero value

to cause the abrupt phase shift of word CT_1 of FIGURE 2d.

Signal PHCNGE is coupled to a microprocessor 306 of FIGURE 1 that tests for the occurrence of signal PHCNGE = TRUE. The condition of signal PHCNGE = TRUE, that occurs after instant T_2 of FIGURE 2f, is indicative of phase shift ϕ having a magnitude that exceeds the threshold level represented by signal REF of FIGURE 1. A change in phase shift ϕ that is smaller, will not activate arrangement 120. Under these circumstances, it is the transient change in word PERIOD that will cause PLL 20 to be synchronized to signal H_s , in accordance with the response that is determined by filter 33. If signal PHCNGE = TRUE is followed by signal PHCNGE = FALSE, there is an indication of a stable phase shift. After detecting the condition, signal PHCNGE = TRUE, microprocessor 306 tests signal PHCNGE for detecting the occurrence of signal PHCNGE = FALSE. Signal PHCNGE = FALSE is indicative of a stable phase shift ϕ having a rate of change that is lower than a second threshold level. The second threshold level may be smaller than, or equal to, the threshold level represented by signal REF.

Assume the phase shift ϕ of FIGURE 2g stabilizes immediately after the change at instant T_2 . Consequently, after a corresponding number of periods H that is determined by averager 300 of FIGURE 1, word PH_{AV} will have a constant value. Because word 303a represents a change in words PH_{AV} , word 303a, that occurs after word PH_{AV} becomes constant, will be zero, such as at instant T_3 of FIGURE 2f. Thus, the condition, signal PHCNGE = FALSE, that occurs after instant T_3 is indicative of phase shift ϕ that is constant, or stable. Phase shift ϕ that is substantially constant is caused by, for example, the VTR head switching, as described before. A varying phase shift may occur when PLL 20 of FIGURE 1 is not in steady state operation, such as during tracking of pulses H_s .

After instant T_3 of FIGURE 2f, when the condition, signal PHCNGE = FALSE, is detected, microprocessor 306 of FIGURE 1 will supply word VCRM0D at port 201b of adder 201, thereby bypassing loop filter 33. Word VCRM0D has a value that, as described later on, will cause the phase of word CT_1 of FIGURE 2d to change by the value ϕ_0 at instant T_4 . Therefore, after the phase change, word CT_1 will again be in phase with pulses h_{s2} of FIGURE 2c due to the operation of arrangement 120 of FIGURE 1 that is outside the feed back loop of PLL 20.

Microprocessor 306 of FIGURE 1 supplies the value or word VCRM0D in a manner that is now described. During steady state operation, microprocessor 306 generates a signal CNT that causes word PH to be stored in a register 400 to produce

a word PASTDIFF. Word PASTDIFF contains the value of word PH when PLL 20 operates in steady state operation. Word DIFFD1, that is representative of phase shift ϕ , and word PASTDIFF are coupled to corresponding ports of a subtractor 308 that produces, at an output port 308a, a word VCRMADA that is equal to the difference between words DIFFD1 and PASTDIFF. Word VCRMADA is stored in a register 307 under the control of decoder 23 to produce a word VCRMADB. Word VCRMADB is indicative of the difference between the value of word PH, during transient state, and the value of word PH, during steady state. For a typical design of PLL 20, word PASTDIFF is, illustratively, close to zero in steady state operation. Thus, word VCRMADB is indicative of the magnitude and polarity of phase shift ϕ of FIGURE 2g.

Immediately after detection of the condition, signal PHCNGE = FALSE, that follows the occurrence of the condition signal PHCNGE = TRUE, the phase information that is contained in word VCRMADB is used by microprocessor 306 for producing word VCRMOM of FIGURE 1. Word VCRMOM is coupled to adder 201 during an interval that is determined by microprocessor 306 in accordance with the timings of word CT that is coupled to microprocessor 306. Word VCRMOM that is produced by microprocessor 306 causes, in an abrupt manner, a phase shift in, illustratively, word CT₁ of FIGURE 2d that is equal to the value ϕ_0 . Thus, immediately after instant T₄, each word CT₁ is caused to be in phase with the corresponding pulse h₂₂ of FIGURE 2c by the operation of phase modifying word VCRMOM of FIGURE 2e.

After effectuating the abrupt phase shift ϕ_0 in word CT₁ of FIGURE 2d that occurs at instant T₄, word VCRMOM of FIGURE 2e becomes zero again. Throughout the remaining portion of each vertical scanning interval V, phase shift ϕ remains illustratively, zero so as not to affect the operation of PLL 20 of FIGURE 1.

In accordance with yet another aspect of the invention, the phase shift in word CT₁ of FIGURE 2d at instant T₄, that immediately follows the VTR head switching and that is caused by word VCRMOM of FIGURE 2e, causes phase word PH of FIGURE 2g to become immediately close to zero. Word PH of FIGURE 1 becomes immediately close to zero because arrangement 120 causes the phase of word CT to become immediately equal to that of sync pulse H_s. Word PH of FIGURE 2 that becomes immediate close to zero by the operation of arrangement 120 prevents the occurrence of a long transient state that is undesirable in word PERIOD, as described before.

The change in phase of words CT may alternatively be accomplished gradually in discrete steps over a few periods H. When such phase

change is done in a gradual manner, word VCRMOM is supplied with corresponding values during several periods H. The control over the value and timing of word VCRMOM during each of the several periods H is accomplished by microprocessor 306.

After the change in the phase of word CT₁ at instant T₄ of FIGURE 2d, each word CT₁ is in phase with the corresponding pulse h₂₂ of FIGURE 2c. Each word CT₁ of FIGURE 2d remains in phase until after an instant T₅ when the next VTR head switching occurs. After instant T₅, the phase of word CT₁ of FIGURE 2d relative to the corresponding pulse h₂₁ of FIGURE 2c changes in a manner that is similar to that occurring after instant T₁ but in an opposite direction. Consequently, arrangement 120 of FIGURE 1 supplies word VCRMOM at a value that causes a phase shift in word CT₁ of FIGURE 2d in a way similar to that described before.

It should be understood that microprocessor 306 of FIGURE 1 may be responsive to a vertical signal V_s generated by separator 60 for modifying word VCRMOM only during vertical blanking when the VTR head switching may occur.

In arrangement 120, decoder 23 generates corresponding control signals DC_n that control averager 300 and register 301, 302 and 307. The timings of control signals DC_n are determined in accordance with the timings of word CT. It should be understood that in another embodiment of the invention that is not shown in the FIGURES, a microprocessor that is coupled to receive horizontal sync pulse H_s may perform the entire operation of arrangement 120 and/or generate the control signals that control the PLL.

In the event that the phase of pulses H_s of FIGURE 1 is constant but PLL 20 is not locked-in the pulses H_s, such as at start-up, the condition, signal PHCNGE = TRUE, may be detected by microprocessor 306 as long as PLL 20 is not locked-in. When lock-in occurs, the condition, signal PHCNGE = FALSE, is detected. However, at that time, word VCRMADB, representing a steady state phase difference, unlike in the situation discussed before, is already zero. Therefore, word VCRMOM will remain unmodified at the value zero. Thus, advantageously, arrangement 120 may be designed in such a way that it does not affect PLL 20 unless a stable phase shift occurs in pulses H_s. Such stable phase shift may be caused, for example, by the switching of the heads in the VTR.

Claims

1. A phase-lock-loop circuit of a television apparatus, comprising:
 - a source (60) of a synchronizing input sig-

a word PASTDIFF. Word PASTDIFF contains the value of word PH when PLL 20 operates in steady state operation. Word DIFFD1, that is representative of phase shift ϕ , and word PASTDIFF are coupled to corresponding ports of a subtractor 308 that produces, at an output port 308a, a word VCRMODA that is equal to the difference between words DIFFD1 and PASTDIFF. Word VCRMODA is stored in a register 307 under the control of decoder 23 to produce a word VCRMODB. Word VCRMODB is indicative of the difference between the value of word PH, during transient state, and the value of word PH, during steady state. For a typical design of PLL 20, word PASTDIFF is, illustratively, close to zero in steady state operation. Thus, word VCRMODB is indicative of the magnitude and polarity of phase shift ϕ of FIGURE 2g.

Immediately after detection of the condition, signal PHCNGE = FALSE, that follows the occurrence of the condition signal PHCNGE = TRUE, the phase information that is contained in word VCRMODB is used by microprocessor 306 for producing word VCRMOD of FIGURE 1. Word VCRMOD is coupled to adder 201 during an interval that is determined by microprocessor 306 in accordance with the timings of word CT that is coupled to microprocessor 306. Word VCRMOD that is produced by microprocessor 306 causes, in an abrupt manner, a phase shift in, illustratively, word CT₁ of FIGURE 2d that is equal to the value ϕ_0 . Thus, immediately after instant T₄, each word CT₁ is caused to be in phase with the corresponding pulse h_{s2} of FIGURE 2c by the operation of phase modifying word VCRMOD of FIGURE 2e.

After effectuating the abrupt phase shift ϕ_0 in word CT₁ of FIGURE 2d that occurs at instant T₄, word VCRMOD of FIGURE 2e becomes zero again. Throughout the remaining portion of each vertical scanning interval V, phase shift ϕ remains illustratively, zero so as not to affect the operation of PLL 20 of FIGURE 1.

In accordance with yet another aspect of the invention, the phase shift in word CT₁ of FIGURE 2d at instant T₄, that immediately follows the VTR head switching and that is caused by word VCRMOD of FIGURE 2e, causes phase word PH of FIGURE 2g to become immediately close to zero. Word PH of FIGURE 1 becomes immediately close to zero because arrangement 120 causes the phase of word CT to become immediately equal to that of sync pulse H_s. Word PH of FIGURE 2 that becomes immediately close to zero by the operation of arrangement 120 prevents the occurrence of a long transient state that is undesirable in word PERIOD, as described before.

The change in phase of words CT may alternatively be accomplished gradually in discrete steps over a few periods H. When such phase

change is done in a gradual manner, word VCRMOD is supplied with corresponding values during several periods H. The control over the value and timing of word VCRMOD during each of the several periods H is accomplished by microprocessor 306.

After the change in the phase of word CT₁ at instant T₄ of FIGURE 2d, each word CT₁ is in phase with the corresponding pulse h_{s2} of FIGURE 2c. Each word CT₁ of FIGURE 2d remains in phase until after an instant T₅ when the next VTR head switching occurs. After instant T₅, the phase of word CT₁ of FIGURE 2d relative to the corresponding pulse h_{s1} of FIGURE 2c changes in a manner that is similar to that occurring after instant T₁ but in an opposite direction. Consequently, arrangement 120 of FIGURE 1 supplies word VCRMOD at a value that causes a phase shift in word CT₁ of FIGURE 2d in a way similar to that described before.

It should be understood that microprocessor 306 of FIGURE 1 may be responsive to a vertical signal V_s generated by separator 60 for modifying word VCRMOD only during vertical blanking when the VTR head switching may occur.

In arrangement 120, decoder 23 generates corresponding control signals DC_n that control averager 300 and register 301, 302 and 307. The timings of control signals DC_n are determined in accordance with the timings of word CT. It should be understood that in another embodiment of the invention that is not shown in the FIGURES, a microprocessor that is coupled to receive horizontal sync pulse H_s may perform the entire operation of arrangement 120 and/or generate the control signals that control the PLL.

In the event that the phase of pulses H_s of FIGURE 1 is constant but PLL 20 is not locked-in the pulses H_s, such as at start-up, the condition, signal PHCNGE = TRUE, may be detected by microprocessor 306 as long as PLL 20 is not locked-in. When lock-in occurs, the condition, signal PHCNGE = FALSE, is detected. However, at that time, word VCRMODB, representing a steady state phase difference, unlike in the situation discussed before, is already zero. Therefore, word VCRMOD will remain unmodified at the value zero. Thus, advantageously, arrangement 120 may be designed in such a way that it does not affect PLL 20 unless a stable phase shift occurs in pulses H_s. Such stable phase shift may be caused, for example, by the switching of the heads in the VTR.

Claims

1. A phase-lock-loop circuit of a television apparatus, comprising:
a source (60) of a synchronizing input sig-



nal (H_s) at a given phase;

a controllable generator (21) responsive to said input signal for generating a periodic output signal (CT) at a frequency that is related to the frequency of said input signal and at a phase that is controlled in accordance with said given phase of said input signal;

a phase detector (202) responsive to said output (CT) and input (H_s) signals for producing a signal (PH) that is indicative of a phase difference therebetween;

a low-pass filter (33) responsive to said phase difference indicative signal (PH) for producing, in accordance therewith, a first signal (PERIOD) that is coupled to said generator (21) to form a feedback loop path (20) for controlling said phase of said output signal (CT) such that, when a change between said given phase of said input signal (H_s) and said phase of said output signal (CT) occurs, said first signal (PERIOD) varies to cause a corresponding change in said phase of said output signal (CT) in a manner that reduces the phase difference between said input and output signals for synchronizing said output to said input signal; characterized by

means (120) coupled to said feedback loop path (20) between said phase detector (202) and said low-pass filter (33) for generating, in accordance with the phase difference that is contained in said phase difference indicative signal (PH), a second signal (VCRMOD) when said change in said phase difference indicative signal (PH) persists for a predetermined interval, said second signal (VCRMOD) being coupled to said generator (21) to change the phase of the output signal to produce at least a portion of said change in said phase of said output signal (CT) that is needed to synchronize said output signal (CT) to said input (H_s) signal.

2. A circuit according to Claim 1 characterized in that said second signal (VCRMOD) is generated when a rate of said change in said phase difference indicative signal (PH) is greater than a first predetermined value (REF) such that, after said change in said phase difference indicative signal occurs, said portion of said phase difference indicative signal (PH) becomes smaller than a second predetermined value.
3. A circuit according to Claim 1 characterized in that said input signal (H_s) is at the horizontal deflection frequency.

4. A circuit according to claim 3 characterized in that said second signal generating means (120) is responsive to a signal (V_s) at a vertical rate to generate said second signal (VCRMOD) only during vertical blanking.
5. A circuit according to Claim 1 characterized in that said second signal generating means (120) is responsive to said phase difference indicative signal (PH) that is produced by said phase detector (202) for generating therefrom said second signal (VCRMOD), is coupled to said generator (21) in a manner that bypasses said low-pass filter (33).
6. A circuit according to Claim 1 characterized by, combining means (201) responsive to said first (PERIOD) and second (VCRMOD) signals for combining said first and second signals to produce a third signal (RESET) that is coupled to said generator (21) to control said phase of said output signal (CT) such that said phase of said output signal is simultaneously affected by corresponding values of each of said first (PERIOD) and second (VCRMOD) signals.
7. A circuit according to Claim 1 characterized in that said second signal generating means (120) generates said second signal (VCRMOD) after a change in said given phase of said input signal (H_s) occurs that results in said input signal (H_s) being at a phase that is stable and that is shifted relative to said phase of said output signal (CT).
8. A circuit according to Claim 1 characterized in that said controllable generator (21) comprises sequential means for generating said output signal (CT) in accordance with a sequence of states that change in synchronism with a clock signal (CK) and wherein said second signal (VCRMOD) causes said sequence of states, and the period of said input signal (H_s) which corresponds thereto, to vary in accordance with said second signal (VCRMOD).
9. A circuit according to claim 8 characterized in that when said change in said phase of said output signal (CT) that is caused by said second signal (VCRMOD), occurs, it occurs abruptly and in synchronism with said clock signal (CK).
10. A circuit according to Claim 1 characterized in that said second signal (VCRMOD) causes said change in said phase of said output signal (CT) when said predetermined criterion is detected, by an amount that is related to an



amount by which the phase difference is different from a steady state value of the phase difference.

11. A circuit according to Claim 1 characterized in that said first signal (PERIOD) is indicative of a length of a given period of said output signal (CT), and wherein said first signal (PERIOD) remains substantially unaffected when said change in said phase difference indicative signal (PH) occurs that meets said predetermined criterion.

Patentansprüche

1. Phasenregel-Schaltung (PLL) für ein Fernsehgerät

- mit einer Quelle (60) eines Synchron-Eingangssignales (H_s) einer vorgegebenen Phase;
 - mit einem steuerbaren Generator (21), der abhängig von dem Eingangssignal ist, zum Erzeugen eines periodischen Ausgangssignales (CT) mit einer Frequenz, die Bezug hat zu der Frequenz des Eingangssignales, und mit einer Phase, die steuerbar ist in Übereinstimmung mit der gegebenen Phase des Eingangssignales;
 - mit einem Phasendetektor (202), der abhängig von Ausgangs-(CT) und Eingangs-(H_s) Signalen ist, zum Erzeugen eines Signales (PH), das eine Phasendifferenz zwischen diesen anzeigt;
 - mit einem Tiefpass(-Filter) (33), das abhängig von dem Signal (PH) zur Anzeige der Phasendifferenz ist, zur Erzeugung - in Übereinstimmung damit - eines ersten Signales (PERIOD), das zu dem Generator (21) gekoppelt wird, um einen Rückkopplungs-Weg (20) zum Steuern der Phase des Ausgangssignales (CT) zu bilden, und zwar so, daß bei Auftreten eines Wechsels zwischen der gegebenen Phase des Eingangssignales (H_s) und der Phase des Ausgangssignales (CT) das erste Signal (PERIOD) variiert, um eine entsprechende Änderung in der Phase des Ausgangssignales (CT) in der Weise zu bewirken, daß die Phasendifferenz zwischen den Eingangs- und Ausgangssignalen reduziert wird zur Synchronisation des Ausgangs- auf das Eingangssignal;
- gekennzeichnet durch**
- Mittel (120), die mit dem Rückkopplungs-Weg (20) zwischen dem Phasendetektor (202) und dem Tiefpass (33) gekoppelt

sind, zur Erzeugung - in Übereinstimmung mit der Phasendifferenz, die in dem Signal (PH) zur Anzeige der Phasendifferenz enthalten ist - eines zweiten Signales (VCRMOD), wenn die Änderung in dem Signal (PH), das die Phasendifferenz anzeigt, für ein vorgegebenes Intervall Bestand hat,

- wobei das zweite Signal (VCRMOD) an den Generator (21) gekoppelt wird, um die Phase des Ausgangssignales zu ändern, womit zumindest ein Teil der Änderungen der Phase des Ausgangssignales (CT) bewirkt wird, die benötigt wird zur Synchronisation des Ausgangssignales (CT) mit dem Eingangssignal (H_s).

2. Schaltung nach Anspruch 1, dadurch gekennzeichnet,

daß das zweite Signal (VCRMOD) erzeugt wird, wenn die Änderungs-Rate in dem Signal (PH), das die Phasendifferenz anzeigt, größer ist als ein erster vorgegebener Wert (REF), so daß nach dem Auftreten der Änderung in dem Signal, das die Phasendifferenz anzeigt, der Teil des Signales (PH), das Phasendifferenz anzeigt, geringer wird, als ein zweiter vorbestimmter Wert.

3. Schaltung nach Anspruch 1, dadurch gekennzeichnet,

daß das Eingangssignal (H_s) die Horizontal-Ablenkfrequenz aufweist.

4. Schaltung nach Anspruch 3, dadurch gekennzeichnet,

daß die Mittel (120) zur Erzeugung des zweiten Signales abhängig sind von einem Signal (V_s) mit einer vertikalen Rate zur Erzeugung des zweiten Signales (VCRMOD) nur während der Vertikalaustastung (vertical blanking).

5. Schaltung nach Anspruch 1, dadurch gekennzeichnet,

daß die Mittel (120) zur Erzeugung des zweiten Signales abhängig sind von dem Signal (PH) zur Anzeige der Phasendifferenz, welches von dem Phasendetektor (202) erzeugt wird, zur davon ausgehenden Erzeugung des zweiten Signales (VCRMOD), in einer Weise mit dem Generator (21) gekoppelt ist, die den Tiefpass (33) umgeht (bypassed).

6. Schaltung nach Anspruch 1, dadurch gekennzeichnet,

daß Kombiniermittel (201) vorgesehen sind, die abhängig sind von dem ersten (PERIOD) und zweiten (VCRMOD) Signal zur Kombination der



ersten und zweiten Signale, um ein drittes Signal (RESET) zu erzeugen, das an den Generator (21) gekoppelt wird, um die Phase des Ausgangssignales (CT) so zu steuern, daß die Phase des Ausgangssignales gleichzeitig von den korrespondierenden Werten jedes des ersten (PERIOD) und zweiten (VCRMOD) Signale beeinflusst wird.

7. Schaltung nach Anspruch 1, **dadurch gekennzeichnet**, daß die Mittel (120) zur Erzeugung des zweiten Signales das zweite Signal (VCRMOD) erzeugen, nachdem ein Wechsel in der gegebenen Phase des Eingangssignales (H_s) auftritt, was darin resultiert, daß das Eingangssignal (H_s) eine Phase aufweist, die stabil ist und die relativ zu der Phase des Ausgangssignales (CT) verschoben ist.
8. Schaltung nach Anspruch 1, **dadurch gekennzeichnet**, daß der steuerbare Generator (21) sequentielle Mittel aufweist zur Erzeugung des Ausgangssignales (CT) in Übereinstimmung mit einer Sequenz von Zuständen (states), die synchron mit einem Taktsignal (CK) wechseln, und wobei das zweite Signal (VCRMOD) bewirkt, daß die Folge von Zuständen (sequence of states) und die Periode des Eingangssignales (H_s) - die damit korrespondiert - in Übereinstimmung mit dem zweiten Signal (VCRMOD) variiert.
9. Schaltung nach Anspruch 8, **dadurch gekennzeichnet**, daß, wenn die Änderung (Wechsel) in der Phase des Ausgangssignales (CT), die von dem zweiten Signal (VCRMOD) bewirkt wird, auftritt, sie/er abrupt auftritt und synchron mit dem Taktsignal (CK).
10. Schaltung nach Anspruch 1, **dadurch gekennzeichnet**, daß das zweite Signal (VCRMOD) die Änderung in der Phase des Ausgangssignales (CT) bewirkt, wenn das vorbestimmte Kriterium erfaßt wird, und zwar um einen Betrag, der bezogen ist auf den Betrag, um den die Phasendifferenz sich von dem stationären Wert der Phasendifferenz unterscheidet.
11. Schaltung nach Anspruch 1, **dadurch gekennzeichnet**, daß das erste Signal (PERIOD) eine Länge/Breite einer gegebenen Periode des Ausgangssignales (CT) anzeigt und wobei das erste Signal (PERIOD) im wesentlichen unbeeinflusst davon bleibt, wenn die Änderung des

Signals (PH) zur Anzeige der Phasendifferenz auftritt, die das vorbestimmte Kriterium erfüllt.

Revendications

1. Circuit de boucle verrouillée en phase d'un téléviseur comprenant :
 une source (60) d'un signal d'entrée de synchronisation (H_s) de phase donnée ;
 un générateur commandable (21) sensible audit signal d'entrée pour générer un signal de sortie périodique (CT) à une fréquence qui est reliée à la fréquence dudit signal d'entrée et à une phase qui est commandée selon ladite phase donnée audit signal d'entrée ;
 un détecteur de phase (202) sensible auxdits signaux de sortie (CT) et d'entrée (H_s) pour produire un signal (PH) qui est indicateur d'une différence de phase entre eux ;
 un filtre passe-bas (33) sensible audit signal indicateur de la différence de phase (PH) pour fournir, selon eux, un premier signal (PERIOD) qui est couplé audit générateur (21) pour former un chemin de boucle de réaction (20) destiné à commander ladite phase dudit signal de sortie (CT) de telle sorte que, quand une variation entre ladite phase donnée dudit signal d'entrée (H_s) et ladite phase dudit signal de sortie (CT) se produit, ledit premier signal (PERIOD) varie pour provoquer une variation correspondante de ladite phase dudit signal de sortie (CT) d'une manière qui réduit la différence de phase entre lesdits signaux d'entrée et de sortie afin de synchroniser ledit signal de sortie audit signal d'entrée ; caractérisé par
 des moyens (120) couplés audit chemin de boucle de réaction (20) entre ledit détecteur de phase (202) et ledit filtre passe-bas (33) pour générer, selon la différence de phase qui est contenue dans le signal indicateur de différence de phase (PH), un second signal (VCRMOD) quand ladite variation dudit signal indicateur de différence de phase (PH) persiste pendant un intervalle prédéterminé, ledit second signal (VCRMOD) étant couplé audit générateur (21) pour changer la phase du signal de sortie pour produire au moins une partie dudit changement de ladite phase dudit signal de sortie (CT) qui est nécessaire pour synchroniser ledit signal de sortie (CT) audit signal d'entrée (H_s).
2. Circuit selon la revendication 1, caractérisé en ce que ledit second signal (VCRMOD) est généré quand une valeur de ladite variation dudit signal indicateur de différence de phase (PH) est supérieure à une première valeur prédéterminée (REF) de telle sorte que , après que



ladite variation dudit signal indicateur de différence de phase se produit, ladite partie dudit signal indicateur de différence de phase (PH) devient plus petite qu'une seconde valeur prédéterminée.

3. Circuit selon la revendication 1, caractérisé en ce que ledit signal d'entrée (H_s) est à la fréquence de déflexion horizontale.

4. Circuit selon la revendication 3, caractérisé en ce que lesdits moyens de formation du second signal (120) sont sensibles à un signal (V_s) à une fréquence verticale pour générer ledit second signal (VCRMOD) seulement pendant la suppression trame.

5. Circuit selon la revendication 1, caractérisé en ce que lesdits moyens de formation du second signal (120) sont sensibles audit signal indicateur de différence de phase (PH) qui est produit par ledit détecteur de phase pour générer à partir de lui ledit second signal (VCRMOD), sont couplés audit générateur (21) d'une manière qui contourne ledit filtre passe-bas (33).

6. Circuit selon la revendication 1, caractérisé par des moyens de combinaison (201) sensibles auxdits premier (PERIOD) et second (VCRMOD) signaux pour combiner lesdits premier et second signaux afin de produire un troisième signal (RESET) qui est couplé audit générateur (21) pour commander ladite phase dudit signal de sortie (CT) de telle sorte que ladite phase dudit signal de sortie soit simultanément affectée par les valeurs correspondantes de chacun desdits premier (PERIOD) et second (VCRMOD) signaux.

7. Circuit selon la revendication 1, caractérisé en ce que lesdits moyens de formation du second signal (120) génèrent ledit second signal (VCRMOD) après que se produit un changement de ladite phase donnée dudit signal d'entrée (H_s) qui conduit ledit signal d'entrée (H_s) à posséder une phase qui est stable et qui est décalée par rapport à ladite phase dudit signal de sortie (CT).

8. Circuit selon la revendication 1, caractérisé en ce que ledit générateur commandable (21) comprend un moyen séquentiel pour générer ledit signal de sortie (CT) selon une séquence d'états qui change en synchronisme avec un signal d'horloge (CK) et dans lequel ledit second signal (VCRMOD) entraîne ladite séquence d'états et la période dudit signal d'entrée (H_s) qui lui correspond à varier selon ledit

second signal (VCRMOD).

9. Circuit selon la revendication 8 caractérisé en ce que, quand ledit changement de ladite phase dudit signal de sortie (CT) qui est entraîné par ledit second signal (VCRMOD) a lieu, il se produit de façon abrupte et en synchronisme avec ledit signal d'horloge (CK).

10. Circuit selon la revendication 1, caractérisé en ce que ledit second signal (VCRMOD) entraîne ledit changement de ladite phase dudit signal de sortie (CT) quand ledit critère prédéterminé est détecté par une quantité qui est reliée à une quantité dont la différence de phase diffère d'une valeur de la différence de phase en régime permanent.

11. Circuit selon la revendication 1, caractérisé en ce que ledit premier signal (PERIOD) est indicateur d'une longueur de période donnée dudit signal de sortie (CT) et dans lequel ledit premier signal (PERIOD) reste sensiblement inchangé quand se produit ladite variation dudit signal indicateur de différence de phase (PH) qui satisfait ledit critère prédéterminé.

